Alternative Design Methodologies for the Next Generation Logic Switch

Invited Paper

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***Abstract*—Next generation logic switch devices are expected to rely on radically new technologies mainly due to the increasing difficulties and limitations of state-of-the-art CMOS switches, which, in turn, will also require innovative design methodologies that are distinctly different from those used for CMOS technologies. In this paper, three alternative emerging technologies are showcased in terms of their requirements for design implementation and in terms of potential advantages. First, a CMOS evolutionary approach based on vertically-stacked gate-all-around Si nanowire FETs is discussed. Next, an alternative design methodology based on ambipolar carbon nanotube FETs is presented. Finally, a novel approach based on the recently discovered memristive devices is presented, offering the possibility of combining memory and logic functions.**

***Index Terms*—logic synthesis, nanowire arrays, cell library, arithmetic blocks**

I. Introduction

DURING the past few years the scaling trend for *complementary-metal-oxide-semiconductor (CMOS)* technology included emerging research directions in order to address the difficult question of voltage scaling, *short-channel-effects (SCEs)* and the exponentially increase of power consumption [1]. Solid state research has introduced novel materials, such as high-κ dielectrics with metal gates, or strained Si or SiGe channel replacement [2]; and by introducing novel configurations, such as double-gate, FinFETs or *gate-all-around (GAA)* constructions [3]. All this required more advanced processing and additional effort in the evaluation of the state-of-the-art technology.

In this respect, one-dimensional channel transistors, such as Si nanowire or Carbon nanotube FETs are among the most promising devices, due to increased performance [4] and for new functionalities [5]. Nevertheless, radically new technologies such as memristive devices also emerge towards the end of Moore's Law scaling, bringing completely new computational paradigms into the realm of design.

In this paper, three alternative emerging technologies are showcased in terms of their requirements for design implementation and in terms of potential advantages. First, a CMOS evolutionary approach based on vertically-stacked gate-all-around Si nanowire FETs is discussed. Next, an alternative design methodology based on ambipolar carbon nanotube FETs is presented. Finally, a novel approach based on the recently discovered memristive devices is presented, offering the possibility of combining memory and logic functions.

II. Overview on vertically-stacked nanowire technology

Vertically-stacked Si nanowire (SiNW) technology makes use of smart processing to fabricate transistors having parallel SiNW channels or *fingers*. As depicted in Figure 1 the basic device is composed of a stack of SiNW channels embedded in a poly-Si GAA structure. Each nanowire strand or channel forms a unit width transistor. The fabrication process was reported earlier by the authors [6] and it employs a combination of *deep-reactive-ion-etching (DRIE)* and sacrificial oxidation steps to form the SiNW channels, starting from a relatively inexpensive standard bulk-Si or SOI substrate. The process allows for easy tuning of vertical and horizontal separation between channels as well as the number of channels to be used for a certain device. All the channels are anchored to source/drain regions. Due to stacking, the SiNW channels will have different values of access resistance. This point is investigated in Section IV. One advantage of this technology is that the width of the transistor is wrapped around the stacked SiNW channels, thus reducing the silicon estate of the active area. In addition, the versatility of stacking a variable number of fingers reduces the active area occupancy even more. Besides, due to the one dimensionality of the channels, specific technology boosters such as strain [7] can be envisaged, enhancing the performance compared with planar SOI technology.

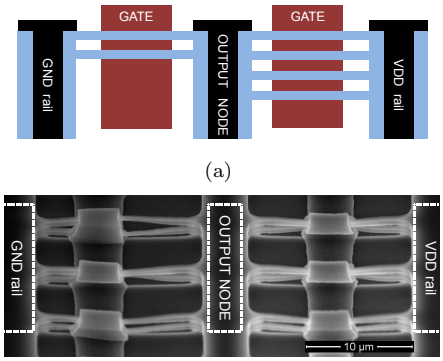

Figure 1. (a) Vertically-stacked inverter structure with SiNW channels anchored to Si pillars with GAA configuration. The electrical equivalent circuit is a CMOS inverter with double drive. The number of SiNW channels is double for pull-up network compared with the pull-down network. (b) Tilted *scanning electron micrograph (SEM)* view of an inverter construction composed of 3 parallel stacks each composed of 4 SiNW channels. In this case pull-up and pull-down transistors have 12 unit width each.

III. Combinational logic design

To assess the performance of complex logic circuits using the vertically-stacked nanowire technology, we perform combinational logic synthesis of carry-lookahead adders that are

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then mapped with vertically-stacked nanowire libraries. The vertically-stacked transistor electrical behavior was modeled as a switch in series of a resistance, which include both access and channel resistance. An estimation of the total diffusion capacitance is also carried out. Then performance and active area estimation are calculated for different combinational logic gates. Finally different libraries of logic gates are built varying both design and technology parameters of the basic transistor cell.

A. Logic gate modeling and libraries

We considered 9 different combinational logic gates that are listed in Table I. We implemented 14 libraries, listed in Table II; every one of them being formed by these 9 logic gates. The libraries include a planar SOI technology and 13 different SiNW technology libraries. These latter are obtained by varying two technology parameters: the access resistance (represented by R_s) and the strain (represented by the actual channel resistance, and a design parameter: the number of nanowire stacks). We designed the 9 logic gates in every library using the linear switch model [8], which assumes that every logic gate is driving the same current as a unit inverter, when it switches. We therefore obtained the required characterization in terms of area and delay. The latter was estimated as the *fanout-of-four (FO4)*, assuming that every gate drives its own intrinsic delay and a loaf of 4 instances of itself. The obtained area, FO4 delay and input capacitance for 3 different sample libraries are illustrated in Table I.

B. Synthesis/mapping results

The ABC tool from Berkeley [9] was used to generate CLAs of 8, 16, 32 and 64 bits. Fast and efficient synthesis with the designed libraries is achieved by DAG-aware rewriting of the *and-inverter-graph (AIG)* representation of the adder network. We used the script *resyn*2 for synthesis, which consist of an alternation of network rewriting and balancing algoritms that reduce the AIG size and the number of AIG levels. The optimized network was then mapped with the different libraries (see Table II). The impact of the different design and technology parameters on mapped CLAs is analyzed in the following.

1) Impact of series resistance on delay: The data refers to FO4 delays of CLAs with different number of bits mapped with single stack configuration. As expected, the FO4 delay linearly increases with series resistance. This behavior is enhanced for adders with more inputs, due to the use of more complex gates. Data points at $\frac{R_s}{R_{channel}} = 0$ correspond to a FO4 delay that is the same of the planar SOI case.

2) Impact of parallelizing stacks on delay and area: The detrimental effect of series resistance can be counterbalanced by using more stacks instead of a single one, thus reducing the effect of R_s on R_{tot} which in turn is reflected on the delay. For instance a 64 bits carry-lookahead adder synthetized with 2 stacks shows an evolution of FO4 delay with series resistace that is 6 times lower than the configuration which uses 1 stack. The speed-up achieved by the double stacking costs additional active area occupancy. However, the total active area occupancy remains lower than the planar case. For instance, the 64 bits CLA with single stack would reduce occupancy area of 49% compared with the one mapped in planar technology. The use of double stack will still reduce occupancy area of 4%. However, the improvement in delay get by using double stack is bigger than the additional cost on area.

3) Impact of strain on delay: More significant performance improvement can be achieved by using strained nanowires. The impact of strain was evaluated varying α within single or double stack configurations. By comparing FO4 delays we notice that strain can effectively counterbalance the effect of series resistance, eventually outperforming planar technology.

IV. Ambipolar CNTFET

The second device structure we present is the double-gate ambipolar Carbon Nanotube FET (CNTFET). This device has a natively one-dimensional channel structure, with channels consisting of an array of Carbon Nanotubes (CNTs) of 1-2nm in diameter [10]. Among the types of CNTFETs demonstrated in literature, independent double-gate ambipolar CNTFETs are four-terminal devices where a second gate terminal is added to control the device polarity. These devices combine performance exceeding that of current scaled MOSFETs, with the possibility to control the device polarity (n or p-type) by electrostatic doping of the nanotubes [11].

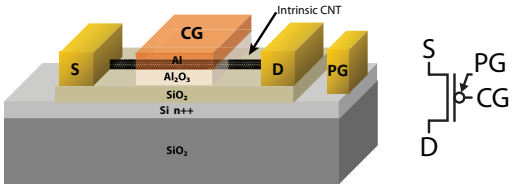

Figure 2. Independent double gate CNTFET structure and device symbol.

Figure 2 shows a possible physical structure for the double gate ambipolar CNTFET. In this device, the CNTs are embedded in a sandwich-like structure with a local top gate, the control gate, and a bottom gate, the polarity gate, which can be shared by multiple devices and controls the device polarity.

A. Gate design considerations and advantages

Ambipolar CNTFETs do not require strong chemical doping, as polarity can be tuned by means of the polarity gate. Moreover, CNTs present similar carrier mobility for both electrons and holes [12], feature which can be exploited to produce intrinsically symmetric devices.

By exploiting the symmetry in conductance between n-type and p-type devices, CNTFET complementary logic gates can be designed to be intrinsically symmetric, e.g. a NOR (shown in Figure 3a) gate can be built from a NAND one (Figure 3b) by simply vertically mirroring its layout. Moreover, the channel of CNTFETs is isolated from the substrate, and does not require wells to obtain proper functionality. These features enable the construction of more compact layouts, adding degrees of freedom on the placement of n, p or ambipolar CNTFETs, which can share different sections of the same nanotube array.

A further advantage can be seen in the implementation of regular layouts, such as gate arrays or structured ASICs [13]. Layouts can be constructed consisting of a chessboard-like tiling of dual logic gates, i.e. a logic cell and the cell produced by switching the pull-up (PU) and pull-down (PD) networks topology, without significantly reducing the overall macro-regularity of the design.

Table I
GATE PARAMETERS OF THREE DIFFERENT LIBRARIES REPORTING ACTIVE AREA OCCUPANCY, FO4 DELAY AND CAPACITIVE INPUT LOAD.

Gate	planar SOI			L06 : SiNW, single stack			L07: SiNW, double stack		
	Active Area [units]	FO4 delay [ps]	C_{in} [C units]	Active Area [units]	FO4 delay [ps]	C_{in} [units]	Active Area [units]	FO4 delay [ps]	C_{in} [units]
INV	3	75	3	2	125	5	3	75	3
NAND2	8	110	4	4	220	7	4	110	4
NAND3	15	145	5	6	315	11	7	195	7
NAND4	24	180	6	8	410	14	10	280	10
NOR2	10	130	5	4	280	11	7	170	7
NOR3	21	185	7	6	435	17	13	315	13
NOR4	36	240	9	8	590	23	19	460	19
MUX2	24	180	6	8	420	14	10	300	10
MUX4	72	240	6	24	560	14	10	400	10

Table II
LIBRARY LIST OBTAINED VARYING SERIES RESISTANCE, NUMBER OF HORIZONTAL STACKS AND $R_{channel}$ REDUCTION DUE TO STRAIN BOOSTER.

Library	$\frac{R_s}{R_{channel}}$	n° of stacks	$\frac{R_{channel,strained}}{R_{channel}}$	add8b		add16b		add32b		add64b	
				Area [units]	Delay [ns]	Area [units]	Delay [ns]	Area [units]	Delay [ns]	Area [units]	Delay [ns]
planar SOI	0%	-	100%	601	1.87	1265	3.87	2593	7.87	5249	15.87
L01	0%	1	100%	302	1.87	638	3.87	1310	7.87	2654	15.87
L02	25%	1	100%	302	2.44	638	5.08	1310	10.36	2654	20.92
L03	25%	2	100%	595	1.97	1267	4.13	2611	8.45	5299	17.09
L04	50%	1	100%	302	2.95	638	6.15	1310	12.55	2654	25.35
L05	50%	2	100%	571	2.02	1211	4.26	2491	8.74	5051	17.7
L06	100%	1	100%	302	3.92	638	8.24	1310	16.88	2654	34.16
L07	100%	2	100%	570	2.17	1210	4.65	2490	9.61	5050	19.53
L08	50%	1	80%	302	2.07	638	4.31	1310	8.79	2654	17.75
L09	50%	2	80%	586	1.61	1211	3.37	2491	6.89	5051	13.93
L10	100%	1	80%	302	2.49	638	5.21	1310	10.65	2654	21.53
L11	100%	2	80%	571	1.66	1211	3.5	2491	7.18	5051	14.54
L12	100%	1	60%	302	2.12	638	4.44	1310	9.08	2654	18.36
L13	100%	2	60%	597	1.29	1261	2.73	2589	5.61	5245	11.37

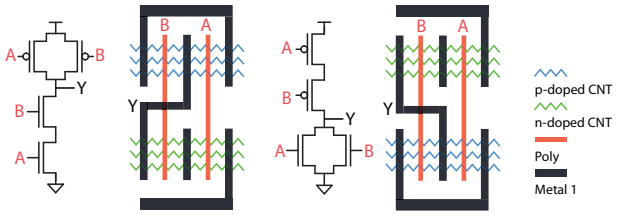

Figure 3. A NOR2 gate layout (b) is derived from a NAND2 layout (a) by simple vertical mirroring.

B. Ambipolar logic design methodology

Two main approaches have been taken to exploit this new feature. In the first case, ambipolar double gate FETs are used as configurable transistors. The polarity gates are fed with appropriate configuration signals by means of SRAM cells or antifuses. Depending on these, the gate can be configured to calculate a set of different logic functions. Such configurable gates have been implemented in dynamic [14] and static logic [15].

In the second approach, polarity gate signals are directly fed with logic signals, and the transistor is polarized at run time. In Figure 4 we can see the simplest logic gate which can be implemented using this methodology [15]. By connecting an ambipolar DG-CNTFET to a pull-up resistor, the output characteristic of this gate is twofold, depending on the polarity gate input. In the case of a positive polarity gate input, the transistor behaves as a n-type FET, thus producing the output of a classical pseudo-logic inverter. Alternatively, if the polarity gate has a negative bias, the transistor behaves as p-type, producing a degraded buffer output characteristic. If we consider this gate as a black box, and see both input signals as high level logic values, we can see that the gate calculates the XNOR logic function.

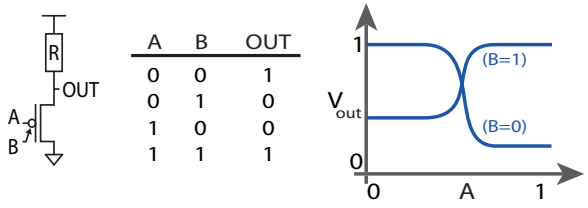

Figure 4. Pseudo-logic gate with a double gate ambipolar CNTFET in the pull-down network. Depending on the value of the polarity input B, the device behaves as an inverter or as a buffer, producing the truth table of an XNOR.

The output of this basic pseudo logic gate is highly degraded, due to the non complementary design, and to the presence of a weakly polarized p-type transistor in the buffer configuration (B=0). A natural extension of this gate, which would restore full swing output, is the addition of a transistor in the pull up network, and by coupling each transistor with another one of opposite polarity. We can then add other transistors to the gate, in a complementary manner, to produce more complex gates, capable to include XOR operators in an efficient manner.

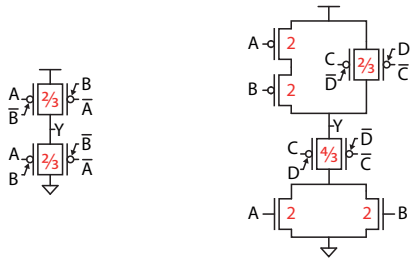

Figure 5. Full swing output XNOR gate (a) and a more complex gate, implementing function $(A+B)\cdot(CD)$. Gate sizes for unitary output strength are shown [16].

V. Perspective on the Multi-Terminal Memristive Devices

Due to the natural limitations of materials, deeply scaled circuits in future technologies will have to exploit more efficient ways for computation and memory storage. One possible scenario envisages the end of charge-based technologies, after which computation will rely on alternative, more power efficient state variable manipulation. However, technologies using new state variables would have to be implemented within a completely new technological platform, and cannot be seen as CMOS-compatible alternatives. The recent realization of HP Labs memristor gave new push to solid state research for logic and memory applications [17].

The memristive functionality is widespread in nature, and it appears in many different multi-terminal devices. The most prominent examples now relate to the 2-terminal solid-state memristors, due to several advantages. In the first place, ultra-dense crossbar memristive memory arrays can be built thanks to the compactness of the two terminal junction. This high density can be very important in a broad range of applications such as CMOL (hybrid of CMOS and molecular technologies), non-volatile memory arrays or as synapse emulator nodes in artificial neural networks. One of the salient features of these devices is the possibility to integrate these into the Back-End-of-the-Line, as these basically consist of a dielectric layer sandwiched between two metal lines. One example of Back-End-of-the-Line implementation demonstrated by the authors [18] the feasibility for 3D programmable/reconfigurable interconnects by combining $Pt/TiO_2/Pt$ memristive layers with Cu Through Silicon Vias.

The memristive functionality is not a unique property of two-terminal passive devices but mainly a memory effect related to internal state variable changes. One such example is the ambipolar Si nanowire Schottky barrier FET [19]. This three-terminal device has an hysteretic behavior that is related to charge trapping at the semiconductor/oxide interface of the MOS capacitor, as well as the existence of interface states at the Schottky junction. This leads to hysteretic $I_{ds}-V_{gs}$ curves (see Figure 6) whose behavior depend upon sweep time, and can be potentially be used as emulator for Spike Time Dependent Plasticity in artificial neural networks.

VI. Conclusions

In this paper we report on alternative design solutions relating to three innovative technologies: vertically-stacked Si nanowire FET arrays, which shows advantages on density in respect with planar SOI. Secondly, the ambipolarity of CNT FETs can be exploited in a dual gate configuration to perform logic operation with intrinsically more compact gates. Finally, multi-terminal memristive devices are presented as novel technology for widespread application range.

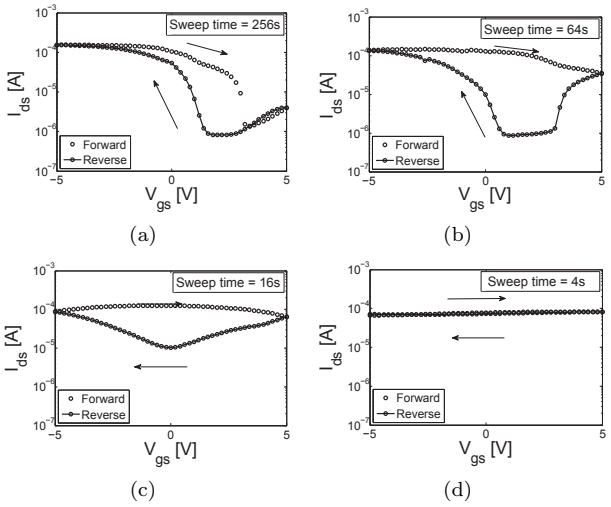

Figure 6. Hysteretic dependence with the measurement (sweep time) duration, the hysteresis window closes by reducing the measurement time: (a) 256 sec. (b) 64 sec. (c) 16 sec. (d) 4 sec.

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