Poly-Silicon Nanowire Transistors and Arrays Fabricated with the Multi-Spacer Technique

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***Abstract*—In this paper, we demonstrate the ability of the *multi-spacer patterning technique (MSPT)* to yield layers of *poly-crystalline silicon nanowires (poly-SiNWs)* with a sub-lithographic pitch, by exclusively using micrometer resolution and *complementary metal-oxide-semiconductor (CMOS)* processing steps. We characterize single spacers operating as *poly-Si nanowire field effect transistors (poly-SiNW FET)*. We demonstrate also the possibility to lay a spacer perpendicularly to a set of parallel spacers in a crossbar fashion. The extrapolated cross-point density from the small 4×1-array is in the range of 10^{10} cm^{-2}. We discuss the applications of this technique to improve the density of previously reported poly-SiNW memories and as a future framework for nanowire crossbars and decoders. Then we analyze the limitations and costs of the proposed technique.**

I. Introduction

Silicon nanowires (SiNW) are promising candidates for continuing the scaling of *complementary metal-oxide-semiconductor (CMOS)* technology. The increasing costs of photolithography motivates the development of lithography-independent *nanowire (NW)* fabrication processes. These techniques can be divided into bottom-up approaches based on SiNW growth from a catalyst [1] and top-down approaches based on accurate control of etching and oxidation of Si [2] and deposition of poly-Si [3], [4] (for SiNW and poly-SiNW respectively).

Even though nanowires with sub-photolithographic width below 10 nm have been demonstrated, their pitch, which is the sum of their width and spacing, is generally defined by photolithography. The pitch, which is the spacing between two successive nanowires in the layer, is more representative of the nanowire density. Thus, it is highly desirable to develop techniques yielding a photolithography-independent nanowire pitch in order to increase the overall integration density.

The paradigm of arranging arrays of parallel nanowires perpendicular to each other in a crossbar fashion received the attention of many research groups. The dense crossbars can perform logic or store information at the cross-points, which contain bistable molecules or phase-change materials [5], [6]. To access every nanowire in the crossbar from the outer CMOS circuit, the utilization of a decoder consisting of a set of access devices operating as *silicon nanowire field effect transistors (SiNW FETs)* was suggested [7], [8].

The purpose of this work is to investigate the possibilities offered by the *multi-spacer patterning technique (MSPT)* in terms of structural and electrical properties of the fabricated sub-lithographic structures, to assess the opportunity of arranging them into crossbar arrays and to address the challenges and limitations of the proposed technique.

This paper is organized as follows. Sec. 2 surveys the background and previous work related to the spacer technology and introduces the baseline organization of crossbar circuits that can be fabricated with this technology. Sec. 3 introduces the fabrication process and Sec. 4 presents the obtained results including a structural and an electrical characterization of the fabricated structures. Sec. 5 explains possible applications of the presented technique and Sec. 6 discusses its challenges related to the technology and the circuit architecture. The conclusion is given in Sec. 7.

II. Background and Related Work

In the following, previously reported work with the spacer technology is surveyed. The interest in applying this technology to nanowire crossbar circuits is then motivated and the overall architecture of crossbars is explained.

A. Spacer Technology

The spacer technique has been suggested as a possible fabrication process that yields parallel nanowires. In general, nanowire fabrication techniques can be divided into bottom-up and top-down approaches. Bottom-up techniques are based on the growth of nanowires on a silicon substrate from catalyst seeds. The as-grown nanowires are then collected in a solution and dispersed on top of the substrate to be functionalized [9], [10]. In top-down approaches, nanowires are directly defined on the functional substrate by accurately controlling the deposition, oxidation and etching rates [11], [4], or by using nanometer-scale molds whose pattern can be transferred onto another substrate using the nanomold imprint lithography [12].

With the spacer technique it is possible to control device dimensions below the photolithographic limit [13], [14] yielding sub-lithographic nanowires with a top-down approach. The approach is based on the definition of a spacer by conformally depositing a material at the edge of a sacrificial layer and then anisotropically etching it. The width of the spacer depends on the thickness of the deposited material, which can be

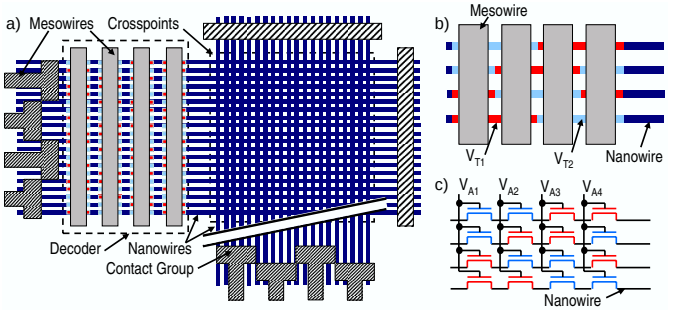

Fig. 1. Baseline architecture of a crossbar circuit (a) and highlights of the decoder layout (b) and circuit (c)

controlled accurately–often on the scale length below 1 nm–without any dependence on the photolithographic dimensions. By removing the sacrificial layer, the spacer can be used as a hard mask to define structures in the underlying layers. The spacer technique has been applied in order to fabricate *fin field effect transistors (Fin FETs)* with shorter gate length and higher performance than lithographically defined *metal-oxide-semiconductor field effect transistors (MOS FETs)* [15], [16], [17], [18]. Devices made with the spacer technique have been deployed in other fields as well, such as optical applications [19], high-frequency transistors [20] and bio-sensing [21].

The spacer patterning process is maskless and self-aligned, which makes it a very attractive way to shrink dimensions. However, it necessitates additional deposition and etch steps. Interestingly, the spacer patterning can be iterated several times, resulting in the *multi-spacer patterning technique*. For instance, every spacer can be used as a sacrificial layer for the following spacer. This iterative approach, called the *multiplicative road* [22], is a possible way to reduce the lithographic pitch by a factor of 2^n, with n the number of iterations [13], [21]. Another approach based on the iterative definition of successive spacers by alternating semiconducting (poly-Si) and insulting materials (SiO_2) defined on the edge of the same sacrificial layer [4], is a second way to obtain layers of nanowires with a sub-lithographic pitch, and it is called the *additive road* [22]. Either approaches have been used in order to define dense nanowire molds. The pattern of such nanomolds is subsequently transferred onto a different substrate by nanomold imprint lithography in order to define layers of micrometer long and parallel nanowires [21], [23].

B. Baseline Circuit Architecture

The increasing interest in fabricating dense layers of parallel nanowires with a sub-lithographic pitch is motivated by the emergence of the nanowire crossbar paradigm as a possible architecture for post-CMOS technologies [24], [25], [26]. The baseline organization of a nanowire crossbar circuit is depicted in Fig 1(a). An arrangement of two orthogonal layers of parallel nanowires defines a regular grid of intersections called cross-points. Phase-change materials or molecular switches can fill the separation between the two layers at the cross-points; thus performing information storage, interconnection or computation at these cross-points [27], [28]. A set of contact groups is defined on top of the nanowires. Every contact group has an ohmic contact to a corresponding set of nanowires that represents the smallest set of nanowires that can be contacted by the lithographically-defined lines (mesowires).

Every set of nanowires within a contact group is connected to the outer CMOS circuit through the mesowires. A decoder is utilized in order to make every nanowire within this set uniquely addressable by the outer circuit. It is formed by a series of transistors along the nanowire body, controlled by the mesowires and having different threshold voltages [29], as shown in Fig. 1(b) and 1(c). Depending on the distributions of threshold voltages of the series transistors along the nanowires and on the sequence of applied voltages in the decoder (V_A's), one single nanowire in the array can be made conductive, which is required for a correct addressing operation.

Many decoders have been suggested for nanowire arrays. Their design strongly depends on the nanowire fabrication technology. Axial and radial decoders are proposed for nanowires fabricated with a bottom-up approach [30], [31] and they are based on random dispersion of nanowires whose pattern is defined by in-situ doping. Mask-based decoders [8] are proposed for nanowires fabricated with a top-down approach, whose pattern is deterministically defined by using a conventional mask. Random-contact decoders [32] are an alternative approach for top-down nanowires, whereby the nanowire pattern is defined through stochastic contacts. For other bottom-up techniques with a large pitch, a gate-all-around decoder is suggested in [11]. A conceptual approach to fabricate and designing a specific decoder with the spacer technique is presented in [33].

C. Spacer-Based Nanowire Crossbars

Given the ability of the MSPT to yield parallel nanowires, it is therefore interesting to investigate the opportunities of fabricating crossbar circuits with the MSPT. As a matter of fact, despite the additional deposition and etch step, this maskless and self-aligned technique offers an interesting alternative approach to high-resolution lithography (electron beam or ultraviolet lithography), which are slow or/and expensive; and to nanoimprint lithography, which may require special measures to align the nanomold to wafers. Poly-Si spacers can be deposited at 600 to 700°C. Consequently, the integration of crossbars into a CMOS process can be carried out between front- and back-end process steps. Once the metallization is finished, the molecular switches are dispersed onto the wafer, and they attach to the cross-points with self-assembly [34].

However, when the suitability of a technology for crossbar circuits is evaluated, there are two important parts of the circuit to be considered separately: the crossbar and the decoder.

When it comes to the fabrication of crossbars with the MSPT, *i.e.*, crossing nanowires, we notice to the best of our knowledge that only parallel spacers have been demonstrated with the MSPT and used as stand-alone nanowires [22] or as nanomold to pattern different substrates [21]. Crossing nanowires have not been demonstrated with the MSPT yet. In this paper, this opportunity is investigated and crossing nanowires based on the MSPT are demonstrated. This step

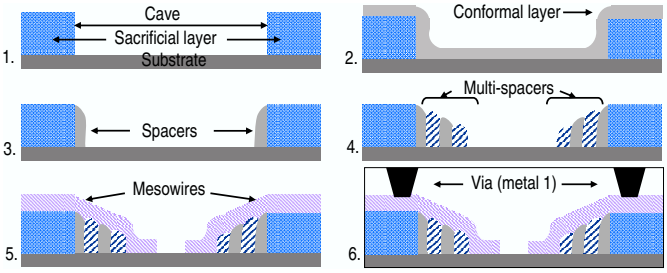

Fig. 2. Main process steps: (1) Definition of sacrificial layers (2) Conformal deposition of poly-Si. (3) RIE etch. (4) Alternation of poly-Si/SiO_2 spacers. (5) Definition of the gate stack. (6) Passivation and metallization.

is key in achieving the ultimate goal of full crossbar design with the MSPT.

The decoder is a critical part of the circuit, since it bridges the crossbar and the rest of the CMOS circuit. From previously demonstrated or suggested techniques [30], [31], [8], [32], [11], [33], it has been shown that the decoder fabrication and design techniques highly depend on the existing nanowire technology. The yield, measured in this context simply as the percentage of nanowires that can be addressed, can be low if the technology allows only a stochastic decoder design [30], [32]. On the other hand, the decoder size, measured as the number of mesowires needed in order to address a given number of nanowires, may have a considerable overhead depending on the technology. The iterative aspect of the MSPT can be efficiently utilized in order to design a decoder with a compact size [33]. The benefits of the MSPT in designing the decoder is addressed in this paper and the compactness of the decoder compared to other existing approaches is highlighted.

This work addresses the utilization of the spacer technique for the fabrication of nanowire crossbars. Unlike previous approaches that used the MSPT to define simple layers of parallel nanowires [13], [4], [20], and those that used the MSPT to define nanomolds to pattern nanowires [19], [21], [23], this work demonstrates for the first time *i*) that not only layers of parallel nanowires, but also dense nanowire crossbars can be fabricated with the MSPT, and *ii*) that MSPT-based crossbars can be obtained in a self-aligned and maskless process without the utilization of any nanomold. The scalability of the as-fabricated poly-Si crossbars is studied, and the characterization of the access devices operating as poly-SiNW FETs is performed for the first time.

III. Fabrication Process

The fabrication process of a single nanowire layer is described in Fig. 2. The main idea of the process is the iterative definition of thin spacers with alternating semiconducting and insulating materials, which result in semiconducting and insulating nanowires. We start by defining a $1\ \mu\mathrm{m}$ SiO_2 layer on a Boron-doped Si substrate (p-type, 0.1 to 0.5 $\Omega \cdot \mathrm{cm}$) with wet oxidation. Then, we define a sacrificial layer (step 1) with a height of 500 nm in the wet oxide. Then, we deposit a thin conformal layer of poly-Si with a thickness ranging from 40 to 90 nm by *low pressure chemical vapor deposition (LPCVD)*, where SiH_4 is deposited at $600^\circ\mathrm{C}$ (step 2). Subsequently, we etch this layer with a *reactive ion etching (RIE)* equipment using Cl_2 plasma, in order to remove the horizontal layer while keeping the sidewall as a spacer (step 3); and we densify the poly-Si spacer at $700^\circ\mathrm{C}$ for 1 h under N_2 flow. Then, we partially oxidize the poly-Si spacer at $900^\circ\mathrm{C}$ under O_2 flow in order to obtain an insulating layer between the successive poly-Si spacers. Alternatively, we deposit a conformal insulating layer by using a 40 to 80 nm thin *low temperature oxide (LTO)* obtained by LPCVD following the reaction of SiH_4 and O_2 at $425^\circ\mathrm{C}$. The deposited LTO is densified at $700^\circ\mathrm{C}$ for 45 min under N_2 flow, then it is etched in a RIE etchant using C_4F_8 plasma in order to remove the horizontal layer and just keep the vertical spacer. We perform these two operations (poly-Si and SiO_2 spacer definition) one to six times in order to obtain a multi-spacer with 2 to 12 alternating poly-Si and SiO_2 nanowires (step 4).

In order to address the issue of realizing a crossbar framework, we fabricate the bottom multi-spacer as explained previously, then we grew 20 nm dry oxide as an insulator between the top and bottom nanowire layers. The top sacrificial layer is defined with LTO perpendicular to the direction of the bottom sacrificial layer. Then a poly-Si spacer is defined at the edge of the top sacrificial layer in a similar way to the bottom poly-Si spacers. Subsequently, the separation dry oxide and both sacrificial layers are removed in a buffered HF solution in order to visualize the crossing poly-Si spacers realizing a small poly-Si nanowire crossbar.

In another set of wafers, we address the issue of characterizing a single access device (poly-SiNW FET). In this case, we use a single nanowire layer with one 67 nm wide poly-SiNW, on top of which we define a gate stack with an oxide thickness of 20 nm and different gate lengths (step 5). The drain and source regions of the undoped poly-SiNW were defined by the electron-beam evaporation of 10 nm Cr and 50 nm nichrome $Ni_{0.8}Cr_{0.2}$ (step 6). The use of Cr enhanced the adhesion and resistance of Ni to oxidation during the two-step annealing (5 min at $200^\circ\mathrm{C}$, then 5 min at $400^\circ\mathrm{C}$).

IV. Characterization of the Structures

This section presents the fabricated devices with the previously introduced process flow. The scalability and ability of the process to yield crossing nanowires are demonstrated, and the electrical characterization of access devices, operating as poly-SiNW FET, is reported.

A. Structural Characterization

We first assessed the structural properties of arrays of parallel nanowires fabricated with the proposed technique. Figure 3 shows a sequence of 6 double-spacers formed by poly-Si over SiO_2. Every double-spacer was obtained by poly-Si deposition, etch and then partial dry oxidation at $900^\circ\mathrm{C}$. Despite the ability to repeat the spacer definition steps several times, the edge roughness was too high because of the utilization of poly-Si and the subsequent etch and oxidation steps. It is expected that the poly-Si grain size is approximately equal to the thickness of the deposited layer, *i.e.*, about 80 nm in Fig. 3. The etch step increases the surface roughness. The

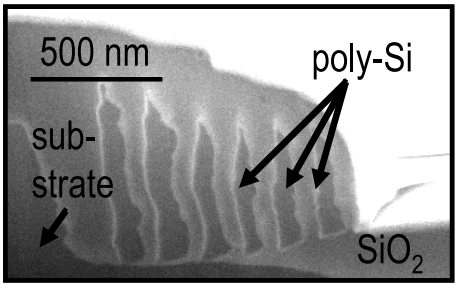

Fig. 3. SEM image of a focused-ion-beam (FIB) cross-section of 6× poly-Si/dry oxide double-spacer.

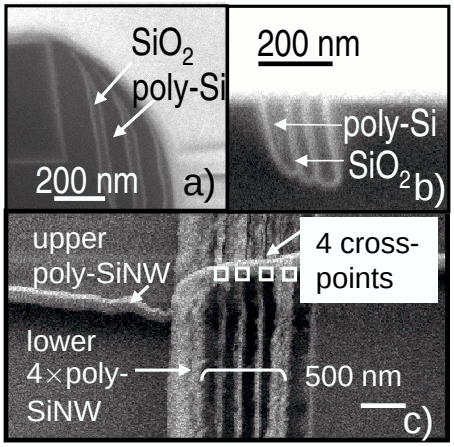

Fig. 4. SEM images of multi-spacers and a small crossbar. (a) Alternating 54 nm thin poly-Si and LTO spacers. (b) Scaling down to 20 nm thin poly-Si. (c) Small 4×1 crossbar with 1 upper and 4 lower poly-Si spacers.

subsequent high-temperature oxidation highly intensifies the edge roughness because the oxidation rate is not homogeneous close to the contact locations between neighboring poly-Si grains.

In order to reduce the vertical surface roughness of poly-Si spacers, we utilized LTO instead of the dry oxide. Figure 4(a) shows a SEM image of 3 poly-SiNW separated by LTO NWs. All the poly-SiNWs have a uniform thickness of 54 nm, with an improved surface roughness. The height of the first poly-SiNW is about the height of the sacrificial layer and it has a rounded corner due to the conformal poly-Si deposition and the following etching procedure. The rounded-corner effect is intensified with the increasing number of spacers resulting in a decrease of the poly-SiNW height with the number of nanowires in the multi-spacer. A NW length of hundreds of micrometers could be achieved, with no nanowire interruption. Our technique has a high yield: in all samples characterized with SEM (over 100 samples on 8 different wafers) no broken nanowires have been seen. We also investigated the scalability of this technique by depositing thinner poly-Si layers (40 nm): Figure 4(b) shows that the obtained poly-SiNW have a width of 20 nm. For the device in this SEM image, we planarized the multi-spacer after it was defined by *chemical mechanical polishing (CMP)* in order to remove the rounded-corner effect reported in Figure 4(a). CMP is therefore a possible way to remove the rounded corners if they are not desirable. The possible use of the MSPT for the fabrication of two perpendicular layers of crossing NWs is illustrated in Figure 4(c) with one poly-SiNW crossing 4 poly-SiNWs underneath it. The first nanowire to the right is wider than the three others because it was defined with a thicker deposited poly-Si layer. Here again, the length of the nanowires in the crossbar could be made as large as desired without any noticeable nanowire interruption.

B. Electrical Characterization

The need to access the nanowires and control the current flow through them motivates for the definition of access transistors having a poly-Si spacer as a channel. We characterized undoped poly-SiNW FETs (single poly-Si spacer) with nichrome ($Ni_{0.8}Cr_{0.2}$) drain and source contacts and with a nanowire channel length $L = 20\ \mu\mathrm{m}$ and a fin width $W = 67\ \mathrm{nm}$. We used a back gate formed by p-doped Si substrate (0.1 to 0.5 $\Omega \cdot \mathrm{cm}$) and the thick back gate oxide corresponds to the cave thickness $\sim 0.4\ \mu\mathrm{m}$.

The I_{ds}-V_{gs} curves show an ambipolar behavior, with a current conductance under either high positive or negative gate voltage (Figure 5). The type of metal to poly-Si contact plays a major role in the reported ambipolar behavior. Chromium present in metallic Cr-alloys generally migrates to the surface when the alloy is heated. During the two-step annealing, the underlying Cr and the Cr in the nichrome alloy migrate to the metal-to-air surface and protect the contact from oxidation. This was experimentally checked by comparing the oxidation rate of a pure nickel contact to one of the contact used in the measured devices. During the annealing step, the poly-Si is therefore in direct contact to the almost pure Ni. At $400°\mathrm{C}$, Ni reacts with Si to form a nickel silicide contact [35]. This contact can result in ambipolar devices [36]. The Schottky barrier for electrons with this kind of contact has been reported by some groups as high as 0.57 eV [37], while it is believed to be about 0.61 eV in bulk silicon [38].

In the measured structures, the $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio was $\sim 2 \times 10^4$ and $\sim\ 4 \times 10^3$ for p- and n-branch respectively. The low $I_{\mathrm{on}} = 0.2\ \mu\mathrm{A}$ and $0.1\ \mu\mathrm{A}$ for p- and n-branches respectively is explained by the low W/L ratio (NW width $W = 67\ \mathrm{nm}$, gate length $L = 20\ \mu\mathrm{m}$) and the low mobility in poly-Si. The Shottky barrier for holes (0.51 to 0.55 eV) may be slightly lower than for electrons (0.61 to 0.57 eV), which explains the higher I_{on}-current in the p-branch. During these measurements, the gate leakage for large positive and negative gate voltages was about 2 to 3 orders of magnitude lower than the drain current.

The I_{ds}-V_{gs} curve showed a hysteretic behavior as depicted in Fig. 6, whereby the labels (1) to (4) indicate the direction of the hysteresis. By enlarging the V_{gs} sweep range from [-10 V, 10 V] to [-40 V, 40 V], the hysteresis width became larger. This hysteretic behavior confirms the high density of trapped charges in the poly-Si grains and at the interface between the poly-Si channel and the gate oxide. The density of trapped charges depends on the applied field, explaining the dependence of the hysteresis width on the gate voltage range.

The ability to control the devices in a FET fashion proves their possible use as access devices to the NW layer within a decoder [33]. The ambipolarity is due to the intrinsic poly-Si

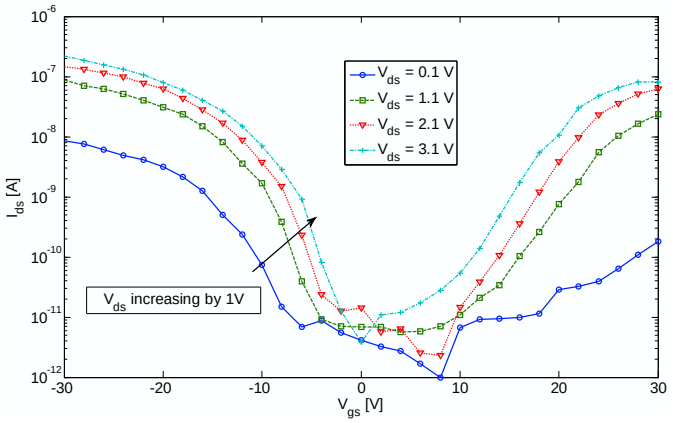

Fig. 5. $I_{\rm ds}$-$V_{\rm gs}$ curve of an undoped single poly-SiNW with a back-gate and nichrome drain/sourse ($L = 20$ μm, $W = 67$ nm).

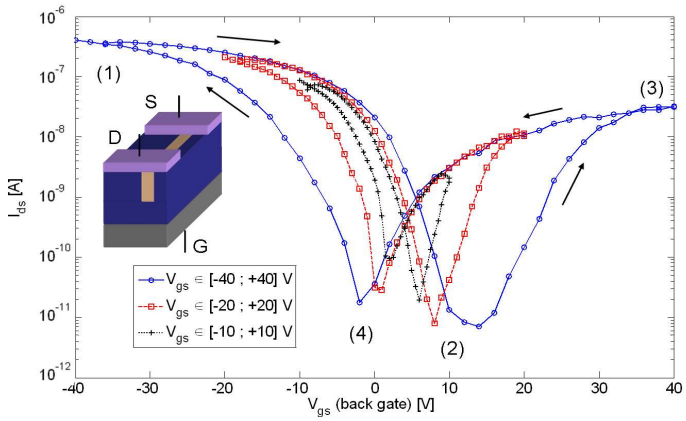

Fig. 6. Hysteresis of the $I_{\rm ds}$-$V_{\rm gs}$ curve shown in Fig. 5 for $V_{\rm ds} = 3.1$ V.

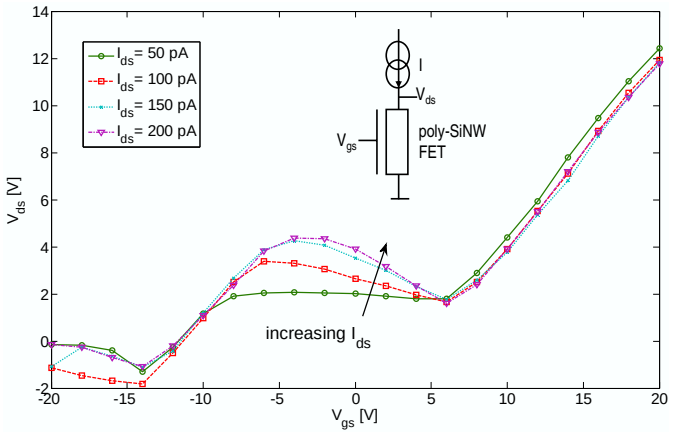

Fig. 7. $V_{\rm ds}$-$V_{\rm gs}$ transfer characteristics for fixed $I_{\rm ds}$ bias of an undoped single poly-SiNW with a back gate and nichrome drain/source.

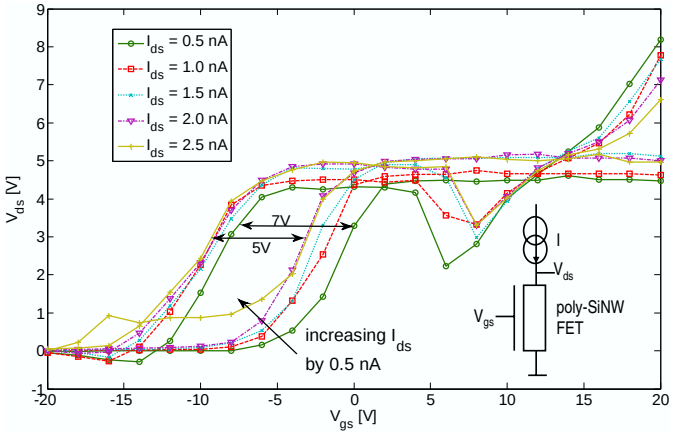

Fig. 8. Hysteresis of the $V_{\rm ds}$-$V_{\rm gs}$ transfer characteristic in Fig. 7.

and the mid-gap contact metal. By using implanted contact regions and metal contact, the unipolar behavior is expected to be achieved [35].

We also plotted the transfer characteristics $V_{\rm ds}$-$V_{\rm gs}$ for a fixed $I_{\rm ds}$ (Figure 7), which has a clear negative slope region. The same transfer characteristics have a hysteresis of 5 to 7 V, which decreases with increasing injected current $I_{\rm ds}$ (Figure 8). The measured hysteresis is in agreement with the behavior of poly-SiNW reported in literature and it can be explored in single nanowire memories [3].

V. Potential Applications

The reported results in the previous section have different application fields. This section explains the possible future utilization of the MSPT as a framework for nanowire crossbars, dense single NW memories and compact nanowire decoders.

A. Crossbar Framework

A promising application of SiNWs is the fabrication of crossbar structures, which can be functionalized in order to operate as a memory or as a computational unit such as a *programmable logic array (PLA)* [25]. Previous approaches to build NW crossbars achieved either *i*) metallic arrays, which do not have any semiconducting part that can be used as an access transistor, or *ii*) silicon-based crossbars with fluidic assembly, which have a larger pitch in average than the photolithography limit. Table I surveys the reported realized crossbars and shows that our technique has both advantages of yielding semiconducting NWs and a high cross-point density $\sim 10^{10}$ cm^{-2}, as measured in the small crossbar of Fig. 4(c), while using conventional photolithographic processing steps. The use of the densest layers (Fig. 4(b)) would yield a higher cross-point density of $\sim 6.3 \times 10^{10}$ cm^{-2}.

The demonstrated crossbar framework shows only the nanowires. However, a functional crossbar must be functionalized by inserting molecular switches or phase-change materials at the cross-points in order to perform the function of the circuit: logic, memory or interconnect. The design of molecular switches is beyond the scope of this paper: the underlying chemistry and the grafting mechanism of molecular switches to nanowires were investigated in [34].

B. Single Poly-SiNW Memory

Besides the application as a crossbar array, there is a second conceptual application as poly-SiNW memory based on the hysteresis of the $V_{\rm ds}$-$V_{\rm gs}$ transfer characteristic for a fixed $I_{\rm ds}$.

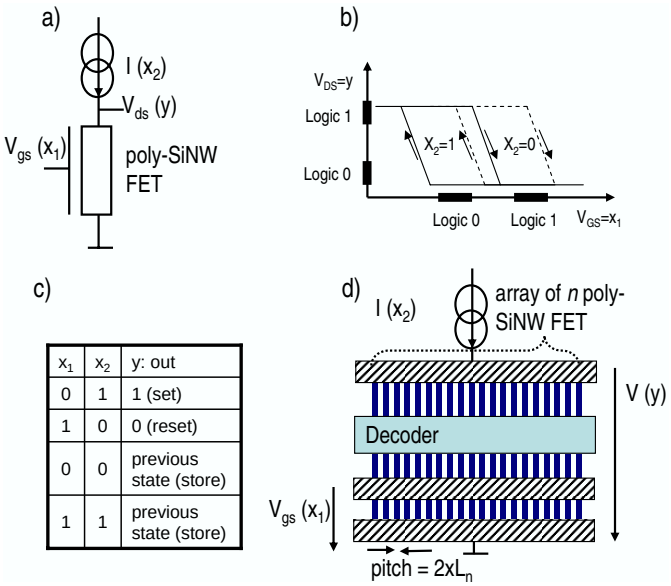

Fig. 9. (a) Poly-SiNW memory cell after [3]. (b) Mapping of logic states onto hyteretic loops. (c) Memory operation principle. (d) Higher density realization concept of poly-SiNW memory cell with the MSPT.

The idea comes from the demonstrated concept of a poly-SiNW memory cell in [3] and the memory operation was experimentally demonstrated in [3] using $I_{\rm ds}$ and $V_{\rm gs}$ as inputs and $V_{\rm ds}$ as output storing the information. A single poly-SiNW memory cell after [3] is illustrated in Fig. 9(a). For detailed description, the operation was reported in [3] and it is based on the choice of two adjacent $V_{\rm ds}$-$V_{\rm gs}$ hysteresis loops corresponding to two distinct $I_{\rm ds}$ current levels for logic 0 and 1 respectively (Fig. 9(b)). The memory state is stored in the output variable $V_{\rm ds}$ (y), and it can be set to 0 or 1 by applying the right sequence of input variables $V_{\rm gs}$ (x_1) and $I_{\rm ds}$ (x_2) as explained in [3]. A summery of the memory operation is given in Fig. 9(c).

This poly-SiNW memory cell proposed in [3] is based on a single nanowire. The half-pitch separating two adjacent cells is equal to the lithographic half-pitch in the best case. Given the fact that the MSPT yields lithography-*in*dependent nanowire pitch, it is possible to think of combining the MSPT with the idea of poly-SiNW memory cells proposed in [3], in order to reduce the distance between two adjacent cells below the lithographic half-pitch. A conceptual scheme of the MSPT-based poly-SiNW memory cells is depicted in Fig. 9(d). In this conceptual configuration, the pitch of the poly-SiNW is not limited by the lithography anymore, but it rather depends on the MSPT pitch, which can be below the lithography pitch. In order to control the nanowire corresponding to the cell to be addressed, a decoder is needed and it is included in the cell scheme. More details about the decoder fabrication and design for parallel nanowires are presented in the following section.

C. Nanowire Decoder

Fabricating crossbars with a sub-photolithographic pitch raises the question of how to make every nanowire addressed by the outer CMOS circuit through a decoder. The design of crossbar decoders has attracted a lot of attention and the proposed solutions are either analog [7] or digital. Among the digital decoders, there are stochastic [30], [31], [32] and deterministic approaches [8], [33].

A possible metrics that can be used to compare decoders is their size given by M, the required number of mesowires needed to address N nanowires. Using nanowires doped withe different doses and the same type (either n or p), the minimal cost is given by $M = 2 \cdot \lceil \log_2(N) \rceil$ [29]. The minimal cost is just the half of this values, when a complementary logic (using both n- and p-type) is used; however, for technological reasons, this is not expected to be the case for nanowire decoders [29]. The randomness of stochastic approaches [30], [31], [32] results in a large overhead in M. Even the deterministic approach in [8] needs a certain overhead due to the dimension mismatch between nano- and mesowires. The cost M for these approaches is summarized in Table II.

We have proposed a concept of a deterministic digital decoder for MSPT-based crossbars in [33], which is expected to yield the lowest possible cost for M (Table II). The multi-spacer patterning technique has the advantage of enabling the fabrication of a deterministic nanowire decoder with a minimal size M, which cannot be achieved with other techniques requiring a certain overhead for M. If the MSPT approach is applied for the decoder, then unipolar access transistors are needed, which requires the implantation of source and drain regions instead of using the proposed nichrome contact.

VI. Discussions

Despite the various potential applications of the MSPT, many aspects are challenging the fabrication and the organization of the crossbar circuits. This section explains these challenges and shows possible opportunities to address them.

A. Process Limitations

The structural characterization reported in Sec. IV-A shows a high edge roughness due to the utilization of poly-Si. The edge roughness is intensified by the subsequent etch and eventually oxidation steps. The utilization of LTO instead of the dry oxide as a insulating layer between successive poly-Si spacers helped noticeably reduce the vertical edge roughness (Fig. 4(a) vs. Fig. 3). However, the topside of the poly-Si spacers still has a high roughness (Fig. 4(c)), which requires a planarization of the structure with CMP following the definition of the whole multi-spacer (as shown in Fig. 4(b)).

The scalability of the fabricated structures is limited by the ability to reduce and control the size of the deposited poly-Si grains in the range of a few tens of nanometer or less. If the ability to deposit thin (below 10 nm) and smooth poly-Si layers is limited, then the MSPT approach becomes less competitive with highly scaled photolithography-based nanowires.

Despite the fact that the definition of the spacers is exclusively based on self-aligned steps, the orientation of the crossing spacer planes with respect to each other depends on the alignment of the masks used to define the sacrificial layers.

TABLE I
SURVEY OF REPORTED NANOWIRE CROSSBARS (FUNCTIONALIZATION MEANS USAGE OF MOLECULAR SWITCHES)

Reference	[12]	[39]	[5]	[1]	This work
NW material	Pt	Ti/Si	Ti/Pt	Si	poly-Si
NW thickness [nm]	8	16	30	20	54
NW pitch [nm]	16	33	60	>1000	100
Cross-point density [cm^{-2}]	10^{11}	9.5×10^{10}	2.7×10^{10}	low	10^{10}
NW technique	SNAP	SNAP	NIL	Fluidic Assembly	MSPT
Functionalization	∅	✓	✓	∅	∅

TABLE II
SURVEY OF REPORTED DIGITAL NANOWIRE DECODERS

Reference	[30]	[31]	[32]	[8]	[33]
NW technique	Fluidic Assembly	Fluidic Assembly	Any Top-Down	NIL/SNAP	MSPT (this work)
NW decoder	Axial Decoder	Radial Decoder	Random Contact Decoder	Mask-Based Decoder	MSPT Decoder
Decoder type	Stochastic	Stochastic	Stochastic	Deterministic	Deterministic
M **(Decoder size)**	$\lceil 2.2 \cdot \log_2(N) \rceil + 11$	$\lceil 2.2 \cdot \log_2(N) \rceil + 11$	$\lceil 4.8 \cdot \log_2(N) \rceil + \mathcal{O}(1)$	$2.0 \cdot \lceil \log_2(N) \rceil + \mathcal{O}(1)$	$2.0 \cdot \lceil \log_2(N) \rceil$

Therefore, a special care has to be taken to accurately align these steps in order to insure that the crossing nanowires are perpendicular to each other.

B. Process Cost

One important question that may arise when it comes to the MSPT is the cost of the additional conformal deposition and RIE etch steps. The fabrication time needed for a 256×256 nanowire crossbar (8 kB memory) would be tremendous if 2×256 deposition/etch operations were required. Fortunately, the MSPT has two advantages. First, it can be parallelized within a single wafer: *i.e.*, by using n parallel sacrificial layers instead of one, the number of deposition/etch steps is divided by n (Fig. 10(a)). Second, the technique allows for parallel batch processing, *i.e.*, any two different batches can be processed together during the deposition/etch steps as long as the thickness of the conformal layers is the same (Fig. 10(b)).

In general, within-die parallelization should be preferred in order to keep n as large as possible. The factor n is chosen such that the width of every cave is matched by the lithographic dimensions, making the number of nanowires in every cave in the range $\sim 3 \times L_{\rm l}/L_{\rm n}$. The factor 3 comes from the symmetry of the caves and the possible need for some overhead in order to bridge the lithographic and sub-lithographic dimensions [29]. For instance, at the 65 nm technology node ($L_{\rm l} = 65$ nm) and with 20 nm wide nanowires ($L_{\rm n} = 20$ nm), n should be chosen such that every cave has ~ 10 parallel nanowires. Given the symmetry of the cave, the number of deposition/etch procedures is only 5 instead of 256. Then, for the full crossbar made of two layers, 10 deposition/etch procedures are needed instead of 512.

C. Circuit Architecture

Another important question about the proposed technique is related to the lower mobility of current carriers in the poly-Si used to define the structure, compared to crystalline Si. The question was generalized previously for any crossbar type: whatever the used NW material is, the structure length and small cross-section will induce a slower signal propagation and higher resistance. To address this fact, it is generally believed [40] that the benefit of crossbars is to parallelize memory and computation in a grid with a large number of small crossbars, rather than using a limited number of large crossbars.

VII. CONCLUSIONS

Many efforts are concentrated on the scaling of SiNWs, but fewer research works offered solutions to scale the NW pitch with standard CMOS process steps in an *in*dependent way on the photolithography. We used the MSPT in order to fabricate dense and lithography-independent poly-SiNWs with standard CMOS steps and micrometer lithography resolution, achieving a very high yield with a sub-lithographic density. In contrast to previous approaches, we did not only define parallel nanowire layers, but we also demonstrated the possibility of having crossing spacers in a crossbar fashion. In addition, we used the MSPT not for the definition of nanomolds as in some previous approaches, rather for the direct definition of the crossing spacers, which makes the process self-aligned and maskless. We characterized the poly-SiNWs fabricated with this technique. We reported their ambipolarity and a hysteresis in their $V_{\rm ds}$-$V_{\rm gs}$ transfer characteristic due to the contact and channel types. We also demonstrated the capability of the MSPT to yield crossing spacers with an extrapolated cross-point density of 10^{10} cm^{-2}. We explored potential future application fields of the presented technique, such as dense memory arrays of single poly-SiNWs and nanowire logic decoders, and we analyzed the technological costs challenging this technique.

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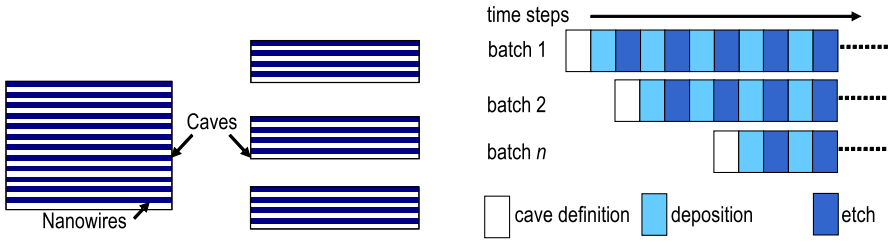

(a) Within-die parallelization (b) Batch parallelization

Fig. 10. Parallelization of the MSPT. (a) Using many small caves instead of a few large ones minimizes the number of steps, but has a cost in terms of area. (b) Any two batches can be processed together during the spacer definition steps, as long as the spacer parameters are identical.

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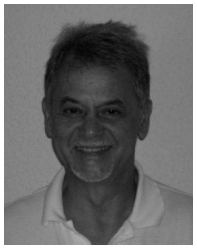

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