Carbon Nanotube Correlation: Promising Opportunity for CNFET Circuit Yield Enhancement

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Abstract

Carbon Nanotubes (CNTs) are grown using chemical synthesis, and the exact positioning and chirality of CNTs are very difficult to control. As a result, "small-width" Carbon Nanotube Field-Effect Transistors (CNFETs) can have a high probability of containing no semiconducting CNTs, resulting in CNFET failures. Upsizing these vulnerable small-width CNFETs is an expensive design choice since it can result in substantial area/power penalties. This paper introduces a processing/design co-optimization approach to reduce probability of CNFET failures at the chip-level. Large degree of spatial correlation observed in directional CNT growth presents a unique opportunity for such optimization. Maximum benefits from such correlation can be realized by enforcing the active regions of CNFETs to be aligned with each other. This approach relaxes the device-level failure probability requirement by 350X at the 45nm technology node, leading to significantly reduced costs associated with upsizing the small-width CNFETs.

Categories and Subject Descriptors
B.7 [Hardware]: Integrated Circuits

General Terms
Design, Performance, Reliability

Keywords
Carbon Nanotube, CNT, Yield Optimization, CNT Correlation.

1. Introduction

Carbon Nanotube Field-Effect Transistors (CNFETs) are considered to be promising candidate devices for future technology nodes due to their superior electrostatic and transport properties [Avouris 07, Deng 07, Wei 09]. A representative CNFET device structure is shown in Fig. 1.1. Multiple Single-Walled Carbon Nanotubes (SWCNTs, or simply CNTs) are grown or transferred onto a substrate; these CNTs act as channels which can be modulated by a transistor gate. The active region is the region that encloses a CNFET – CNTs outside the active regions are removed.

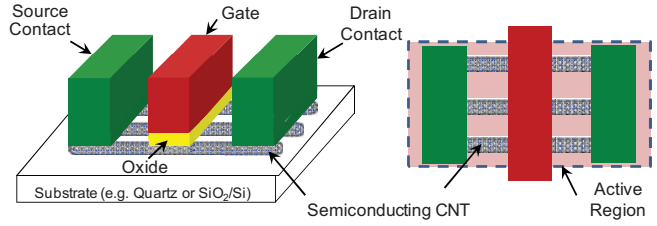

Figure 1.1 Carbon Nanotube Field-Effect Transistor: three dimensional view (left) and top view (right).

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Despite its promising benefits, CNFET technology is expected to have significantly higher variability compared to conventional silicon CMOS. CNFET circuits suffer mainly from the following CNT-specific imperfections: 1. The presence of metallic CNTs (m-CNTs, versus the useful semiconducting or s-CNTs); 2. CNT diameter variations; 3. Mis-positioned CNTs; and 4. CNT density variations. A survey of these CNT-specific imperfections can be found in [Patil 09a, Zhang 10].

All of the above imperfections can directly cause variations in the drive currents of CNFETs, which lead to circuit performance variations. These imperfections can even result in complete failure of CNFETs when there are no s-CNTs between the source and drain. We denote this type of failure by *CNT count failure* (or simply referred to as *failure* in the rest of the paper), and the circuit yield corresponding to this failure mode by *CNT count limited yield*. For VLSI circuits with billions of transistors, CNT count failure can substantially reduce the overall circuit yield.

Fortunately, recent studies [Raychowdhury 09, Zhang 09a, Zhang 09b] have shown an important common feature for all the above CNT-specific imperfections: i.e., $\sigma(I_{on}) / \mu(I_{on})$ exhibits a $1/\sqrt{N}$ dependence with N, where N and I_{on} are the CNT count and on-current in a CNFET, respectively. This effect is commonly known as statistical averaging [Borkar 05]. As a result, variations and failure probability caused by CNT-specific imperfections can be reduced to an acceptable level by utilizing wide CNFETs that contain many CNTs on average. However, as shown in Sec. 2, upsizing CNFETs (i.e., increase the width of a CNFET to include more CNTs in the channel) for yield improvement can be very expensive, especially at highly scaled technology nodes.

In order to reduce or even eliminate the need for upsizing CNFETs, we present a processing/design co-optimization approach to reduce the circuit-level failure probability of CNFET circuits. The key idea is to take advantage of the strong correlation in both CNT count [Zhang 09a] and CNT type (metallic or semiconducting) [Lin 09] that is present in directional CNT growth. However, correlation in CNT growth cannot be taken advantage of in its entirety, unless the CNFETs are laid out in such a way that they share the same CNTs. The full benefits of CNT correlation can be realized by enforcing layout restrictions in the active regions (Sec. 3). Unlike traditional layout restrictions that focus on the strictly-gridded patterns for the gate (poly) layer [Wang 04, Webb 08], this paper presents a scenario where layout restrictions on the active regions are required. The effectiveness of our approach is evaluated using a 45 nm technology library (due to its public availability). Our approach enables a 350X reduction in CNFET failure probability requirements for 45 nm CNFET logic circuits with a constant targeted yield, leading to significantly reduced costs associated with upsizing the CNFETs.

The rest of the paper is organized as follows. Section 2 presents a quantitative model for CNT count limited yield, and discusses the cost of upsizing small-width CNFETs to meet a certain yield goal. Section 3 introduces yield optimization of CNFET circuits by utilizing directional CNT growth and aligned-active layout restriction. Benefits and tradeoffs of this approach are also quantified. Section 4 concludes this paper.

2. Yield of Logic Circuits with Uncorrelated CNFETs

2.1. Model for CNT Count Limited Yield

CNT count failure (defined in Sec. 1) can be caused due to m-CNTs, CNT density variations and mis-positioned CNTs. The effect of mis-positioned CNTs within a CNFET has been found to be very limited [Patil 08], especially when the channel length is small or if directional CNT growth is adopted. Therefore, our model focuses on CNT count failure caused by m-CNTs and CNT density variations.

During CNT growth, assume each CNT has a probability p_m of being metallic and p_s (=1-p_m) being semiconducting. Consider an m-CNT removal process [Patil 09c], where p_{Rm} stands for the conditional probability of a CNT being removed given it is an m-CNT. For practical VLSI circuit applications, p_{Rm} of greater than 99.99% is required [Zhang 09b]. For most of the discussions in this paper, we assume that $p_{Rm} \rightarrow 1$. As a side effect, m-CNT removal processes may also inadvertently remove some fraction of s-CNTs, and the conditional removal probability of an s-CNT is denoted by p_{Rs}. A single CNT can contribute to CNT count failure of a CNFET if it is an m-CNT or if it is an s-CNT but is removed inadvertently. Let p_f stand for this probability, we have

$$p_f = p_m + p_s p_{Rs} \qquad (2.1)$$

Consider a CNFET designed with width W, and has $N = N(W)$ CNTs prior to m-CNT removal. In the presence of CNT density variations, $N(W)$ has a statistical distribution, denoted by Prob{$N(W)$}. [Zhang 09a] presents a model for the probability distribution of $N(W)$ as a function of W, and the mean and standard deviation of inter-CNT pitch (denoted by μ_S and σ_S). We utilize this model and keep the σ_S / μ_S ratio as reported in [Zhang 09a]. However, to enable a predictive analysis, the mean of inter-CNT pitch (μ_S) is assumed to be an optimized value of 4 nm [Deng 07].

Denote by p_F the probability of CNT count failure (or simply failure probability) of a CNFET. Assuming CNT failures are independent of each other, the CNFET fails only if all the $N(W)$ CNTs fail. Applying the law of total probability, we find p_F to be

$$p_F(W) = \sum_{N_i} p_f^{N_i} \text{Prob}\{N(W) = N_i\} \qquad (2.2)$$

Figure 2.1 illustrates the relationship of p_F vs. W for different processing conditions. For each case, p_F decreases exponentially with W, as can be seen from equation (2.2). Therefore, upsizing CNFETs is an effective (but expensive) way to reduce p_F.

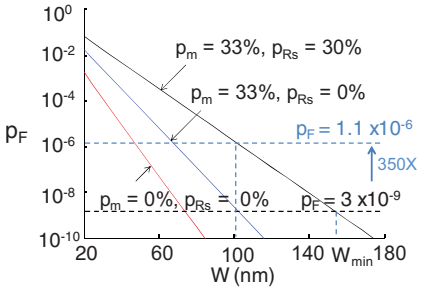

Figure 2.1. CNFET failure probability vs. CNFET width (p_{Rm} = 1).

It is important to note that CNT count failure is not the only failure mode for CNFET circuits. For example, [Zhang 09b] shows that noise margin degradation due to the surviving m-CNTs can cause additional problems. However, noise susceptibility of a logic gate would not necessarily cause a logic failure because the signal may be restored in succeeding CMOS logic stages [Zolotov 02], reducing the chance of a noise problem being turned into yield loss. We therefore focus on CNT count limited yield for the discussion of logic circuits.

2.2. Circuit-Level Yield Model

To evaluate yield at the circuit level, we consider a chip consisting of M transistors (CNFETs) that are independent of each other, with W_i representing the width of the i^{th} CNFET. The circuit-level yield is given by

$$Yield = \prod_{i=1}^{M} [1 - p_F(W_i)] \approx 1 - \sum_{i=1}^{M} p_F(W_i) \qquad (2.3)$$

where $p_F(W_i)$ can be found using (2.2) or equivalently from Fig. 2.1. Because $p_F(W_i)$ is sensitive to CNFET width W_i, most of the yield loss in (2.3) is due to small-width CNFETs. To optimize an existing circuit design to meet a certain yield, a simple strategy is to increase the sizes of the small-width CNFETs according to a *threshold width* (W_t). We further define W_{min} as the minimum possible W_t, such that a chip level yield requirement ($Yield_{desired}$) is met. Formally, W_{min} can be found by solving the following optimization problem

$$W_{\min} = \min(W_t)$$
$$s.t.\ \ Yield = \prod_{i=1}^{M} \{1 - p_F[U_{Wt}(W_i)]\} \geq Yield_{desired} \qquad (2.4)$$

where $U_{Wt}(W_i) = \max(W_i, W_t)$ is an "upsizing" function. Finding the exact optimal solution to (2.4) can be tedious, but the problem can be substantially simplified by neglecting the yield loss in (2.3) due to non-minimum-sized transistors. That is, if there are M_{min} transistors with minimum size (W_t), then problem (2.4) can be re-written as

$$W_{\min} = \min(W_t)$$
$$s.t.\ \ \prod_{i=1}^{M_{\min}} [1 - p_F(W_t)] \approx 1 - M_{\min} p_F(W_t) \geq Yield_{desired} \qquad (2.5)$$

The procedure for finding W_{min} according to (2.5) is straightforward: take a device-level p_F vs. W curve such as Fig. 2.1, draw a horizontal line corresponding to (1-$Yield_{desired}$) / M_{min} and the x-coordinate of the intersection gives W_{min}. Although estimating M_{min} for (2.5) can be iterative in nature, it is simple in practice especially for discrete sizing schemes adopted in standard cell based designs.

As a case study, we consider a transistor sizing distribution (shown in Fig. 2.2a) extracted from an OpenRISC processor design (cache not included) [OpenCores 09] synthesized with the Nangate 45nm Open Cell Library [Nangate 09] (slightly modified for CNFET technology, see [Bobba 09]) using Synopsys Design Compiler. M_{min} can be estimated to contain the two left-most bins in Fig. 2.2a, which gives 33% of the total number of transistors M. If M = 100 million and the desired circuit yield is 90%, the W_{min} in this example is about 155 nm (illustrated in Fig. 2.1). This result verifies the initial choice of M_{min} for containing only the first two bins.

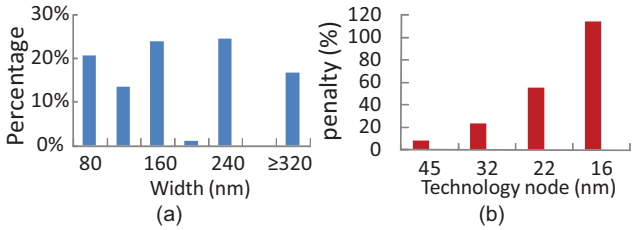

Figure 2.2. Case study: (a) Transistor width distribution of an OpenRISC core synthesized using Nangate 45nm Cell Library (b) Gate capacitance increase (penalty) vs. technology node associated with upsizing the small transistors to W_{min}. The case with full correlation is discussed in Sec. 3.

Next, we discuss area and power penalties associated with upsizing small-width CNFETs. For standard cell-based designs, there is little area penalty for up-sizing the smallest cells, since there is enough free space available as the distance between the rails is fixed. Power penalty (both static and dynamic), on the other hand, is roughly proportional to the total transistor width increase. Figure 2.2b shows this penalty (%) as measured by the percentage increase of total gate capacitance from upsizing the circuit. A scaling analysis is also performed for different technology nodes beyond 45 nm by

assuming that the CNFET width distribution scales linearly with technology node, while the inter-CNT pitch (μ_S) remains constant at 4 nm. Note that, the amount of penalty is expected to increase significantly as technology scales down.

3. CNFET Logic Circuit Yield Optimization

3.1. CNFET Correlation for Yield Optimization

The circuit-level yield (and therefore W_{min}) calculation in Sec. 2 is based on the assumption that failure probabilities (p_F) of all CNFETs are independent of each other. This assumption is close to reality if the CNFET circuit is fabricated using a growth that produces uncorrelated CNTs (e.g., Fig. 3.1a). However, if directional CNT growth (Fig. 3.1b) is used, this assumption is overly pessimistic. If two CNFETs have the same size and are aligned in the CNT direction (Fig. 3.1c), large correlation can be observed in both CNT count ([Zhang 09a]) and CNT type (i.e., metallic or semiconducting [Lin 09]) of the CNTs contained in the two CNFETs. To simplify the analysis, we assume that all CNTs have a fixed length L_{CNT}, and perfect correlation can be achieved within the CNT length, and complete uncorrelation for CNFETs spaced beyond L_{CNT}. Impact of CNT length variations will be discussed in a more detailed version of this work.

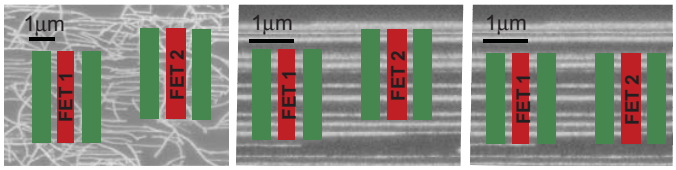

Figure 3.1. (a) Non-aligned layout style on uncorrelated CNT growth (b) Non-aligned layout style on directional CNT growth and (c) Aligned-active layout style on directional CNT growth.

To find a less pessimistic value of W_{min} for directional CNT growth, we assume that the whole circuit (composed of M_{min} small-width CNFETs, as defined in Sec. 2.2) is distributed in K_R rows. CNFETs taken from different rows do not share common CNTs and are therefore independent with each other. The yield expression of (2.3) can be re-written as

$$Yield = \prod_{i=1}^{K_R}(1-p_{RF_i}) \approx 1-\sum_{i=1}^{K_R} p_{RF_i} = 1-K_R p_{RF} \quad (3.1)$$

where p_{RFi} is the failure probability of row i, and p_{RF} is the chip-level average value of the p_{RFi}'s.

Calculating p_{RF} in a general case (allowing arbitrary positioning of the CNFETs) requires numerical methods. However, we realize that the minimum value for p_{RF} is achieved in the special case where all the minimum-sized CNFET active regions are strictly aligned to each other (as shown in Fig. 3.1c). This layout style is defined as *aligned-active* layout. Because all the CNT counts and types are correlated in this case, the probability of having a failing row is the same as the probability of having one failing CNFET in this row, i.e., $p_{RF} = p_F$. Comparing it with the fully independent case (2.4), the circuit failure probability (i.e., *1–Yield*) is reduced by M_{min} / K_R times. This ratio of M_{min} / K_R represents the average number of minimum-sized CNFETs in a row, which we denote by M^R_{min}. M^R_{min} is largely determined by L_{CNT} and the average pitch between the small-width CNFETs (denoted by $P_{min\text{-}CNFET}$):

$$M^R_{\min} = L_{CNT} / P_{\min-CNFET} \quad (3.2)$$

Hence, CNT growth with large L_{CNT} or designs with small $P_{min\text{-}CNFET}$ are both beneficial to the yield improvement. With the improved yield expression (3.1), the requirement that determines W_{min} in (2.5) can be relaxed by the exact same amount as the reduction in p_{RF}. A much lower W_{min} can therefore be expected.

3.2. Enforcing Aligned-Active CNFET Standard Cells

For standard cell-based CNFET designs, the aligned-active layout style requires the active regions not only within each individual cell, but also between different cells to be aligned to each other. More specifically, the aligned-active restriction can be applied to an existing standard cell library by the following heuristic:

1. Estimate W_{min} according to equations (2.5) and (3.1).
2. Find active regions corresponding to all the CNFETs with width ≤ W_{min} and perform upsizing. These active regions are called *critical active regions*.
3. Place the n-type (same for p-type) critical active regions of all cells in the cell library in such a way that their y-coordinates match with each other.
4. Modify the intra-cell routing as necessary.

Note that, although non-critical active regions have not been explicitly mentioned in the above heuristics, it is still beneficial to align them with the critical active regions as much as possible.

The standard cells in the Nangate Open Cell Library were modified according to the aforementioned procedure for the enforcement of aligned-active restriction. Figure 3.2 illustrates one of the standard cells (AOI222_X1) before (a) and after (b) enforcing this restriction. The critical n-type active regions in this cell are highlighted in dashed yellow lines. After the modification, all the n-type active regions in the cell are aligned according to a globally defined grid. The cell width has increased by ~9% as a result of this change. This effect of possible cell widening and area increase resulting from enforcing the aligned-active restrictions is discussed in Sec. 3.3.

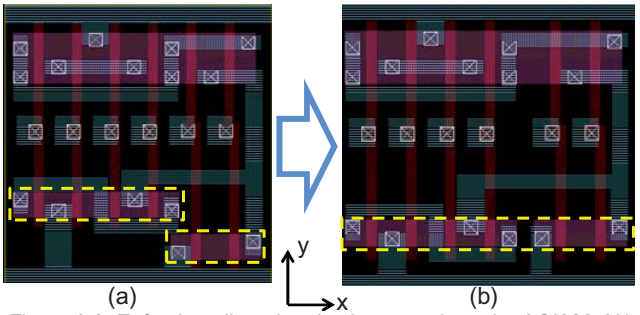

Figure 3.2. Enforcing aligned-active layout style to the AOI222_X1 cell from the Nangate 45nm Open Cell Library.

3.3. Yield Optimization Results and Discussions

To quantify the benefits of the yield optimization, we continue to use the example from the OpenRISC design synthesized with the Nangate 45nm Open Cell Library after enforcing the aligned-active restrictions. The average pitch $P_{min\text{-}CNFET}$ in this design is found to be 1.8 FETs/µm, while L_{CNT} is taken to be 200 µm long [Kang 07, Patil 09b]. Table 1 compares the p_{RF} values calculated for this design with (1) completely non-directional CNT growth, (2) directional CNT growth but the unmodified cell library, and (3) directional CNT growth and the modified cell library enforcing the aligned-active layout style. As seen from the table, the total reduction in p_{RF} resulted from combined directional CNT growth and aligned-active layout style is about 350X, of which 26.5X is due to the aligned-CNT growth, and the other 13X coming from the enforcement of aligned-active layout style.

Table 1. Benefits from directional CNT growth and aligned-active layout style.

	Uncorrelated CNT growth	Directional growth No aligned-active	Directional growth Aligned-active
p_{RF}	$5.3\text{x}10^{-6}$	$2.0\text{x}10^{-7}$	$1.5\text{x}10^{-8}$

The W_{min} after the optimization can be found by relaxing the required p_F by 350X (as shown in Fig. 2.1), which gives W_{min} = 103 nm at 45 nm technology node. As shown in Fig. 3.3, the penalty associated with upsizing the CNFETs is almost completely eliminated

with this optimized value of W_{min}. For technology nodes beyond 45 nm, significantly reduced upsizing penalty can be observed as compared to the case before any optimization (replicated from Fig. 2.2b).

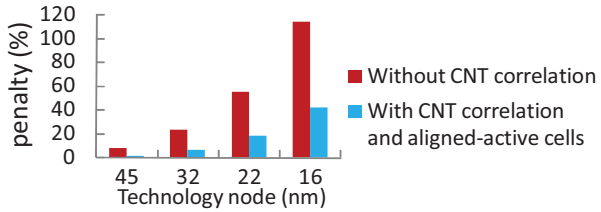

Figure 3.3 Gate capacitance increase (penalty) vs. technology node before and after enforcing directional CNT growth with aligned-active standard cells.

We now discuss the area costs of strictly aligning the active regions of the critical transistors ($W < W_{min}$) in the standard cell library. Altering the positions of active regions in the critical cells will have an impact on the intra-cell as well as inter-cell routing. However, in order to minimize the penalty on inter-cell routing, we retained the location of the I/O pins as much as possible while modifying the cells.

Aligning to the optimal grid has an area impact on 4 cells (out of a total of 134 cells) from the Nangate Open Cell Library, including the AOI222_X1 cell shown in Fig. 3.2.

We have further extended our analysis to a commercial 65 nm standard cell library, having 775 cells. About 20% of the library cells have an impact on area while aligning the active regions. Overall we observe that aligning active regions becomes complex for gates with high fan-in as well as flip-flops and latches, thereby leading to area penalty. However, the area penalty can be reduced to zero by having two aligned active regions for both p-type and n-type CNFETs instead of one. This will result in a 2X reduction in the p_{RF} benefit described in Sec. 3.1 (corresponding to < 5% increase in W_{min}).

Table 2. Area penalty on standard cell libraries for enforcing aligned-active layout style.

	65nm commercial library		45nm Nangate Open Cell Library
	one aligned active region	two aligned active regions	
# std. cells	775	775	134
Cells with area penalty	~ 20%	0	3%
Min penalty	10%	0%	4%
Max penalty	70%	0%	14%
W_{min} (nm)	107	112	103

4. Conclusion

CNFETs with small widths are vulnerable to failures due to CNT-specific imperfections such as CNT density (count) variations and metallic CNTs. Upsizing these vulnerable small CNFETs is an effective but costly option. Large degree of spatial correlation observed in directional CNT growth provides a unique opportunity to enable significant yield improvement. To take full advantage of the potential benefits of directional CNT growth, this paper introduces the aligned-active layout restrictions – an approach that engineers the correlations among CNFETs in a useful way. This process/design co-optimization approach relaxes the device-level failure probability requirement by 350X at the 45 nm technology node given a target chip-level yield, leading to significantly reduced costs associated with upsizing the small-width CNFETs.

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References

[Avouris 07] Avouris, P., Z. Chen, V. Perebeinos "Carbon-based electronics", *Nature Nanotechnology*, pp. 605-615, 2007.

[Bobba 09] Bobba, S. *et al.,* "Design of Compact Imperfection-Immune CNFET Layouts for Standard-Cell-Based Logic Synthesis", *Proc. DATE*, pp. 616-621, 2009.

[Borkar 05] Borkar, S., *et al.,* "Statistical circuit design with carbon nanotubes", U.S. Patent Application 20070155065, 2005.

[Deng 07] Deng, J., *et al.*, "Carbon Nanotube Transistor Circuits: Circuit-Level Performance Benchmarking and Design Options for Living with Imperfections", *Proc. ISSCC*, pp. 70-588, 2007.

[Kang 07] Kang, S. J., *et al.,* "High-Performance Electronics Using Dense, Perfectly Aligned Arrays of Single-Walled Carbon Nanotubes", *Nature Nanotechnology*, vol. 2, pp. 230-236, 2007.

[Lin 09] Lin, A., *et al.*, "ACCNT: A Metallic-CNT-Tolerant Design Methodology for Carbon-Nanotube VLSI: Concepts and Experimental Demonstration," *IEEE Trans. Elec. Dev.*, vol 56, pp. 2969-2978, 2009.

[Nangate 09] http://www.nangate.com.

[OpenCores 09] http://www.opencores.org.

[Patil 08] Patil, N., *et al.*, "Design Methods for Misaligned and Mis-positioned Carbon-Nanotube-Immune Circuits", *IEEE Trans. CAD*, pp. 1725-1736, 2008.

[Patil 09a] Patil, N., *et al.,* "Digital VLSI Logic Technology using Carbon Nanotube FETs: Frequently Asked Questions", *Proc. DAC*, pp. 304-309, 2009.

[Patil 09b] Patil, N., *et al.,* "Wafer-Scale Growth and Transfer of Aligned Single-Walled Carbon Nanotubes", *IEEE Trans. Nanotechnology*, vol. 8, pp. 498-504, 2009.

[Patil 09c] Patil, N., et al., "VMR: VLSI-Compatible Metallic Carbon Nanotube Removal for Imperfection-Immune Cascaded Multi-Stage Digital Logic Circuits using Carbon Nanotube FETs", *Proc. IEDM*, pp. 573-576, 2009.

[Raychowdhury 09] Raychowdhury, A., *et al.*, "Variation Tolerance in a Multichannel Carbon-Nanotube Transistor for High-Speed Digital Circuits", *IEEE Trans. Elec. Dev.*, vol. 56, pp. 383-392, 2009.

[Wang 04] Wang, J., A. Wong and E. Lam, "Performance Optimization for Gridded-layout Standard Cells", *Proc. SPIE*, pp. 107-117, 2004.

[Webb 08] Webb, C., "45nm Design for Manufacturing", *Intel Technology Journal*, Vol. 12, Issue 02, pp. 121-130, 2008.

[Wei 09] Wei, L., *et al.*, "A Non-iterative Compact Model for Carbon Nanotube FETs Incorporating Source Exhaustion Effects," *Proc. IEDM*, pp. 577-580, 2009.

[Zhang 09a] Zhang, J., *et al.*, "Carbon nanotube circuits in the presence of carbon nanotube density variations", *Proc. DAC*, pp. 71-76, 2009.

[Zhang 09b] Zhang, J., N. Patil, and S. Mitra, "Probabilistic Analysis and Design of Metallic-Carbon-Nanotube-Tolerant Digital Logic Circuits", *IEEE Trans. CAD*, pp. 1307 – 1320, 2009.

[Zhang 10] Zhang, J., *et. al.*, "Carbon Nanotube Circuits: Living with Imperfections and Variations," *Proc. DATE*, pp. 1159-1164, 2010.

[Zolotov 02] Zolotov, V., *et al.,* "Noise Propagation and Failure Criteria for VLSI Designs", *Proc. ICCAD*, pp. 587-594, 2002.