Fabrication of Memristors with Poly-Crystalline Silicon Nanowires

M. Haykel Ben Jamaa*[1], *Student Member, IEEE,* Sandro Carrara*[1], *Member, IEEE,* Julius Georgiou[2], *Senior Member, IEEE,*
Nikolaos Archontas[3], and Giovanni De Micheli[1], *Fellow, IEEE*

[1] EPFL (Swiss Federal Institute of Technology), 1015 Lausanne, Switzerland
[2] University of Cyprus, 1678 Nicosia, Cyprus
[3] Democritus University of Thrace, Greece

Abstract- **Memristors are the two-terminal components that complete the symmetry between the fundamental circuit variables, and they are highly suitable for bioinspired and neural-network-based computational systems due to their inherent memory effect. In this paper we present a fabrication technique that uses only Complementary Metal Oxide Semiconductor (CMOS) processing steps and conventional photolithography, yielding poly-crystalline silicon nanowires that show a memristive behavior. Besides measurements, we performed numerical device simulations that address the observed memristive effect.**

Keywords- silicon nanowire, SiNWFET, spacer technique, polycrystalline silicon, poly-Si, ambipolar, memristor, hysterisis, charge trapping

I. INTRODUCTION

The existence of a new two-terminal circuit element called *memristor* (*mem*ory-resi*stor*) has been envisaged by Leon O. Chua [1] in order to complete the symmetry of the equation system describing the relationships between the four fundamental circuit variables: current i, voltage v, charge q and magnetic flux φ:

$$R = \frac{dv}{di}; C = \frac{dq}{dv}; L = \frac{d\varphi}{di}; M = \frac{d\varphi}{dq}. \qquad (1)$$

The fourth equation defines a new relationship between charge q and magnetic flux φ described by the memristance M. The memristor is reduced to a resistance if it is constant, i.e. if M does not depend on q; but it leads to a hysteretic behavior of the i–v curve if it depends on q.

The significance of memristors arises from their natural existence in biological computational systems. For instance, ion diffusion is responsible of the time-dependant conductance of the neuron membrane in the Hodgkin-Huxley model [2], which is therefore modeled as a memristive device. Learning mechanisms are also explained using the memristive model of synapses [3] and they were demonstrated with single devices

[4]. Self-programming circuits were demonstrated by embedding memrsitors into logic circuits [5].

The memristor effect, seen as the hysteretic behavior of the i–v curve, may be obtained by using a circuitry that includes active elements and an internal power source [1, 6]. However, this solution is just an emulation of memristors and it consumes valuable chip area and power. With the scaling of device dimensions, new phenomena have been claimed to be responsible for the memristor behavior in monolithic devices. For instance, it has been demonstrated that a memristor effect arises naturally in nanoscale systems in which solid-state electronic and ionic transport are coupled under an external bias voltage [7]. Voltage driven memristor effects were demonstrated as well in Pt/organic/Ti [8], in PEO/PANI polymeric [4] and in amorphous Silicon [9] devices.

In this paper, we report the fabrication of poly-crystalline Silicon nanowires (poly-SiNW) with a process that is compatible with Complementary Metal Oxide Semiconductor (CMOS) technology and exclusively with photolithography steps. We demonstrate a hysteretic behavior in the measured characteristics of the poly-SiNW field effect transistors (poly-SiNW FET). The behavior is reminiscent to a memristor effect that we explain by the bias dependency of the interface states in the device channel. Device simulations are confirming the assumed hypothesis.

II. DEVICE FABRICATION

The spacer technique is used in order to define sub-photolithographic dimensions by using standard photo-lithography and CMOS steps [10]. The process flow is illustrated in Fig. 1. We started by defining a SiO_2 sacrificial layer on a Si substrate (p-doped, 0.1-0.5 Ω·cm). Then, we deposited a thin conformal layer of poly-crystalline Si (poly-Si) with a thickness ranging from 40 to 90 nm. Poly-Si was obtained by Low Pressure Chemical-Vapour-Deposition (LPCVD) of SiH_4 at 600°C. Next, we etched this layer with a Reactive Ion Etchant (RIE), in order to remove the horizontal layer while keeping the sidewall as a spacer; and we densified the poly-Si spacer at 700°C for 45 minutes. Then we defined a second Low Temperature Oxide (LTO) spacer next to the poly-Si in a similar way in order to isolate the first poly-Si spacer.

The LTO was deposited from the reaction SiH$_4$ with O$_2$ at 425°C. We densified this LTO spacer for 45 minutes in N$_2$ flow at 700°C. The spacers are reminiscent of nanowires with thicknesses ranging between 20 and 60 nm. The contact regions of the undoped poly-Si nanowire (poly-SiNW) were defined by the electron-beam evaporation of 10 nm Cr and 50 nm nichrome (Ni$_{0.8}$Cr$_{0.2}$) and lift-off. The Cr enhances the adhesion and thermal stability of Ni to oxidation during the following 2-step annealing process (5 minutes at 200°C, followed by 5 minutes at 400°C). The substrate was used as a back-gate with a thick dry oxide as insulator (400 nm).

A perspective *scanning electron microscopy (SEM)* of a single poly-SiNW defined on a SiO$_2$ sacrificial layer is shown in Fig. 2. A cross-sectional SEM of a similar structure is shown in Fig. 3.
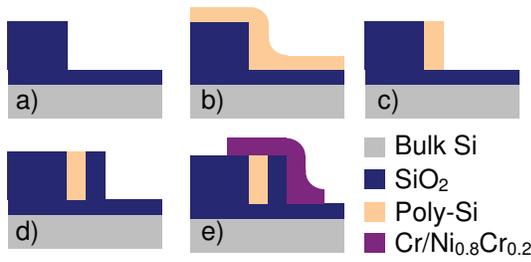

Fig. 1: Poly-SiNW FET fabrication steps: a) sacrificial layer etch, b) poly-Si deposition, c) RIE etch, d) LTO spacer definition, e) metallization
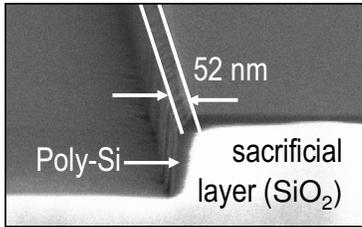

Fig. 2: Perspective SEM of a 52 nm wide poly-SiNW defined as a spacer on a SiO$_2$ sacrificial layer
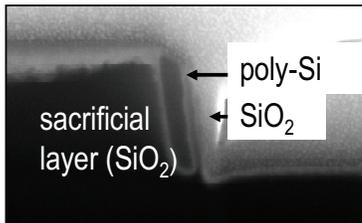

Fig. 3: Cross-sectional SEM of a poly-SiNW defined as a spacer on a SiO$_2$ sacrificial layer

III. NUMERICAL SIMULATIONS

To analyse the electrical characteristics of poly-Si Nanowires, 2-D numerical simulations are performed using available tools [11]. The behavior of poly-Si Nanowires is strongly influenced by trapped charges, which contribute to the total space charge. They affect the generation-recombination rate. In our model, we assume traps to be uniformly distributed over the entire volume of the poly-Si film. The electrical characteristics of the poly-Si Nanowire are investigated by considering the density of states. The total density of states, g(E), was modeled by a sum of exponential terms [11]:

$$g(E) = g_{TA}(E) + g_{TD}(E) + g_{GA}(E) + g_{GD}(E) \quad (2)$$

where

$$
\begin{cases}
g_{TA}(E) = N_{TA} \exp\dfrac{E - E_C}{W_{TA}}; & g_{TD}(E) = N_{TD} \exp\dfrac{E_V - E}{W_{TD}} \\[2mm]
g_{GA}(E) = N_{GA} \exp\left[-\left[\dfrac{E_{GA} - E}{W_{GA}}\right]^2\right]; & g_{GD}(E) = N_{GD} \exp\left[-\left[\dfrac{E - E_{GD}}{W_{GD}}\right]^2\right]
\end{cases} \quad (3)
$$

With T, G, A and D stand for tail, Gaussian (deep level), acceptor and donor states, respectively. E is the trap energy; E_C and E_V are the conduction and valence band energies. These equations also include the total states density (N_{GA} and N_{GD}), its decay energies (W_{GA} and W_{GD}), and its peak energy/peak distributions (E_{GA} and E_{GD}). The energy gap of the poly-Si that best fit the experimental data was 1.35 eV and a fixed negative trapped charge at the interface poly-Si/SiO$_2$ was included in the model.

IV. RESULTS

We characterized undoped single poly-SiNWs (width W_{NW} ~67 nm) with Cr/nichrome D/S contacts and the substrate used as a 20-μm long back gate with a thick SiO$_2$ gate oxide (0.4 μm). The I_{ds}-V_{gs} curve shows an ambipolar behaviour, *i.e.*, a current conductance under either high positive or negative gate voltage (Fig. 4), with a more dominant hole conduction under high negative gate voltage. The I_{on}/I_{off} ratio was $1.8 \cdot 10^4$ and $3.8 \cdot 10^3$ for p- and n-branches respectively. The ambipolar behaviour is explained in Fig. 5. The I_{ds}-V_{gs} curve in Fig. 4 showed a hysteretic behaviour. By enlarging the V_{gs} sweep range from [-10V,10V] to [-40V,40V], the hysteresis became larger.

The simulations have qualitatively confirmed that charge trapping and detrapping explains the hysteresis in Fig. 4. From (1) to (2), trapped holes at the SiO$_2$/poly-Si interface create positive fixed charges, and are detrapped with increasing V$_{gs}$. From (2) to (3), an electron channel is created. With the increasing electron density, more electrons are trapped at the SiO$_2$/poly-Si interface, leading to a negative interface charge density. From (3) to (4), electrons are detrapped with the vanishing electron channel. Detrapping is a slower process than trapping, explaining the hysteresis (2)-(3)-(4). From (4) to (1), a hole channel is created and increases the trapping

Fig. 4: Variation of hysteresis width of I_{ds}-V_{gs} and I_{on}/I_{off} with V_{gs} range (back-gated devices) at V_{ds}=3.1V

Fig. 5: Band diagram explaining ambipolarity of poly-SiNW: high positive (negative) V_{gs} makes Schottky barrier thinner for electrons (holes)

probability for holes. This is a faster process than detrapping holes; explaining again the hysteresis (4)-(1)-(2). The off-current at (2) is lower than the one at (4) because of the additional probability of having electrons trapped in SiO_2 besides the electrons trapped at the SiO_2/poly-Si interface.

By enlarging the sweep range (higher V_{gs}), more charge carriers are trapped. This shifts the threshold voltage in the n-branch (p-branch) to more positive (negative) values during the trapping phase. The detrapping is slow, thus all 3 curves almost coincide during the detrapping phases.

CONCLUSIONS

In this paper, we have presented the fabrication of memristors based on poly-crystalline silicon nanowires. Experimental results showed an ambipolar hysteretic behavior of the realized structures. The hysteresis became larger by enlarging the voltage sweep range. Numerical simulations confirmed that the hysteretic effect is due to charge trapping at the interface states between the channel and the gate oxide.

REFERENCES

[1] L. O. Chua, "Memristor-The missing circuit element," Sch. Elec. Eng., Purdue Univ., Lafayette, Ind.; Tech. Rep. TR-EE (1970) 70-39

[2] A. L. Hodgkin and A. F. Huxley: "A quantitative description of membrane current and its applications to conduction in the nerve," J. Physiol., 1 (1952) 500-544

[3] B. Linares-Barranco and T. Serrano-Gotarredona, "Memristance can explain spike-time-dependent-plasticity in neural synapses," Nature Proc., 2009, 1-4

[4] A. Smerieri, T. Berzina, V. Erokhin and M. P. Fontana, "A functional polymeric material based on hybrid electrochemically controlled junctions," Materials Science and Engineering C 28 (2008) 18–22

[5] J. Borghetti et al., "A hybrid nanomemristor/transistor logic circuit capable of self-programming," PNAS, 106 (2), 2009, 1699-1703

[6] C. Toumazou, J.Georgiou and E. M. Drakakis, " Current-mode analogue circuit representation of the Hodgkin and Huxley neuron equations," IEEE Electronic Letters, 34 (1998) 376-1377

[7] D. B. Strukov, G. S. Snider1, D. R. Stewart1 and R. S. Williams, "The missing memristor found," Nature, 453 (2008), 80-83.

[8] Stewart, D. R. et al., "Molecule-independent electrical switching in Pt/organic monolayer/Ti devices," Nano Lett. 4 (2004) 133–136

[9] S. H. Jo, K.-H. Kim and W. Lu, "High-density crossbar arrays based on a Si memristive system," Nano Lett., 9 (2009), 870-874

[10] G. Cerofolini, "Realistic limits to computation II. The technological side," Appl. Phys. A, 86 (2007) 31-42

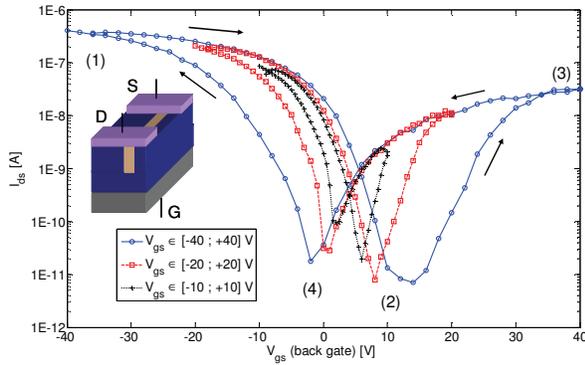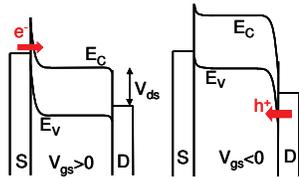[11] Atlas Users Manual, SiIvaco Inc., Santa Clara, CA, 2003