Available online at www.sciencedirect.com
ScienceDirect
Microelectronic Engineering 85 (2008) 1406–1409
MICROELECTRONIC ENGINEERING
www.elsevier.com/locate/mee

Prospects for logic-on-a-wire

K.E. Moselund *, D. Bouvet, M.H. Ben Jamaa, D. Atienza, Y. Leblebici, G. De Micheli, A.M. Ionescu

Ecole Polytechnique Fédérale de Lausanne, EPFL, Switzerland

Received 3 October 2007; received in revised form 14 January 2008; accepted 15 January 2008
Available online 20 January 2008

Abstract

In this paper we present the top-down fabrication of gate-all-around (GAA) and body-tied Ω-gate devices by a combination of etching and oxidation steps resulting in a local silicon-on-insulator structure. The GAA has advantages in terms of enhanced current drive, whereas the body-strapped structures allow for active leakage control and in some cases impact ionization devices. We demonstrate an inverter fabricated along a single silicon rib. The inverter consists of two enhancement mode body-strapped Ω-gate NMOS transistors. Static and dynamic experiments demonstrate a fully functional inverter with the output experiencing $V_{DD}/2$ voltage swing, as expected for an NMOS inverter with identical driver and load dimensions. In addition, we propose the use of these devices for cross-bar memory addressing.

Keywords: Top-down silicon nanowire; Omega-gate MOSFET; Inverter-on-wire

1. Introduction

Recently there has been a widespread interest in silicon nanowires (Si NW) for the next generation of electronic devices [1]. The thin wires allow for 1D transport and in addition nanowire devices are expected to offer an increase in the density of logic functions. Generally, two different options are explored; (i) Bottom-up approach, such as in [1–3], in which the wires are grown or self-assembled onto the substrate, this has advantages in terms of scalability and integration density, and in addition in-situ doping of wires is possible during chemical vapour deposition (CVD) growth [4]. However, contacting and alignment is problematic, since the location of the wires on the die is generally not determined by a predefined mask set. (ii) Top-down is the approach considered in this article, in this case the wires are defined by "classical" microelectronic lithographic processing and thus contacting and alignment is not particularly challenging [5,6]. Nanoscaling is done by smart processing, in our case a series of sacrificial oxidation and etching steps.

In this work we have fabricated two types of devices; Ω-gate and gate-all-around (GAA) structures, shown in Fig. 1a and b, respectively, which each present their specific advantages and both allow for a better control of short-channel effects, and thus increased scalability.

The body-strap in the Ω-gate MOSFET allows for active leakage control, and it is also required for the demonstration of punch-through impact ionization MOSFETs, which we presented in [7]. On the other hand, the oxidation causes bending in completely liberated (GAA) structures, which induces tensile strain and leads to an important performance improvement, see [8] for details.

Previously, we have successfully demonstrated the fabrication of individual devices. However, in order for any technology to be viable, it should also demonstrate the capability of incorporating devices into large scale electronic circuits. In [9] a Si NW CMOS inverter is demonstrated, but with devices on separate wires. The present work focuses on the demonstration of an NMOS inverter,

* Corresponding author. Tel.: +41 21 693 5660; fax: +41 21 693 3640.
E-mail address: kirsten.moselund@epfl.ch (K.E. Moselund).

0167-9317/$ - see front matter © 2008 Elsevier B.V. All rights reserved.
doi:10.1016/j.mee.2008.01.022

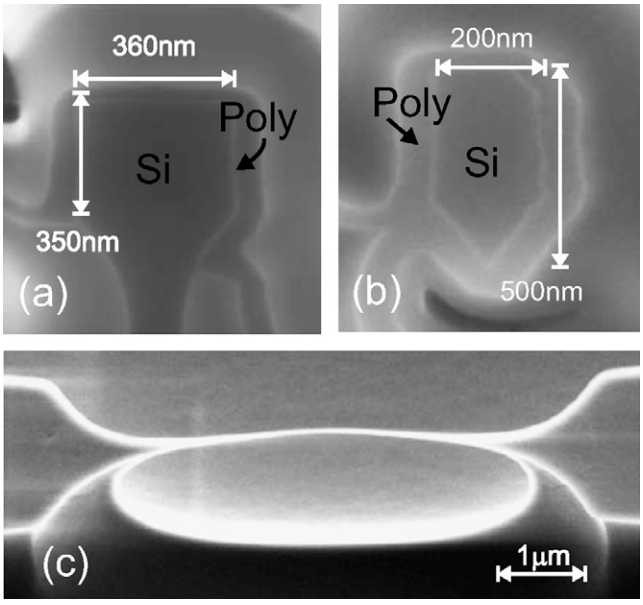

Fig. 1. FIB-SEM image of the cross-section of (a) the Ω-MOSFET in the inverter. (b) A GAA device on the same wafer. (c) SEM image of a liberated bended wire after oxidation and oxide removal.

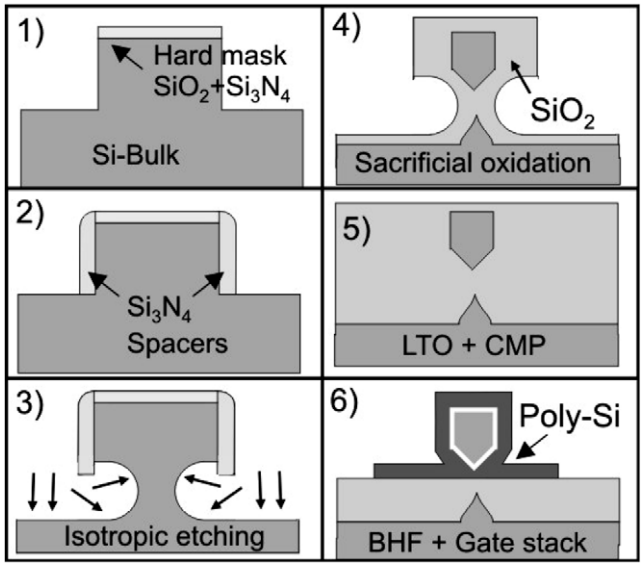

Fig. 2. Schematic showing a cross-section through the wire for a simplified process flow. The steps are. (1) Anisotropic etching of a silicon rib. (2) Spacer formation. (3) Isotropic etching to form the wire structure. (4) Sacrificial oxidation. (5) Isolation and CMP. (6) Partial oxide etch followed by gate stack formation, patterning and self-aligned implantation. Not shown are standard isolation and metallization steps.

by the integration of two body-strapped Ω-gate MOSFETs on the same nanowire. An inverter is one of the most basic building blocks of electronic circuits, thus it is the first step towards "logic-on-a-wire".

2. Top-down si-wire fabrication

This section describes the process flow for the fabrication of both GAA and Ω-gate devices. Whether one or the other is obtained depends on the design width of the rib in step 1, thus on the same wafer we generally have both types of devices. We use a top-down lithographic approach (0.8 μm resolution) according to the process flow depicted in Fig. 2.

This figure shows a process flow resulting in a pentagonal cross-section, but by varying the duration of the anisotropic etch (step 1) and the isotropic etch (step 3) a triangular cross section can be obtained. A rib is etched in silicon, followed by a spacer formation, isotropic etching (step 3) and a sacrificial oxidation (step 4). Depending on the duration of these two steps and the design width, the wires can either be connected to the substrate by a body-tied pillar, Fig. 1a, or completely suspended, Fig. 1b. In the latter case an out-of-plane bending of the wires is observed, which is an indication of tensile stress (see Fig. 1c).

A local SOI structure is created by deposition of a low temperature oxide (LTO), followed by planarization by chemical mechanical polishing (CMP) and partial etching. A gate stack consisting of 10nm thermal oxide and poly-silicon (100–500 nm) is created. The gate lithography uses a fairly thick positive resist (2 μm) which after exposure and development is etched 10 min in oxygen plasma. This is required to remove unexposed resist underneath the silicon wire, which could otherwise lead to a shorting of the two gates. The poly-silicon gate is etched isotropically, in order to completely separate the two 3D devices.

A self-aligned implantation of gate, source and drain is carried out (arsenic, $5 \times 10^{15}\,\mathrm{cm}^{-2}$, 40 keV), followed by annealing at 950 °C for 10 min. Because of the 3D geometry of the device along with the low diffusivity of arsenic, a part of the gate on the lower concave part of the sidewalls is practically un-doped. This results in some high I_{off}. The leakage can be controlled by the substrate bias on Ω-gate devices, see Fig. 3. Recently we have reduced leakage in

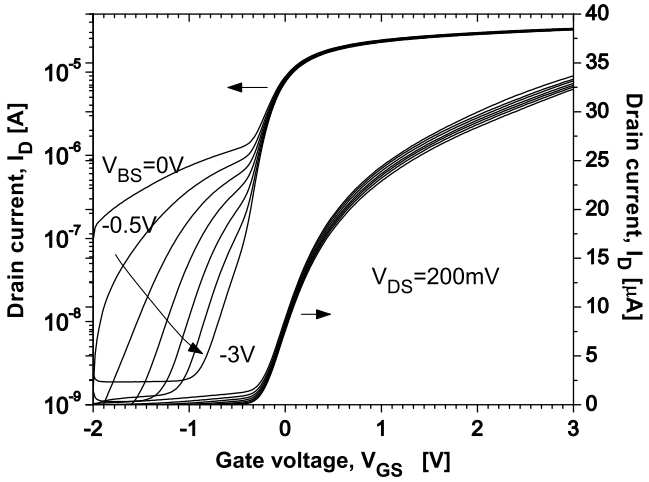

Fig. 3. $I_D(V_{GS})$ for an Ω-gate device, showing that the uneven gate doping is at the origin of the large I_{off}. This can be reduced by applying a negative substrate bias. $L_{eff} = 4.2$ μm, $W_{eff} = 1.6$ μm.

both Ω-gate and GAA devices by increasing the poly-thickness and doing a dual doping step; $POCl_3$ diffusion before gate patterning, followed by self-aligned implantation. Nano-scaled gate lengths can be achieved by advanced lithography, such as DUV or e-beam.

3. Electrical characterization

The $I_D(V_{GS})$ characteristics of a typical Ω-MOSFET is shown in Fig. 3. The I_{on} is on the order of 100 μA/μm for $V_{GS} = V_{DS} = 2$ V ($L_{eff} = 1.5$ μm). The gate leakage is negligible, but the device has a high I_{off} around 2.3 μA/μm without body bias, because of the uneven Ω-gate doping, as mentioned before. This can be reduced by around two orders of magnitude by applying a negative substrate bias of –3 V (see Fig. 3).

Fig. 4 shows the normalized $I_D(V_{DS})$ for a bended GAA MOSFET and a body-tied tri-gate. The effective current drive of the GAA is much larger than the body-tied device for a given bias condition, which translates into a magnified mobility of about 100% increase. This is due to existing tensile strain in our fabricated suspended structures introduced by oxidation, which significantly improves the electron mobility; the amount of strain was measured to 1–3 GPa in [8].

The $I_D(V_{GS})$ and $g_m(V_{GS})$ for the Ω-MOSFETs constituting the inverter are shown in Fig. 5. These show high low-field mobility of ~500 cm^2/Vs, which is also consistent with previously observed results. The inverter devices suffer from a somewhat larger contact resistance than that found for previous devices, since the contacting on top of the gate, without short-circuiting the channel, is rather difficult. Which is why the characteristics are not as good as those previously measured on individual devices.

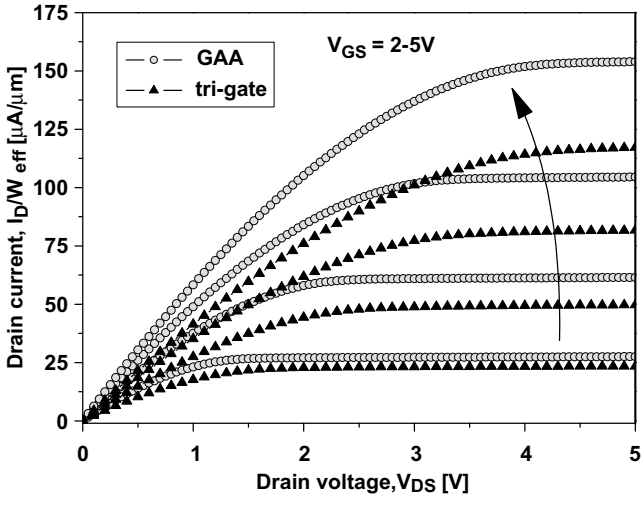

Fig. 4. $I_D(V_{DS})$ curves normalized per effective width for a GAA device, $W_{eff} = 620$ nm and a tri-gate device, $W_{eff} = 1.2$ μm, $V_{GS} = 1$–5 V, $L = 10$ μm. The threshold voltage difference (ΔV_T ~tens of mV) is negligible compared to the value of V_{GS}.

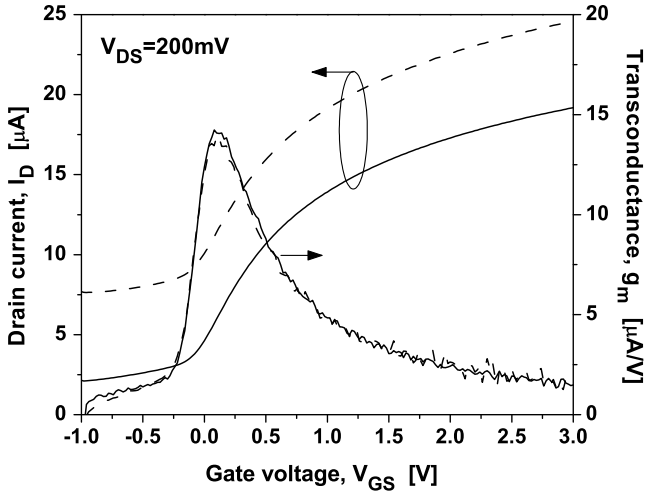

Fig. 5. Individual $I_D(V_{GS})$ curves for the two NMOS transistors constituting the inverter. The large I_{off} is due to in complete gate doping and hence a part of the channel is not controlled, $L_{eff} = 1.5$ μm and $W_{eff} = 1.2$ μm.

4. Applications

4.1. NMOS inverter on silicon rib

The normalized transfer characteristics for two different V_{DD} along with a SEM image of the inverter showing the biasing scheme is shown in Fig. 6, we keep V_{CC} as well

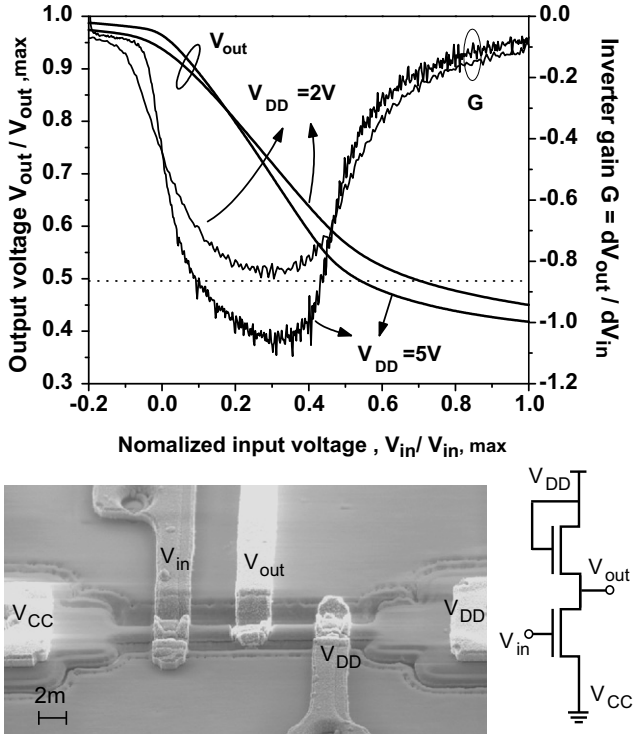

Fig. 6. Normalized transfer characteristics for $V_{in,max} = V_{DD} = 2$ and 5 V as a function of normalized V_{out}, $L_{eff} = 1.5$ μm, $W_{eff} = 1.2$ μm. SEM image of inverter showing the biasing scheme, the gate lengths are 1.5 μm, and $W_{eff} = 1.2$ μm. Inset show the inverter schematic, $V_{CC} = 0$ V.

as the substrate bias V_{BS} at ground potential, V_{DD} is set to either 2 V or 5 V. The gate of the one NMOS is shorted to V_{DD} to form a saturated resistive load, while the input, V_{in}, is applied to the gate of the other transistor. V_{in} is swept from –1 V to V_{DD}. Since the driver and load devices have identical dimensions and similar I_{on} levels, the output voltage V_{out} can only be reduced to about $V_{DD}/2$. The slope is mainly determined by the high load current, combined with a fairly high contact resistance. This issue can be resolved easily by proper device sizing.

Dynamic characteristics are shown in Fig. 7, demonstrating the expected inverter functionality at low frequency switching (switching speed is limited by the measurement setup – high output capacitance due to probe testing – and not by the devices).

4.2. Crossbar addressing with GAA MOSFET

Another application which we foresee for the suspended small dimension GAA devices concerns the decoding scheme for highly-dense cross-bar memories [10]. Cross-bar memories consist of a cross point between two nanowires, containing a memory node, for example a mechanical switch or a molecular junction of variable resistivity. The cross-bar has a high scalability potential since the state is written, stored and read by the cross-bar junction itself, which can be as small as a few tens of nanometres. However, an interface between the nanoscale cross-bar memory and the micro-scale external circuitry, an addressing scheme, is required. The GAA Si NW technology is perfectly suited for this purpose, as the Si NW channel can serve as one of the dimensions of the cross-bar, while the micron-scale poly gates are used for addressing a specific row, see Fig. 8. The fabrication of a GAA inverter is the first step towards this goal, which requires the integration

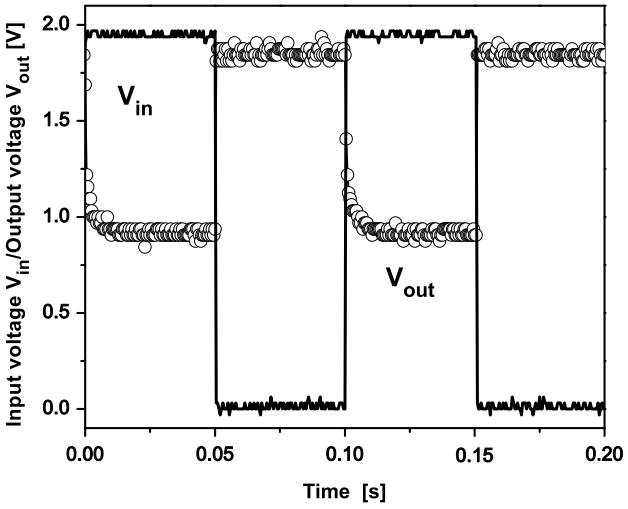

Fig. 7. Dynamic characteristics of the NMOS NW inverter. $V_{DD} = 2$ V, $V_{BS} = V_{CC} = 0$ V. The equal size of the two devices results in half the voltage swing at the output. The frequency is limited by the experimental set-up.

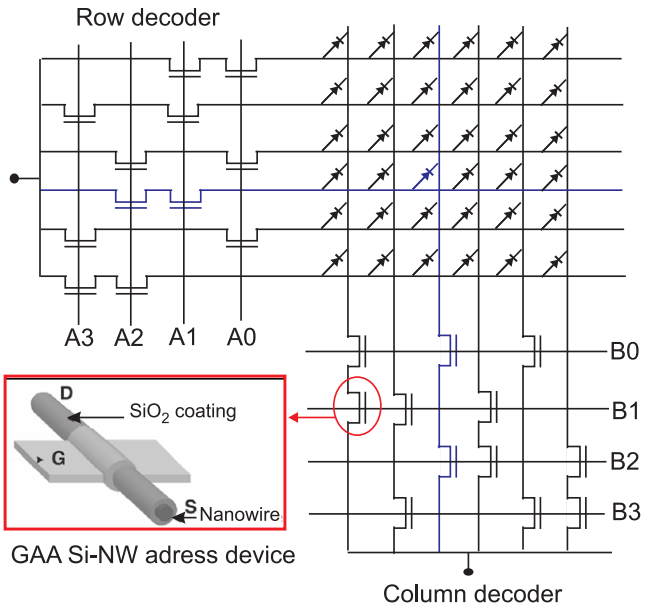

Fig. 8. Schematic of a decoding scheme to select a unique device in the cross-bar matrix.

of multiple transistors (gates) on the same nanowire. A detailed theoretical analysis of the addressing scheme under expected device parameter variations in the present technology is presented in [11].

5. Conclusion

In this paper we have demonstrated the design and fabrication of GAA and body-tied Ω-gate MOSFETs and we have reported the electrical characteristics of the individual devices. I_{on} enhancement in GAA devices compared to Ω-gate devices is observed due to tensile strain.

Furthermore, an NMOS inverter based on Ω-gate devices has been implemented on a silicon rib and its functionality is demonstrated.

Acknowledgement

This work was partially funded by the Swiss CCMX, Materials for Micro- and Nanosystems research project.

References

[1] Y. Cui, C.M. Lieber, Science 291 (5505) (2001) 851–853.
[2] O. Hayden et al., Small 3 (2) (2007) 230–234.
[3] J.D. Holmes, K.P. Johnston, R.C. Doty, B.A. Korgel, Science 287 (5457) (2000) 1471–1473.
[4] M.S. Gudiksen et al., Nature 415 (2002) 617–620.
[5] S.-M. Koo et al., Nano Lett. 4 (11) (2004) 2197–2201.
[6] S.D. Suk et al., Tech. Dig. IEDM (2005) 717–720.
[7] K.E. Moselund, V. Pott, D. Bouvet, A.M. Ionescu, ESSDERC 2007, Tech. Dig. (2007) 287–290.
[8] K.E. Moselund et al., IEDM 2007, Tech. Dig. (2007) 191–194.
[9] K.D. Buddharaju et al., ESSDERC 2007, Tech. Dig. (2007) 303–306.
[10] A. DeHon, Trans. Nanotechnol. 2 (1) (2003) 23–32.
[11] M.H. Ben Jamaa et al., ICCAD 2007, Tech. Dig. (2007) 765–772.