Reliable Communication in Systems on Chips

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Cathegories and Subject Descriptors

B.8Performance and Reliability

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System on Chip (SoC) design faces several challenges which are due to the extremely small nature of electronic devices and the consequent opportunity to realize multi-processing systems of extremely high complexity. To manage large scale design, SoCs are assembled out of complex standard parts, such as programmable cores and memory arrays. Thus, the major design challenge is to provide correct and reliable operation of the interconnected components. Top-down correct component interconnection will become increasingly harder to succeed, because the interface features of components will also scale-up in complexity. New design methodologies will need to leverage component self-configuration and adaptation to the underlying communication fabric.

The structured realization of on-chip interconnection is the future *platform* for multi-processor SoC design, and consists of a *micro-network* of components, where routing wires can be abstracted as communication channels [1, 3]. Due to device downsizing and voltage downscaling, signal transmission will face an increasingly noisier environment, where noise abstracts undesirable effects such as timing variations, cross-talk and interference.

The design of micro-networks requires the combination of techniques coming from networking and micro-electronic domains. Design objectives include achieving high bandwidth with low communication latency, low error rates and low energy consumption. Opportunities stem from the ability of using *ad hoc* networks on chip and designing communication protocols customized to the application and architecture.

Micro-network design can be achieved by extending synthesis technology to cope with the particular features of micro-networks and their components, such as programmable switches, pipelined links and network interfaces to programmable cores and memories [6]. The support for optimization of the network topology and parameters will provide competitive advantage over manual solutions.

Reliable network design will address coping with signal integrity in the physical channels while supporting reliable end-to-end data transmission. Note that signal integrity may be consciously lowered while searching for operational voltages of computational/storage units and voltage swings on links that reduce the system energy consumption [8].

Information encoding, packetization and routing are distinctive aspects of reliable micronetwork design [2]. Information encoding in switches or data interfaces has shown to be effective in raising the *mean time to failure* (MTTF) of communication links in noisy environments. Shadow registers have been successful used to increase resiliency against soft errors, and more generally, against timing errors.

Data packetization provides us with a versatile framework to encapsulate data for reliable transmission with a low overhead. Different packetization schemes and packet routing strategies [9]have also been addressing specific needs for micro-networks, such as the support for guaranteed throughput on specific links in combination with best-effort communication services on other links[4].

Overall, the design of reliable micronetworks is a challenging research area. The combination of various design objectives, such as performance, low-energy communication, and MTTF addresses some of the current needs of the design community. Moreover, the ability to synthesize and optimize reliable micro-networks provides a competitive advantage for the realization of complex multi-processor SoCs.

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