

Robust System Design with Uncertain Information

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New opportunities and challenges in system design are direct consequences of the progress in semiconductor technologies, and are due to the extremely *small* nature of electronic devices, the extremely *large* complexity of systems, and the *new*, uncharted territory set by novel technologies.

As miniaturized devices approach the physical limits of operation, the characterization of their parameters becomes an increasingly harder task. The spread of physical parameters complicates design, as traditional, conservative worst-case design approaches may hinder the advantages of using extremely scaled-down devices. New, aggressive design methods may address the problem by using self-calibrating circuits and error-resilient computation and communication. New design methodologies will be based on a design paradigm shift: electrical level information may happen to be corrupted, yet systems will yield reliable services because means are provided to correct for such errors. At the same time, the amount of effort spent in correcting information may be used to calibrate operational parameters (e.g., voltages) so that error rates fit within desirable bounds.

As systems become also more complex, their assembly will be made out of complex standard parts, such as processor and controller cores and memory arrays. The major design challenge will be to provide correct and reliable operation of the interconnected components. Also for this reason, new design paradigms will be used. Top-down correct component interconnection will become increasingly harder to succeed, because the interface features of components will also scale-up in complexity. New design methodologies will leverage component self-configuration and self-healing [1], to increase system-level availability.

Reliable on-chip communication will require viewing routing wires as information channels, and systems as *micro-networks* of components. Signal transmission will face an increasingly more noisy environment, where noise abstracts undesirable effects such as timing variations, cross-talk and interference. Techniques borrowed

from networking will be applicable at the chip level, to provide reliable communication over unreliable physical channels [2]. Information encoding, packetization and routing will provide us with a new facet of design, to support reliable data transfer in a noisy environment [3].

Forthcoming computing technologies (non silicon based) will enable the design of systems with a much higher density of switching devices. On the other hand, monolithic systems constructed with self-assembly techniques will also display a much higher defect density. The unprecedented amount of computational power will be useful only if new design methodologies will be able to insure correct and reliable design on an unreliable physical medium. Again, techniques based on encoding, computation and communication redundancy and re-configuration will be key to the success of these technologies. In this respect, designing monolithic systems based on nano-technologies will face challenges similar to those of CMOS scaled-down towards its physical limitations. Indeed, robust large-scale system design, with advanced technologies that push devices towards the physical limits of materials, requires solving system-level information management problems.

REFERENCES

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