Design and Implementation of CMOS Image Sensors for Biomedical Applications

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PAR

Gözen KÖKLÜ

acceptée sur proposition du jury:

Prof. A. Kis, président du jury
Prof. Y. Leblebici, Dr S. Carrara, directeurs de thèse
Dr C. Dehollain, rapporteuse
Prof. R. Etienne Cummings, rapporteur
Dr P. Georgiou, rapporteur

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To my parents and my lovely sister ...
Anneme, babama ve canım ablama...

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Abstract

Since the first introduction of digital cameras, the camera market has been taking tremendous interest from many fields. This trend has even accelerated when the cost, size, and power consumption of such devices were reduced with the introduction of camera on a chip concept. This concept is achieved by integrating photoactive and electronics parts of digital cameras on a single chip with Complementary Metal Oxide Semiconductor (CMOS) technology but resulted in reduced photon collection efficiency and increased noise. Since then, scientists and researchers have been putting a huge effort to improve the quality of CMOS image sensors with advancements in lithography and fabrication process, by finding alternative ways of increasing the fill factor, designing lower noise circuits, and putting additional on chip features. Despite these efforts and cost, integration, and power consumption advantages of CMOS image sensors, they have still not been preferred in many application fields such as biomedical imaging, where high quality imaging is targeted. Recently, with the process related technological advancements, the cost of CMOS image sensors have increased and this has made the CMOS image sensors loose their cost advantage and attractiveness for low cost applications.

In this thesis, I summarize my research effort in integrating the low-cost CMOS image sensors in biomedical applications and improving their performance with novel circuits fabricated with standard CMOS process, while maintaining their cost advantage. Towards this aim, I propose possible ways of implementing pixel array sensors and noise reduction and read-out related circuits with standard CMOS technology in order to make these low-cost sensors applicable for biomedical applications. For this purpose, this research started by fabricating a characterization chip that uses standard CMOS process compatible photodiodes and pixels. Using this chip, I obtained characterization data for an n-well 0.18μm standard CMOS technology and made it available for designers using similar technologies. Later, I developed a small camera prototype by using the characterization data of the first chip. This small camera chip includes efficient pixel circuits with column parallel fully differential noise reduction circuits, and horizontal and vertical access circuits. After obtaining good quality images using this camera prototype, I designed a larger array camera chip, which offers Video Graphics Array (VGA) resolution, using the same technology. This third camera chip uses pixel sharing technique, which results in 1.75 transistors per pixel. Moreover, this design provides the flexibility of changing the pixel array resolution with respect to the pixel size, aiming to optimize the performance according to the application. In order to result in highest possible fill factor, all of these fabricated chips use Active Pixel Sensor (APS) technique. Within the scope of this

thesis, I also propose novel Digital Pixel Sensor (DPS) designs, which would bring chip-level additional functions for biomedical imaging applications and hold the potential for future devices.

Keywords: CMOS image sensors, CCD image sensors, CMOS cameras, CCD cameras, biomedical imaging, digital cameras, noise reduction circuits, CDS, correlated double sampling, fluorescence imaging, Active Pixel Sensor, Digital Pixel Sensor, APS, DPS, Charge Coupled Devices, CMOS imager, pixel array, 3T APS, 4T APS, rolling shutter, global shutter, pinned-photodiode, partially pinned-photodiode, event-detection sensor, address-event representation protocol, AER

Résumé

Depuis l'introduction des premiers appareils numériques, le marché de l'appareil photo a énormément gagné en intérêt dans de nombreux domaines. Cette tendance s'est même accélérée lorsque le coût, la taille et la consommation d'énergie de ces appareils ont été réduits grâce à l'introduction du concept de camera on a chip. Ce concept consiste à intégrer les éléments photosensibles et électroniques des appareils photo numériques sur une seule puce au moyen de la technologie Complementary Metal Oxide Semiconductor (CMOS). Ce procédé a toutefois pour conséquence une efficacité réduite dans la collecte des photons ainsi qu'à une augmentation du bruit. Dès lors, les scientifiques et chercheurs se sont efforcés de consacrer leurs efforts sur l'amélioration de la qualité des capteurs d'image CMOS. Cette amélioration devait passer par d'importants progrès au niveau de la lithographie ainsi que dans le processus de fabrication. Pour ce faire, il a fallu créer des solutions alternatives pour augmenter le facteur de remplissage, élaborer des circuits plus silencieux ainsi que développer les caractéristiques de la puce. En dépit de ces efforts et des performances comparables des capteurs CMOS par rapport à leurs principaux concurrents, les capteurs d'image CMOS n'ont toujours pas la cote dans de nombreux domaines tels que l'imagerie biomédicale, discipline nécessitant une imagerie de très haute qualité. C'est surtout le processus lié aux progrès technologiques qui a conduit à augmenter considérablement le prix des capteurs d'image CMOS, entraînant de ce fait une importante perte d'attractivité.

Cette thèse est destinée à prouver qu'une utilisation de capteurs d'image CMOS peu coûteux est possible dans différentes applications biomédicales. Pour ce faire, je propose des solutions qui, d'une part, améliorent la performance de ces capteurs par le biais de nouveaux circuits fabriqués avec le processus CMOS standard, et d'autre part, permettent de conserver leur avantage en terme de coût.

À cette fin, je propose plusieurs moyens de mettre en œuvre des conception de circuits d'image capteur avec la technologie standard CMOS afin de rendre ces capteurs à faible coût applicable pour des applications biomédicales. A cet effet, cette recherche a commencé par la fabrication d'une puce de caractérisation qui utilise des photodiodes et pixels compatibles avec la technologie CMOS.

En utilisant cette puce, j'ai obtenu les données de caractérisation pour la technologie UMC 0.18µm standard CMOS. Ensuite, j'ai développé un petit prototype de caméra à l'aide des données de caractérisation de la première puce. La puce de la petite caméra inclut des circuits de pixels efficaces comprenant des techniques parallèles de réduction du bruit entièrement différentielles. Après avoir obtenu des images de bonne qualité en utilisant ce prototype de

caméra, j'ai conçu une puce de caméra grand tableau, proposant le standard d'affichage Vidéo Graphics Array (VGA), utilisant la même technologie.
Cette troisième puce d'appareil photo utilise une technique de partage de pixel de1,75 transistors par pixel. De plus, cette conception offre la possibilité de modifier la résolution de la matrice de pixels en fonction de la taille des pixels, dans le but d'optimiser les performances suivant l'application donnée. Toutes ces puces fabriquées utilisent la technique Active Pixel Sensor (APS). Dans le cadre de cette thèse, je propose également des modèles Digital Pixel Sensor (DPS) novateurs, apportant des fonctions supplémentaires au niveau de la puce pour les applications d'imagerie biomédicale.

Mots clés : Capteur photographique, CMOS Capteur d'image, CCD Capteur d'image, Microscopie optique, Microscopie fluorescence, CDS, réduction du bruit

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1 Introduction

After the long evolution of cameras, digital cameras are the end products that have made the camera technology accessible to everyone today. The evolution towards digital cameras started with the invention of Charged-Coupled Devices (CCDs) in 1969 at the Bell Labs by Drs. Willard Boyle and George Smith. Although the invention of Complementary Metal Oxide Semiconductor (CMOS) technology dates back to late 70s, it was only early 90s when finally this technology was suggested for use in image sensors. After the first introduction of Active Pixel Sensors (APS) in Complementary Metal Oxide Semiconductor (CMOS) image sensors, it has been straightforward to envision a single chip camera that integrates the pixel array with photo-device and pixel electronics, timing and control electronics, signal processing electronics, and analog to digital converter and interface. The concept of electronic camera on a chip paves the way to the inevitable rise of today's modern CMOS image sensors. With this concept, CMOS cameras started to provide higher integration capability, lower power consumption, smaller area, and lower cost compared to its major competitor, CCD cameras. These advantages of CMOS cameras have made them inevitable for portable and low-cost devices.

In 1995, E. Fossum has stated that "If the cost of the camera can be made sufficiently low (e.g. $100 or less per camera), it is expected that most personal computers will have at least one camera peripheral"[Fossum, 1997]. Now, 20 years after this statement has been made, considering how many cameras we have around right now is enough to understand how aggressively the CMOS camera market has been growing. Today, most of the people uses a smart phone that integrates one or more number of high resolution cameras with minimum 2 Mega Pixel (MP), plus has laptops, digital cameras, even toys and game stations, which are all integrated with high quality cameras. According to the IC Insights' 2012 Optoelectronics, Sensors, Actuators, and Discretes (O-S-D) Report, after having hard times in the second half of the last decade, CMOS image sensor sales have increased to $6.3B in 2012 and expected to climb to $10.8 billion in 2016 as presented by Fig. 1.1 [ICInsight, 2012]. Similar to this, according to a recent study from Yole Developpement (Lyon, France), the global CMOS image sensor market was worth about $7.8 billion in 2013 and will be worth about $13 billion in

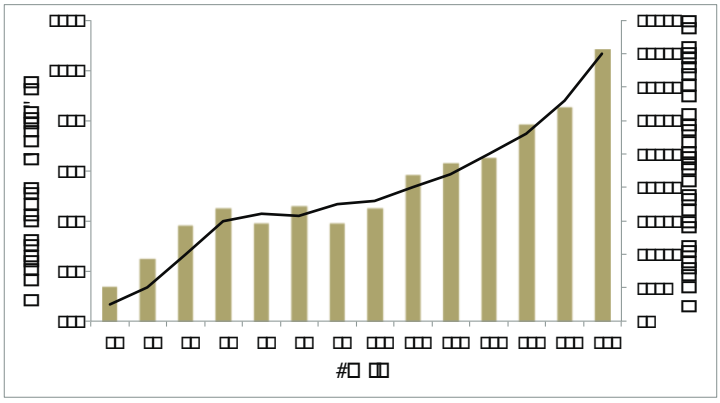


Figure 1.1: IC Insights' 2012 O-S-D Report

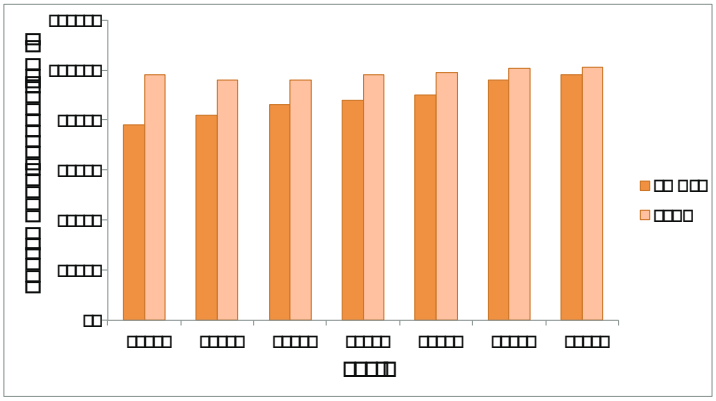


Figure 1.2: Image Sensor Consumption Revenue Forecast, 2012–2018 [IHS, 2012]

2018 [Optics.org, Jan 2014]. When considering such an aggressive market and innovations and improvements to fill the need in the market, it is only straightforward to expect a growing interest towards CMOS cameras from other application fields as well. Today, CMOS camera modules are gaining popularity and seeing increased demand not only across portable and low-cost devices but also for industrial, medical, and automotive sectors, which were initially dominated by CCD cameras. According to a recent study by IHS Technology (Fig. 1.2), CMOS image sensors accounted for over 80% of image sensor revenue in 2013 and is expected to reach 98% in 2018.

In medical imaging sector, standard CMOS cameras have taken a lot of interest especially for applications where the inherent advantages of CMOS cameras e.g. low cost, low power consumption, and high integration capability, are inevitable. Lab on chip (LoC) devices integrated with cameras are some examples of these type of applications, which usually target cost-effective, easy-to-use, and relatively high quality testing solutions. Fluorescence imaging is one of the main analysis methods in today's biomedical LoC devices, which has become an essential tool in biology and biomedical sciences after the introduction of fluorochromes. Biologists use fluorochromes to stain cells and tissues components, bacteria and pathogens, which

are excited by specific wavelengths of light and emit light at another wavelength. Through the use of multiple fluorescence labeling, different probes can also be used to simultaneously identify several target molecules at different wavelengths, which has led to further evolution and interest in this domain. In the literature, we can find many examples of LoC fluorescence imaging devices such as; miniature microscopes for brain imaging of freely moving animals [Murari et al., 2010], micro-optic/micro-fluidic devices for biochemical analysis [Roulet et al., 2002], portable fluorescence detection systems for Point-of-care (PoC) systems for cancer or Human Immunodeficiency Virus (HIV) diagnostics [Zhang et al., 2012], and LoC platforms fur nutrition analysis [Ramadan et al., 2013].

Recently, with the introduction of Scientific CMOS (sCMOS) cameras, CMOS cameras have also started to appear in high quality low-light medical imaging applications e.g., optical microscopy or optical fluorescence imaging. However, these cameras cost much higher than standard CMOS cameras and no longer provide a cost advantage when compared with CCDs. Thus, the use of sCMOS cameras for low-cost biomedical applications is not applicable, instead, new technologies and novel circuit solutions should be considered to improve the performance of standard CMOS cameras and to keep their cost advantage. This is important not only for low-cost biomedical devices e.g., PoCs and LoCs [Greenbaum et al., 2012],[Ramadan et al., 2013], [Ji et al., 2006], but also for increasing the accessibility to high quality optical detection systems integrated with optical microscopy in under-developed or developing countries.

Hence, within the scope of this thesis, I investigated the possible ways of implementing low-cost, high quality optical detectors for use in the optical detection systems, more specifically in the fluorescence imaging systems. As mentioned earlier, today, most of the microscopy or biomedical imaging systems are integrated with CCDs, presumably resulting in better data collection efficiency in low light levels compared to CMOS cameras. However, CCD cameras cost approximately one order of magnitude higher than CMOS cameras [Köklü et al., 2012]. This is why the target of this research has been the replacement of the high-cost CCD cameras of biomedical imaging systems with low-cost CMOS cameras and showing the merit of CMOS cameras in these applications [Köklü et al., 2012], [Köklü et al., 2013b]. Throughout this thesis, I have proved the concept of successful use and implementation of standard CMOS cameras in biomedical applications. In addition, I have developed novel circuits and systems to improve the performance of current CMOS cameras while keeping their cost advantage. I also sent three camera chips for fabrication towards this purpose and provide their simulation and measurement results within this thesis.

Following the introduction, the rest of this thesis is organized as follows:

In Chapter 2, I explain the basics of CMOS and CCD cameras and discuss the advantages and the disadvantages of each technology. I also define the camera specifications within this chapter, which are specifically important for biomedical imaging.

After presenting a brief explanation on available technologies for biomedical imaging and

providing their performance parameters, in Chapter 3, I show examples of the state of the art CCD and CMOS cameras which are available in the market or in the literature and appropriate for use in biomedical (microscopy) imaging applications.

In order to provide a proof of concept for use of low cost CMOS cameras in high quality, low light imaging applications, I build a CMOS camera by integrating a CMOS image sensor from the market with an Field Programmable Gate Array (FPGA) platform. In Chapter 4, I present the details of this camera. In addition, I provide a quantitative comparison of this CMOS camera with the default CCD camera of an inverted microscope based on the application specific collected images. After improving the quality of these images with image processing algorithms, I show that the low-cost CMOS camera results in comparable performance with the high-cost CCD for low-light fluorescence imaging [Köklü et al., 2012], [Köklü et al., 2013b].

After showing that the CMOS cameras may reach comparable quality with CCDs, in Chapter 5, I start the design process of application specific camera chips. Designing application specific camera sensors gives the flexibility in choosing the optimum pixel pitch and photodiode size, providing priority to some specific circuits than the others, and integrating additional pixel level or chip level. This chapter includes the introduction of different CMOS pixel sensor circuits and techniques that are compatible with standard CMOS process and the advantages and disadvantages of each technique when used for biomedical imaging applications. In this chapter, I also present state-of-the art Active Pixel Sensor (APS) and Digital Pixel Sensor (DPS) designs, which are the two main types of CMOS pixels.

I start the camera chip implementation process by first designing a pixel and photodiode characterization chip. Since each CMOS technology has its own characteristics and photon response and the foundries do not provide photon related characterization data, designers always have the need to develop their own characterization chips. Within this context, in Chapter 6, I explain the details of my characterization chip. This chip includes different standard CMOS process compatible photodiodes and pixels. Within this chapter, I also present the characterization results of this chip, which is specific to an $n-well 0.18\mu m$ standard CMOS process. I obtained the characterization data by testing the fabricated chip through an optical setup. Then, when designing the other camera chips throughout this research, I benefited from the characterization results of this chip. To the best of my knowledge, with this characterization chip, I provide for the first time characterization results not only for an $n-well 0.18\mu m$ standard CMOS process but also for a process that uses Shallow Trench Isolation (STI) instead of Local Oxidation Isolation (LOCOS), which immensely affects photodiode dark noise [Köklü et al., 2013a].

In Chapter 7, I demonstrate my first fully functional camera chip that integrates a small active pixel array (64×60) with photodiodes and surrounding pixel electronics, noise reduction circuits, and vertical and horizontal access circuits. I have implemented this chip according to the data obtained from the characterization chip as mentioned earlier. Within this chapter, I explain the design details of each block in this camera chip together with the novel methods

to improve the quality of this camera [Köklü et al., 2011]. After introducing the design details and measurement results, I illustrate the image acquisition interface of this camera chip and provide collected images from this camera chip by using test patterns. This camera chip provides a fully functional prototype of a low-cost high quality CMOS camera. However, since this camera prototype has a small array size, a larger array format camera chip would be required in order to achieve large format smooth images with real biomedical samples.

In Chapter 8, I present the design of the Video Graphics Array (VGA) format camera chip that integrates active pixel array of VGA resolution, together with column parallel noise reduction circuits, horizontal and vertical access circuits, and two parallel Successive Approximation (SAR) type Analog to Digital Converters (ADCs). This design benefits from an efficient pixel sharing technique in order to increase the fill-factor and the light collecting efficiency. It also provides to the best of my knowledge for the first time in the literature a novel programmable interface to adjust the array size with respect to the pixel size depending on the application.

Within the frame of this research, I fabricated only APS camera chips due to the high fill factor and photon collection efficiency advantages of these designs. However, DPS designs offer many advantages as well e.g. avoiding analog design limitations and providing extra pixel level features. Even tough DPS designs bring pixel area penalty, these features are worthwhile to consider in biomedical applications. Hence, in Chapter 9, I propose novel DPS designs that are optimized for biomedical applications [Köklü et al., 2013c]. In the future, the use of DPS designs with Back Side Illumination (BSI) technique would certainly omit the fill factor limitation of these designs and only then it is evident to reach good quality DPS camera chips similar to APS camera chips.

2 CMOS and CCD Cameras

Today, CMOS image sensors are displacing the CCDs in high volume applications where low cost, low power, low area and high speed are unavoidable. However, despite the huge research effort, advancements in lithography, higher fill-factor and low noise achievements in CMOS cameras, CCDs are still the dominant choice in high quality imaging applications i.e. biological and microscopic applications. Knowing that the budget constraints always exist for every research domain, choosing the most profitable and cost-efficient optical detector for the specific research purpose is a very important step. To do that, it is first necessary to understand the basics of CMOS and CCD cameras and their structural and intrinsic differences.

2.1 Introduction

The key to reach a good quality optical microscopy imaging goes through improving the efficiency of the optical light path of the microscope, as well as optimizing the optical detector's Signal to Noise Ratio (SNR) to detect as much light as possible [Frigault et al., 2009].

Traditionally, it is known that CCD cameras target high imaging quality and they have always been the dominating optical detector choice in the microscopy imaging market. In the literature, there are many examples of use of CCD cameras for detecting fluorescent labeled Deoxyribonucleic Acids (DNAs) or some expressions on the stained, fixed or live cells by using optical microscopy. Some of the examples to that is imaging of growing DNA chains [Ansorge, 2009], real-time detection of DNA hybridization to DNA microarrays [Sapuppo et al., 2008], monitoring of anticancer effects of some specific agents [Kang et al., 2010], examining of cell polarity on stained, fixed and live cells [Osmani et al., 2010] and obtaining quantitative information about the chromatin-DNA distribution inside the nucleus [Nicolini et al., 1997], [Mascetti et al., 1996], [Mascetti et al., 2001]. In addition, most of the microscopy companies only provide CCD cameras for optical microscopy applications and in many related review papers and books, CCD cameras have been shown as the detector of choice for low-light i.e.,fluorescence, microscopy imaging applications ([Frigault et al., 2009], [Spring, 2007], [Moomaw, 2012], [Golden and Ligler, 2002]).

On the other hand, CMOS cameras and image sensors have mostly been used in low performance devices or portable devices until recently [Fossum, 1993]), mainly due to their low power consumption, low cost, compactness and high integration. Recently, this traditional misconception of CCDs as a must for high quality imaging applications, started to dissolve and CMOS imagers started to show up in high quality Digital Single Lens Reflex (DSLR) cameras as well as in biological and bio-medical microscopy applications. A couple of examples for the use of CMOS cameras in biological applications include miniaturized fluorescence cameras for brain imaging [Murari et al., 2009b], [Murari et al., 2010], [Ghosh et al., 2011] and fluorescence lifetime imaging with CMOS Single Photon Avalanche Diodes (SPADs) [Li et al., 2010], [Schwartz et al., 2008] where CMOS sensors' speed advantage become crucial. In addition, recently some of the microscopy companies started to offer CMOS camera solutions for bio-medical applications. Moreover, the potential use of low-cost CMOS cameras has been shown for fluorescence imaging when the collected images are empowered with image processing algorithms [Köklü et al., 2013b].

In the following sections, first, I will put emphasis on the structural differences of CCD and CMOS cameras, second, I will introduce the performance parameters of CMOS and CCD cameras and image sensors, third, I will explain the methods that are used to compare different cameras, and finally, I will show different image processing algorithms that are applicable for image enhancement and noise reduction in CMOS camera images.

2.2 CCD/CMOS Image Sensors and Cameras

Fig. 2.1 illustrates the differences of CMOS and CCD sensors. The figure basically compares a CMOS Active Pixel Sensor (APS) design with an Inter Line CCD (IL-CCD) which are both most commonly used sensors in the microscopy imaging camera market. This figure shows that CCD sensors are composed of photosensitive area and registers, and produces an analog output while the CMOS image sensors are not only composed of photosensitive areas but also surrounding electronics including scanning and digital conversion electronic circuits and produces a digital output.

This structural difference between CCD and CMOS sensors usually leads to difficulties to compare their camera performances. That is because the main noise sources in a CMOS sensor include dark current noise, shot noise, temporal noise, fixed pattern noise and digital readout noise, but in a CCD sensor, it consists of only pixel level dark signal, shot noise and on chip analog readout noise [Tian et al., 2001]. However, as mentioned earlier, a CCD camera consists of not only a CCD sensor but also off-chip signal processing, noise reduction and readout circuits. Thus, in a CCD, while the off-chip noise reduction circuit decreases the generated noise, the readout circuit increases it. Hence, the comparison made on the sensor performances does not provide enough information to draw a conclusion to define these cameras' noise floor or minimum light detection limit. That is why instead of relying on the data-sheet performances of the sensors, which would be misleading if a CMOS sensor

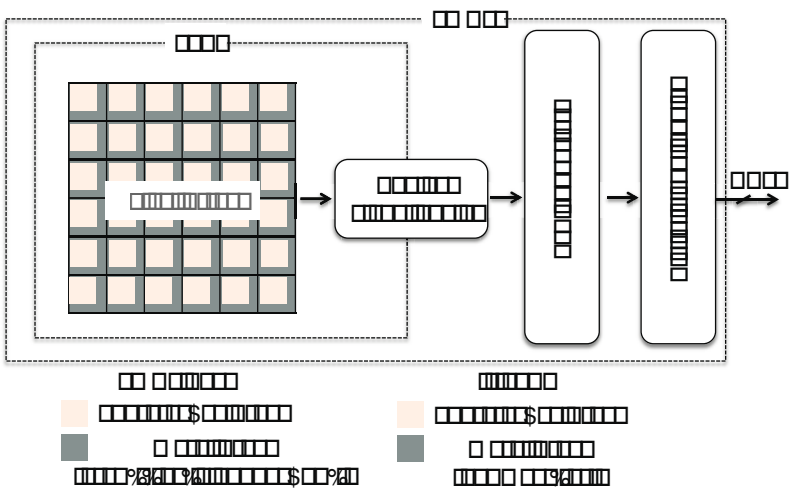


Figure 2.1: General View of CMOS and CCD Sensors

is compared with a CCD sensor, it is better to compare the two cameras directly based on the application-specific collected images [Köklü et al., 2013b] or by using a very well known camera comparison technique called Photon Transfer Curve (PTC) [Janesick et al., 1987], [Janesick, 2001]. PTC is a technique that plots noise against signal and is used to measure many of the camera performance parameters. A straightforward comparison between a CCD and a CMOS camera can also be made based on their performance parameters, however this comparison should rely on the specifications given in the camera data-sheets instead of the sensor data-sheets. For the CMOS devices, the sensor and the camera data-sheet specifications are expected to be the same or similar depending on the cooling and packaging of the device however this is not the case for CCD devices.

In the following section, I will explain the CMOS and CCD camera architectures in more detail.

2.2.1 CCD Image Sensors and Cameras

There are many different CCD architectures, mainly as Full-Frame CCD (FF-CCD), Inter-Line Transfer CCD (IL-CCD), and Frame Transfer CCD (FT-CCD) [Aikens et al., 1989]. Each of these architectures have advantages and disadvantages where they can be more useful than the other depending on the application. Electron Multiplying CCDs (EMCCDs) is also considered as one of the CCD architectures, which have recently emerged in the market.

When the silicon and the light on the photo-active surface of CCDs react and excite the charges from the silicon valence band to the conduction band, electrical charges are generated. A CCD is composed of serially connected capacitors and it benefits from the charge transfer mechanism by the movement of the excited electrical charges from one capacitance to another with the digitally controlled pulses [Boyle and Smith, 1970].

2.2.1.1 Full-Frame CCDs

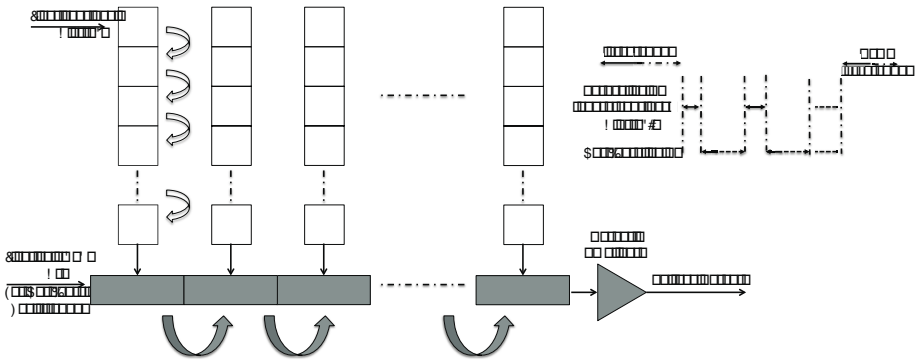
In a FF-CCD, the charges are transported from one well to another on the same vertical line by use of the parallel clocks. At the end of the integration period, the charge packets are transferred to the horizontal registers. The final transfer of the registered outputs are done in single output format by use of serial shift registers with the serial clocks, shifting outputs sequentially starting from the first column to the last. As seen in Fig. 2.2a, in FF-CCDs, the CCD array is a fully photosensitive array with ideally %100 fill factor meaning that the entire pixel array is used to detect incoming photons during exposure to the object being imaged. However, this high fill factor comes with a price of speed. The FF-CCDs require mechanical shutters to control the start and stop of the image capture process and the integration of the next frame can only be started at the end of the whole vertical and horizontal shifting of the registered outputs, which obviously limits the speed of the process. In other words, the use of the mechanical shutter limits the FF-CCDs to take continuous images. In low light imaging applications (fluorescence imaging), although it is preferable to use Full-Frame CCDs (to capture more photons due to the increased fill-factor), since most of the microscopic applications require continuous imaging, the use of the FF-CCDs is only restricted to the digital SLRs in the market.

2.2.1.2 Inter-Line CCDs

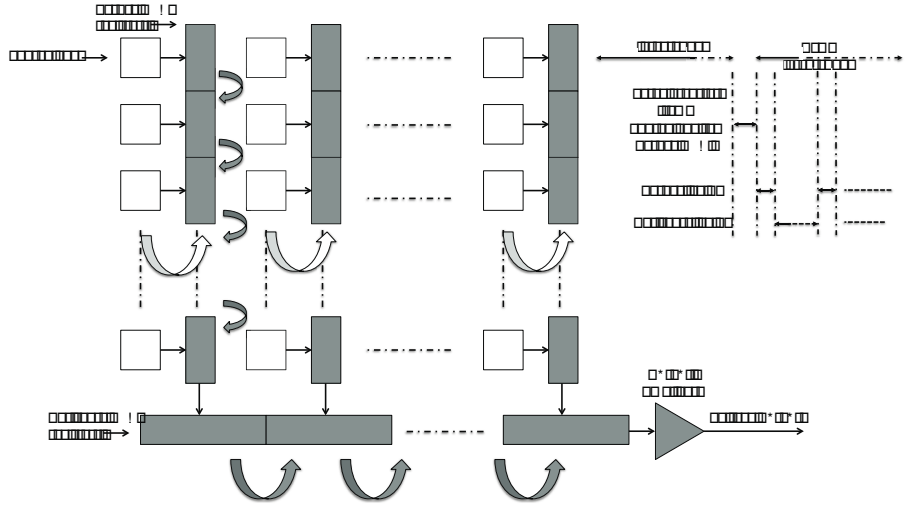
IL-CCDs, Fig. 2.2b, operate with electronic shutters and include a CCD register in each pixel meaning that the speed limitation caused by the mechanical shutter and waiting time for the full transfer no longer exist. In an IL-CCD, each pixel consists of a photodiode and one cell of a CCD register which allows the new integration period to start right after the charge transfer to the register. This of course reduces the fill factor drastically and brings it to the same order as APS CMOS imagers but at the same time establishes a very fast image capture giving possibility to the imager to be used in video mode. Today, with the use of micro-lenses, in IL-CCDs, the fill-factor limitation has been overcome and the IL-CCDs have become the most common CCD types in microscopy camera market. The examples of this type of cameras for microscopic applications will be given in Chapter 3.

2.2.1.3 Frame Transfer CCDs

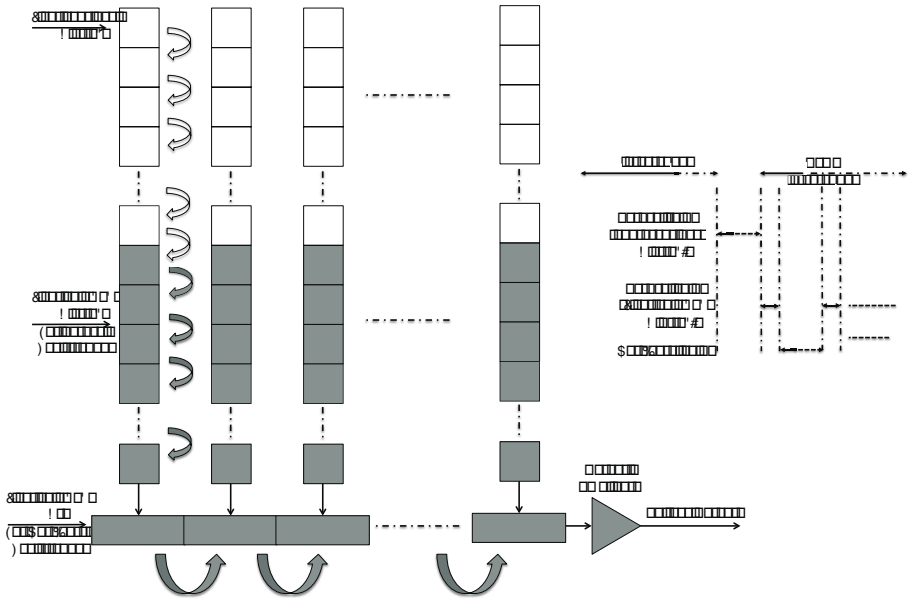
Unlike the other two types, FT-CCDs (see Fig. 2.2c) use half of the imager area as photosensitive area and the other half as optically shielded frame store area. The operation at the top part of this type of CCDs is similar to the FF-CCDs in terms of its requirement for a mechanical shutter and the quick transfer of the charges from top to bottom. The other half of FT-CCD includes only vertical CCD registers which work in a similar manner as the vertical registers in IL-CCD. The advantage of FT-CCDs compared to FF-CCDs is that the operation is pipelined since the new frame can already start to be collected at the end of the charge transfer between the photosensitive array and the light shielded array. In addition, since this type of CCDs does



(a) Full-Frame CCD



(b) Inter-Line Transfer CCDs



(c) Frame Transfer CCDs

Figure 2.2: CCD Types

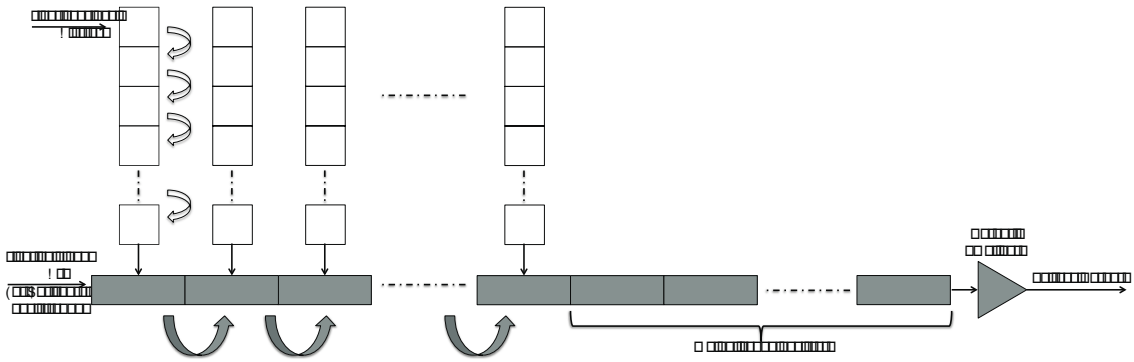


Figure 2.3: EMCCD applied to a IL-CCD architecture

not share active pixel area with the storage pixel area, they reach 100% fill factor. However, the speed is again limited due to the required time for the charge transfer at the photosensitive array unlike the IL-CCDs. Similar to FF-CCDs, FT-CCDs also only appear in professional digital cameras, but not in microscopic imaging due to their incapability of taking continuous images.

2.2.1.4 Electron Multiplying CCDs (EMCCDs)

EMCCDs integrate electron multiplying stages with the conventional CCD architectures with the aim of reducing noise in high speed applications e.g. live-cell real-time imaging. The multiplication register is an extension of the normal serial register and adds gain to the electrons that come out of the sensor's active pixel array which makes EMCCDs easily adaptable to standard CCD designs. This type of CCDs do not have a trade-off between speed and sensitivity as it is the case for regular CCDs. The main reason for this trade-off is the increase of noise generated at the charge amplification unit with the increase of speed, which reduces the minimum detection limit of the sensor. In EMCCDs, since the charge multiplication stage comes before the amplification stage, the noise generated in the amplifier no longer is a problem since the signal is already multiplied and much higher than the noise generated in the amplifier. Thus, EMCCDs are capable of reaching both high speed and high sensitivity which makes them highly preferable for low light live-cell imaging applications in real-time . In the market, I can find EMCCDs of any three type of CCDs.

2.2.2 CMOS Image Sensors and Cameras

The most important advantage of CMOS image sensors over CCDs is their integration capability of the photosensitive and electronic parts, which gives the possibility to fabricate photosensitive and electronics part on the same chip. This advantage of CMOS sensors make the fabrication less costly and easier than CCDs in high volumes. As opposed, the fabrication of CCD image sensors require two different processes, a dedicated process to fabricate the CCDs and a standard CMOS or Bipolar CMOS (BiCMOS) process to fabricate the electronic

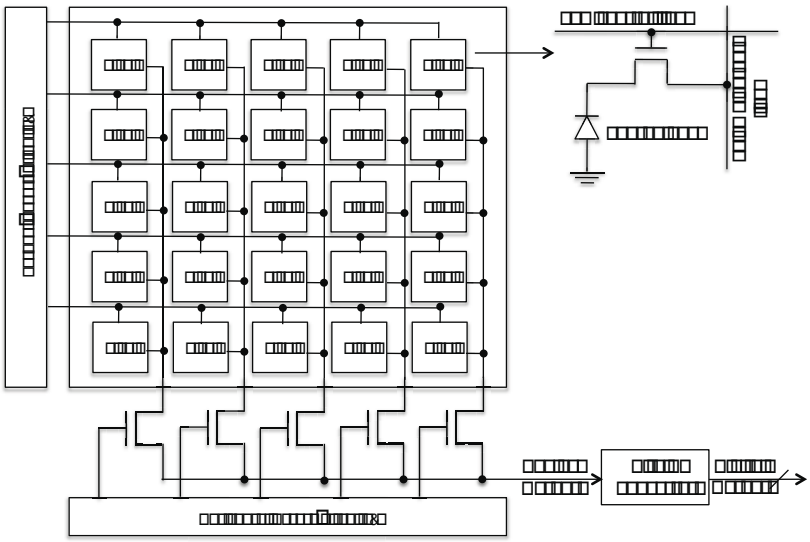


Figure 2.4: CMOS Passive Pixel Sensor Architecture

parts of the cameras. As mentioned earlier, this would increase the cost and area of CCD cameras. However, in low volume productions, due to the higher fabrication mask costs in CMOS devices, the integration capability of CMOS does not necessarily provide cost advantage over CCDs.

Mainly, CMOS image sensors can be grouped in three categories; Passive Pixel Sensors (PPSs), Active Pixel Sensors (APSs), and Digital Pixel Sensors (DPSs). Among these, APS sensors are the most common CMOS sensors in the microscopic camera market.

2.2.2.1 Passive Pixel Sensors

PPSs are the first MOS image sensors that emerged in the market [Koike et al., 1980], [Nabeyama et al., 1981], [Ohba et al., 1980]. However, due to Signal to Noise Ratio (SNR) issues, its development was halted [Ohta, 2010]. They use a single switch in the pixel to read out the photodiode integrated charge as shown in Fig.2.4. The switch transistor in the pixel is used for the row selection and the output or the source terminal of this transistor is a common node for all the pixels in the same column. Because of this simple structure, this design reaches high fill-factor and photon collection efficiency. At the end of each column, there is a column select switch with horizontal access circuit. The design also includes an off-chip amplifier and Analog to Digital Converter (ADC). However, PPSs suffer from many limitations. First, the common column line results in a high parasitic capacitance, which is also the charge to voltage conversion region of the pixel. This high parasitic capacitance is required to be driven by the pixel, which reduces pixel's conversion gain. Moreover, the off-chip read-out scheme introduces high noise and slow read-out. Later, PPS designs with on-chip amplifiers and ADCs have been introduced. These designs have reached lower kTC noise in the sensor. However, still they have not solved the high parasitic capacitance issue at the common column node,

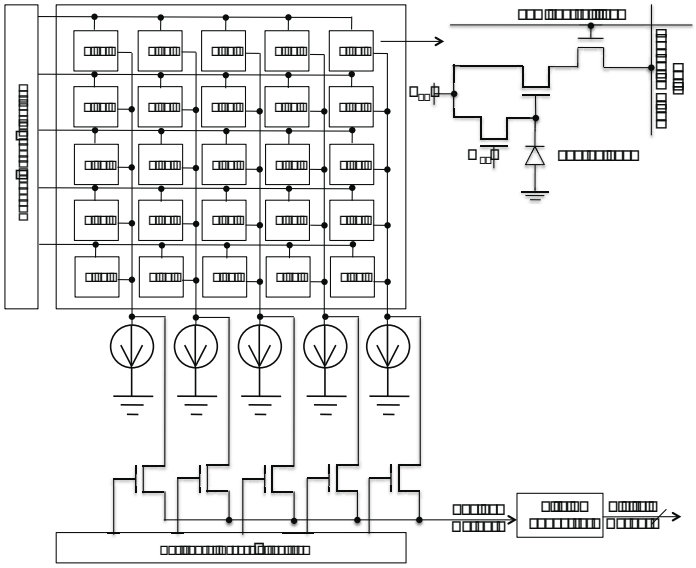


Figure 2.5: CMOS 3-Transistor Active Pixel Sensor Architecture

which is the limiting factor for the detection of low light signals.

2.2.2.2 Active Pixel Sensors

The PPS designs are later replaced by APS designs, where each pixel has an active element providing pixel-level amplification and improving the image quality compared to PPS designs. An example to APS pixel circuits is the 3 Transistor (3T) APS pixel circuit. A top level representation of the APS design with a 3T pixel circuit is shown in Fig. 2.5. Chapter 5 will provide more details on APS type pixel sensors.

Fig. 2.4 and 2.5 show the digital conversion unit per chip, which is connected at the end of the horizontal access circuity. It is also possible to generate column level or pixel level digital outputs, where both techniques are mostly used to speed up the readout process.

2.2.2.3 Digital Pixel Sensors

The CMOS image sensors with pixel level analog to digital conversion are called Digital Pixel Sensors (DPSs). Nowadays the trend in CMOS image sensors is to increase the functionality of the devices by benefiting from DPS designs, which integrate the pixel with ADC units as presented in Fig. 2.6. The DPS designs require large amount of non-photosensitive/metallic area causing a significant drop in the fill-factor and increase in the pixel pitch. However, DPS architectures offer several advantages over analog image sensors including better scaling with CMOS technology due to the reduced analog circuit performance demands, and the elimination of read-related column Fixed Pattern Noise (FPN) and column readout noise. More details on the DPS architectures will be covered in Chapter 5. The DPS designs may

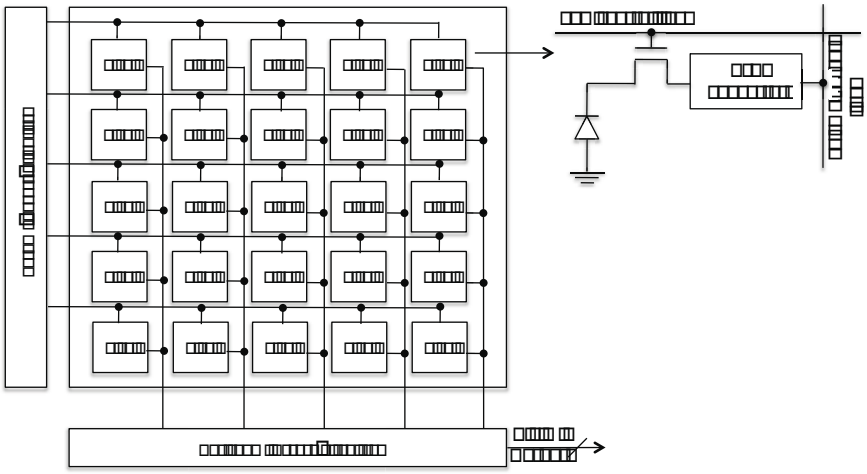


Figure 2.6: CMOS Digital Pixel Sensor Architecture

also serve well in microscopic applications when integrated with Back Side Illumination (BSI) technology to compensate the low fill-factor and high metal density. However, to the best of our knowledge, currently there are no DPS cameras available in the market for microscopic applications and it is the APS cameras that benefit from BSI technology.

2.2.2.4 Further Advances in CMOS Image Sensors

Until recently conventional Front Side Illumination (FSI) technique has been used in CMOS image sensors. In FSI technique, the light travels to the photo-sensitive area through the front side of the camera chip, i.e., pixel, it first passes through the transistors, the dielectric layers and metal circuitry, which can block or deflect it into neighboring pixels, causing a reduced fill factor and additional problems such as cross talk between pixels. The solution to this problem has been found by reversing the sensor and illuminating it from the back-side. This technique is called Back-Side Illumination (BSI) [Nixon et al., 2002]. BSI provides many advantages including high (100%) fill-factor, increased quantum efficiency, efficient implementation of anti-reflection coatings, and improved angular response, while being compatible with the traditional implementation of the pixels [Pain et al., 2005]. Recently, this technique has become very popular and is used in most of the high-sensitive CMOS sensors to improve the performance by allowing an easier travel path for the light before passing to the photo sensitive area and has resulted in almost 30% improvement in Quantum Efficiency (QE) compared to FSI designs (for details on QE see Chapter 3).

Most of today's CMOS image sensors are fabricated with CMOS Image Sensor (CIS) dedicated technologies where the standard CMOS technology has been improved for better photon sensitivity and lower noise. This trend has increased the cost of CMOS image sensors and the production cost has reached similar to CCDs. However, in higher volumes, CMOS devices still cost less than CCDs due to the single chip integration capability.

Finally, similar to IL-CCDs, CMOS image sensors also benefit from micro-lenses to improve their fill-factor and reduce cross talk between the pixels by redirecting and focusing the light onto the active detector regions..

2.3 Summary

In this chapter, I briefly explained the CMOS and CCD cameras and their architectures. Understanding the key advantages of these sensors is of great importance before comparing their performances and considering their use in biomedical applications. In the following chapter, I will examine the performance parameters given in the CCD and CMOS sensor and camera data sheets, then I will compare CMOS and CCD cameras and sensors that are available in the market and proposed in the literature for microscopic imaging.

3 Comparison of CMOS and CCD Camera

With the data provided in the camera and image sensor data-sheets, this part of the thesis aims to review different CMOS and CCD cameras in the literature and in the market after giving a detailed background on the performance parameters. The revision of the CMOS and CCD cameras available in the market or in the literature show us that a CMOS image sensor or camera can perform as good as a CCD image sensor or camera on various grounds and depending on the application specifications, the scientists should consider to use low-cost CMOS cameras instead of high-cost CCDs. Of course, this requires a good revision of different camera options specifically for each application, however it pays off with a serious reduction in the cost of instruments.

3.1 Introduction

Choosing the right camera for a specific application is a very difficult and complex task. It is not enough to understand the basics of CMOS and CCDs cameras and differences between them but this task also requires to have a detailed understanding and interpretation of the sensor and camera specifications. Only then, a straightforward comparison between different cameras can be made.

Since most of the biomedical imaging applications require good quality imaging in low light conditions, some performance parameters, e.g. spatial resolution, Quantum Efficiency (QE), Full-Well Capacity (N_{sat}), Noise Floor (NF), Signal to Noise Ratio (SNR), Dynamic Range (DR), and Digital Resolution are more important for good quality images than the others. Due to this reason, these parameters should be well covered before comparing different cameras' performance.

3.2 Performance Parameters of CCD and CMOS Image Sensors and Cameras

In this section, I intend to provide a detailed understanding and interpretation of the sensor and camera specifications.

Spatial Resolution The spatial resolution of a microscope system can be limited either by the pixel spacing (pixel size or pitch) of the image sensor or the optical resolution of the microscope. The optical resolution or the collection efficiency of the microscope is mainly defined by the Numerical Aperture (NA) of the microscope objective as well as the light emission wavelength of the sample [Castleman, 1993]. The NA of the objective lens is defined by

$$NA = n \times \sin\theta \tag{3.1}$$

where n is the refractive index of the immersing medium adjacent to the objective lens (1.0 for air and 1.515 for oil) and θ is the angular radius of the collection cone [Santiago et al., 1998]. This formula also explains why high-cost oil immersion objectives i.e, objectives with higher refractive index, are preferred for better resolution, i.e., higher NA.

The optical resolution limit of a microscopy system is called diffraction limit, which can be calculated by Abbe's diffraction limit formula [Abbe, 1873]

$$R_{optical} = 0.61 \times \lambda / n \sin\theta = 0.61 \times \lambda / NA. \tag{3.2}$$

where λ is the light emission wavelength and NA is the numerical aperture as defined above.

In order to match the optical and electronic resolution of a microscopy system, the required pixel size, i.e., pixel pitch, of a camera can be calculated by [Levoy et al., 2006]

$$PixelPitch = 1/2 \times R_{optical} \times Magnification \tag{3.3}$$

where the 1/2 factor comes from the Nyquist Limit Theorem, i.e., sampling theorem [Grenander, 1959].

Thus, if we consider a system with 100X magnification objectives with NA = 1.4 and λ = 550nm, the resulting optical resolution would become around 239 nm which is close to the theoretical limit and the required pixel pitch for this setup would be 10μm ($\frac{200nm \times 100}{2}$).

The smallest pixel size requirement occurs in case of the use of 4X magnification objectives, with an approximate NA of 0.2, resulting in theoretical resolution limit of 1.67μm. In order to achieve this theoretical limit, the required pixel size would be 3.35μm maximum ($\frac{1.67\mu m \times 4}{2}$). However, since a smaller pixel will result in lower dynamic range, it should be preferred to use

sensors with larger pixels and match the electronic and optical resolution by use of a higher magnification objection with high NA. However, the magnification of an image spreads the light out and decreases the intensity per pixel in proportion to $1/\text{Magnification}^2$ [Lichtman and Conchello, 2005]. However, as depicted by Eq.3.4, the light efficiency is also in proportion to NA with a factor of NA^4. This results in higher light efficiency with higher magnification objectives due to their increased NA and makes them more preferable in fluorescence imaging. The dependence of the light efficiency to NA and magnification can be represented by the following formula [Lichtman and Conchello, 2005]:

$$E \propto NA^4/\text{Magnification}^2. \tag{3.4}$$

Table 3.1: Spatial Resolution vs Pixel Pitch

Objective	Numerical Aperture	Theoretical Limit (Eq.3.2)	Required Pixel Pitch (Eq.3.3)	Efficiency (Eq.3.4)
100X (oil)	1.4	239nm	11.98µm	%0.038
60X (oil)	1.4	239nm	7.17µm	%0.106
60X	0.95	353nm	10.594µm	%0.022
40X (oil)	1	335nm	6.71µm	%0.062
40X	0.95	353nm	7.06µm	%0.05
20X	0.75	447nm	4.47µm	%0.07
10X	0.45	745nm	3.72µm	%0.041
4X	0.2	1.677µm	3.35µm	%0.01
2X	0.1	3.35µm	3.35µm	%0.025

Table 3.1 summarizes the relation between the pixel pitch and the diffraction limit for different objectives and NAs. According to this table, the smallest pixel pitch is required (3.35µm) only when lowest magnification objectives (2X or 4X) are used. As opposed, for higher magnification objectives, pixel pitches above 6.71µm would even be enough to reach the diffraction limit. For low light imaging applications, low magnification objectives should not be preferred, since they reach lower photon collection efficiency than the higher magnification objectives as shown in the table. For instance, an objective with 4X magnification and 0.2 of NA can only result in 0.01% efficiency while an oil-immersion objective, with 100X magnification with NA of 1.4 can result in 0.038% efficiency. This is a huge improvement especially for fluorescence live-cell imaging applications where the cells are under risk of phototoxicity i.e., cell cycle arrest or cell death [Hoebe et al., 2007], when the fluorophores are excited for a long time. Therefore, it is required to target highest possible collection efficiency in the microscopy system in order to keep the exposure time as low as possible [Frigault et al., 2009]. Moreover, the spatial resolution that can be reached with low magnification objectives (2X or 4X) is only 3.35µm, while imaging cell details would require much lower resolution than this. Thus, for low light biomedical imaging applications, 20X and higher magnification objectives should be chosen. This makes us to conclude that if we have the flexibility to change the pixel pitch of a design, we may reach better collection efficiency by using larger pixels when higher magnification objectives are used. However, despite the increased collection efficiency with larger pixels, and increased Dynamic Range (DR) and Signal to Noise Ratio (SNR), the

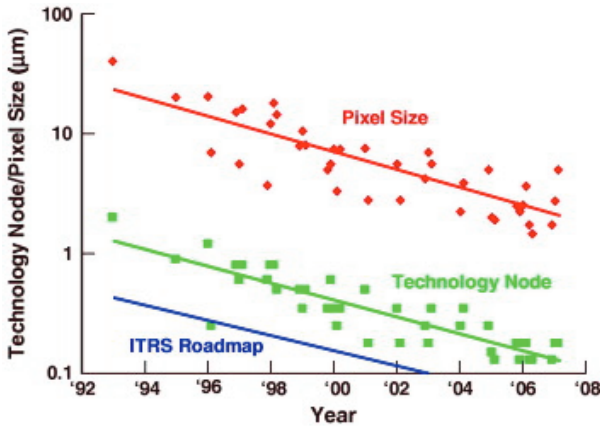


Figure 3.1: Evolution of pixel size, CMOS technology node used to fabricate the devices and the minimum dimension according to the ITRS Roadmap. [Theuwissen, 2008]

trend in the market currently involves the shrinking of the pixel sizes and increasing the number of pixels within the sensor [Theuwissen, 2008]. Fig. 3.1 presents this trend in the pixel dimensions, as well as the technology node, and the road map provided by the Information Technology Services (ITS) [Theuwissen, 2008].

Sensitivity Another important parameter for fluorescence imaging applications is the sensitivity of the sensor, which may be referred in different ways e.g. responsivity (units of V/lux.sec or Amps/Watt), minimum detectable light (in lux), or Quantum Efficiency (QE_λ). Responsivity (R_{ph}) in Amps/Watt is defined by the following formula, where I_L is the photo-current produced when a unit power of P_0 is present on the device.

$$R_{ph} = \frac{I_L}{P_0} \tag{3.5}$$

QE_λ, which refers to the fraction of photons incident on the detector surface that actually generate electrons, can be calculated by using the R_{ph} in the following formula:

$$QE_\lambda = \frac{I_L/e}{P_0/(h\nu)} = R_{ph}\frac{h\nu}{e} \tag{3.6}$$

where e represents the charge of an electron (elementary charge) and $h\nu$ is the energy of a single photon that is related to its wavelength by

$$h\nu = \frac{hc}{\lambda} \tag{3.7}$$

c: speed of light in a vacuum
h: Planck constant ($6.62606957 \times 10^{-34}$ J·s)
λ: photons wavelength

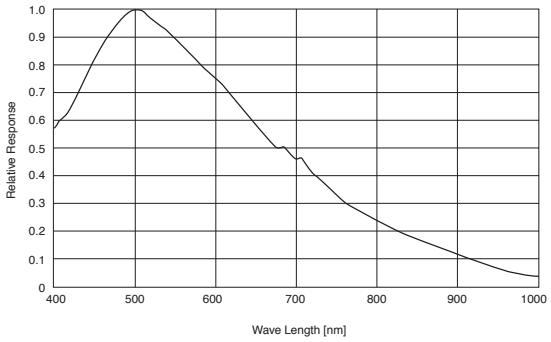


Figure 3.2: Spectral Sensitivity of Sony ICX274AL CCD sensor [Sony, 2014b]

In the literature and in the datasheets of the sensors, it is possible to find information about the sensitivity in all of these alternative ways, which usually makes it difficult to compare the performance of one sensor to another directly by referring to their datasheets.

Spectral Sensitivity Spectral sensitivity is the relative efficiency of a sensor as a function of the frequency or wavelength of the signal. It is not a metric that can be used for comparison purposes but it only provides a relative definition of the sensor response at different wavelengths. Most of the CCD and CMOS sensors are sensitive to the light ranges between 200nm-1000nm and they make a peak at a specific wavelength as in Fig. 3.2. That is why, in a fluorescence imaging application, according to the targeted fluorochromes, the most appropriate sensor should be chosen or if the camera is already in hand, if possible the fluorochrome should be chosen according to the peak wavelength region of the camera sensor.

Digital Resolution The digital resolution parameter, given in Digital Number (DN), is a specification given in the camera data sheets for CCDs and in the both sensor and camera data sheets for CMOS devices. It most commonly is defined according to the noise floor of the device. Knowing the digital resolution of two cameras, it can be approximately said that a camera with higher digital resolution has less noise. However, this statement cannot be proven until the noise floor is stated in the camera data-sheet or noise measurements are done by the users. In addition, it is common to see in some cameras that ADCs with more than necessary digital resolution have been used, although the noise floor of the sensor is higher than the voltage precision of the ADC.

Noise, Signal-to-Noise Ratio (SNR), and Dynamic Range (DR) Read noise or noise floor, SNR, and DR are given in most of the camera data-sheets as another definition for the sensitivity of the camera.

The Read Noise (n_{read}) or the Noise Floor (NF) parameters refer to the sum of all detectable

noise sources in a camera and define the minimum detectable signal level. SNR defines the ratio between the signal and noise floor of the camera. In the datasheets, SNR may be given as minimum, typical or maximum, where in some cases, the definition of these ranges are not defined or in others the typical SNR refers to the DR. Thus, the Dynamic Range (DR) parameter is more reliable than the given SNR since it defines the limits of the sensor and is formalized as follows:

$$DR = 20.\log_{10}(N_{sat}/n_{read}) \tag{3.8}$$

where N_{sat} represents the signal electrons in saturation level (defined by the full-well capacity) and n_{read} represents the total read noise in electrons.

As mentioned earlier, the noise sources for a CMOS sensor and a CCD sensor are different. The noise sources in CMOS image sensors are divided into three: temporal noise, input-signal noise, and spatial noise.

The time-dependent pixel noise is called temporal noise and it includes
1- reset or kTC noise
2- thermal noise or Johnson noise
3- 1/f noise or flicker noise
4- dark current shot noise
5- photon shot noise
5- quantization noise
6- phase noise or timing jitter

The temporal noise is “frozen” as spatial noise when a snapshot is taken. The spatial noise sources include
1- dark Fixed Pattern Noise (FPN)
2- light FPN
3- leakers or hot spots
4- defect pixels
5- cosmetic defects
and these noises are fixed per pixel, per column or per chip.

As opposed to CMOS sensors, CCD sensors only include dark signal and shot noise. The read-out noise is not a part of the CCD sensor but is a part of the CCD camera. Thus, the noise performance of CMOS and CCD sensors cannot be compared but the camera data-sheets should be used for comparison purposes as mentioned earlier.

In microscopic imaging, for short exposures, read noise dominates the noise in the images and for longer exposures, thermal noise usually becomes the dominant factor. Thermal noise results from noise in dark current, and the noise value is the square root of the number of dark-current generated electrons. In order to reduce the thermal noise, most of the high quality

imaging devices are integrated with cooling systems which results in higher performance. Thus, the noise performance of the cooled cameras for both CCDs and CMOS will largely differ from the normal cameras, due to the reduction of the thermal noise with cooling.

Although these parameters are very important to compare different cameras, it should be noted that they never provide a true comparison metric since they highly rely on the measurement conditions.

Sensor Full-Well Capacity The property that describes the capacity to hold the electrons in each pixel that are generated from photons is called the Full Well Capacity (N_{sat}). A larger pixel can hold more number of electrons with a trade-off in spectral resolution depending on the pixel design. However, by staying within the limits of the diffraction, the largest possible pixel (photo device) should be implemented for increased well capacity, which is important for both maximum SNR and larger DR. However, it should be noted that there is also a trade-off between the CMOS pixels' N_{sat} and the Conversion Gain (CG). This dependence will be explained in more detail in Section 5.2.1.

In the following section, I will present a review of the existing sensor and cameras in the market and in the literature, which are appropriate for microscopy (biomedical) imaging applications.

3.3 Comparison of CMOS and CCD Cameras

In this section, I present different CMOS and CCD cameras that are recommended for microscopic applications, which are currently available in the market or in the literature. CCD cameras are represented in two different tables for IL-CCD type cameras and EM-CCD cameras. CMOS cameras are also grouped under two different tables for sCMOS and standard CMOS cameras. Although there is no share in the microscopic imaging market, the standard CMOS cameras/sensors in the market and in the literature are reviewed to show that these sensors also provide good performance and may be preferred depending on the application.

Table 3.2 presents a summary of CCD cameras that are sold by different well-known suppliers in microscopy market and they are grouped under each supplier. In this table, I marked the best performance for each parameter in red. All these CCD cameras recommended for microscopic applications use the IL-CCD architectures to support continuous imaging as stated earlier and are integrated with micro-lenses to improve the sensitivity. As seen in the table, most of the sensors of these cameras are manufactured by Sony. Moreover, Sony's ICX285AL [Sony, 2014c] sensor is the most common sensor choice of all the microscopy manufacturers for fluorescence imaging due to its high QE. However, according to Table 3.2, Hamamatsu ER-150 [Hamamatsu, 2014a], which is recommended by Olympus Corporation, has higher QE (above 70%) than ICX285AL sensor. This sensor from Hamamatsu also reaches the minimum NF ($6e^-$), highest full-well capacity ($36000e^-$) (although it has the same pixel pitch as ICX285AL), digital resolution (12/16), and DR (71dB). In addition, surprisingly although Sony ICX414AL

[Sony, 2014d] has a larger pixel pitch (9µm) than Hamamatsu ER-150, Hamamatsu ER-150 has still higher full-well capacity. As mentioned earlier in the spatial resolution section, all these sensors reach the minimum diffraction limit when the objectives for highest efficiency are chosen. In that case, there is no benefit of reducing the pixel pitch as it is the case of Sony ICX274AL sensor [Sony, 2014b], which reduces the full-well capacity as well as the light sensitivity.

Table 3.2: IL-CCD Camera Examples Currently Available in the Market for Microscopic Applications

Provider (Model)	Sensor Model	Pixel Pitch (µm)	QE(max) (%)	N_{sat} (e^-)	NF (e^-)	DR (dB)	DN (bits)
ZEISS							
Axiocam HSm [1]	ICX414AL [2]	9	≈ 45 [3]	32000 [1]	17 [1]	65 [1]	12 [1]
Axiocam ICm 1 [4]	ICX267AL [5]	4.65	≈ 45	10366 [6]	11.48 [6]	59.11 Eq.(3.8)	12 [4]
Axiocam MRm [7]	ICX285AL [9]	6.45	≈ 64 [3]	17000 [7]	<7.7 [7]	>66.8 [7]	12 [7]
NIKON							
DS-Qi1 [8]	ICX285AL [9]	6.45	≈ 64 [3]	17000 [8]	8 [8]	66.5 Eq.(3.8)	12 [8]
DS-Vi1 [10]	ICX274AL [12]	4.4	54 [3]	7969 [6]	8.35 [6]	60 [6]	12 [10]
OLYMPUS							
XM10 [11]	ICX285AL	6.45	≈ 64 [3]	17000	<10 [11]	64.6 Eq.(3.8)	14 [11]
ORCA-R2 [18]	ER-150	6.45	>70	36000 [15]	6 [15]	71 [15]	12/16 [15]
LEICA							
DFC365 [16]	ICX285AL [13]	6.45	≈ 64 [3]	18000 [16]	6 [16]	>69 [16]	14 [16]
DFC345 [17]	ICX274AL [12]	4.4	54 [3]	15000 [17]	<14 [17]	60 Eq.(3.8)	8/12 [17]

References:
[1][Zeiss, April, 2005a], [2][Sony, 2014d], [3] [PointGrey, Jul, 2010a], [4][Zeiss, April, 2005b], [5][Sony, 2014a], [6][PointGrey, Jul, 2010b]
[7][Zeiss, April, 2005c], [8][Nikon, 2014a], [9][Sony, 2014c], [10][Nikon, 2014b], [11][Olympus, 2014b], [12][Sony, 2014b], [13][Sony, 2014c]
[14][Hamamatsu, 2014a], [15][Olympus, 2014a], [16] [Leica, 2014b], [17] [Leica, 2014a], [18] [Olympus, 2014a]

Table 3.3: EMCCD Camera Examples Currently Available in the Market for Microscopic Applications

Provider (Model)	Sensor Model	Pixel Pitch (µm)	QE(max) (%)	N_{sat} (e^-)	NF (e^-)	DR (dB)	DN (bits)
Hamamatsu	ImagEM X2 [1]	16 [1]	>90 [1]	370k [1]	<1 [1]	>110 Eq.(3.8)	16 [1]
Andor	iXon 897 (BSI) [2]	16 [2]	>95 [2]	180k [3]	<1 [2]	105 Eq.(3.8)	16 [2]
Photometrics	Evolve 512 Delta [4]	16 [4]	>95 [4]	≈ 200k [5]	<1 [4]	106 Eq.(3.8)	16 [4]

References:
[1][Hamamatsu, 2014c], [2][Andor, 2014b], [3] [Andor, 2014a], [4][Photometrics, 2014a], [5][Photometrics, 2014b]

Table 3.3 shows three examples of EMCCD cameras. As mentioned earlier, these cameras are fully compatible with regular CCDs and they can be used in two working modes. These cameras should be considered for very high speed low light applications especially in live cell imaging. They offer increased QE compared to regular CCDs as well as below 1e^- read noise even for frame rates above 10000 frames/s. All these EMCCD cameras provide superior performance in terms of QE and full well capacity compared to both standard CCDs and CMOS cameras. Due to the huge increase in the full-well capacity, these cameras reach above 100dB DR which is mainly due to the high pixel pitch of these devices. However, it should be noted that none of the CCD and CMOS cameras that are presented here have pixel pitches as high as the EMCCDs (16µm).

Table 3.4: sCMOS Camera Examples Currently Available in the Market for Microscopic Applications

Provider (Model)	Sensor Model	Pixel Pitch (µm)	QE(max) (%)	N_{sat} (e^-)	NF (e^-)	DR (dB)	DN (bits)
NIKON							
Andor Zyla	4.2 (FSI) [1]	6 [1]	72 [1]	30000 [1]	0.9 [1]	90.45 Eq.(3.8)	12/16 [1]
Andor Zyla	5.5 (FSI) [1]	6.5 [1]	60 [1]	30000 [1]	1.2 [1]	87.95 Eq.(3.8)	12/16 [1]
OLYMPUS							
ORCA-Flash2.8 [2]	Ham. FL-280 [2]	3.63 [2]	≈ 68 [2]	18000 [2]	3 [2]	89.54 Eq.(3.8)	12 [2]
QImaging optiMOS [3]	BAE CIS1910F [3]	6.5 [3]	55 [3]	30000 [3]	1.5 [3]	86.02 Eq.(3.8)	16 [3]
PCO AG							
Edge Gold 5.5 [4]	CIS2521	6.5 [4]	>65 [4]	30000 [4]	0.8 [4]	91.48 Eq.(3.8)	16 [4]
Edge Gold 4.2 [5]	CIS2020 [5]	6.5 [5]	>70 [5]	30000 [5]	0.9 [5]	90.45 Eq.(3.8)	16 [5]
Edge Gold 5.5 [6]	CIS2521 [6]	6.5 [6]	>60 [6]	30000 [6]	1.1 [6]	88.71 Eq.(3.8)	16 [6]
Raptor Photonics							
Osprey [7]	CMOSIS sCMOS[7]	5.5 [7]	>63 [7]	12000 [7]	<7 [7]	65 [7]	12 [7]

References:
[1][Andor, 2014a],[2][Hamamatsu, 2014b],[3][Qimaging, 2014a],[4][PCO, 2014c],[5][PCO, 2014b],[6][PCO, 2014a],[7][Raptor, 2014]

Table 3.5: CMOS Image Sensor/Camera Examples Currently Available in the Market and in the Literature

Provider (Model)	Sensor Model	Pixel Pitch (µm)	QE(max) (%)	N_{sat} (e^-)	NF (e^-)	DR (dB)	DN (bits)
Aptina	MT9P031 [1]	2.2	60	NA	NA	NA	12
Aptina	AR0130 [2]	3.75	78	NA	NA	NA	12
QImaging Rolera Bolt [3]	Sony IMX035	3.63	≈ 65	17000	3	75.06 Eq.(3.8)	8/12
Point Grey Flea3 [4]	Sony IMX035	4.8	>77	15491	6	67.55	12
Point Grey Flea3 [4]	On Semi VITA1300	3.63	61	10226	26.26	51.64	12
Point Grey Flea3 [4]	e2v EV76C560	3.63	59	8384	25.14	50.29	12
Point Grey Flea3 [4]	Sony IMX036	3.63	67	10066	6.71	62.9	12
Literature[5]	R. Johansson et al.	1.75	53.3	NA	1.88	NA	11
Literature[6]	Y. Chae et al.	2.25	NA	NA	1.9	NA	12-14
Literature[7]	M. Seo et al.	7.5	NA	NA	1.2	NA	13-19

References:
[1][Aptina, 2014b], [2][Aptina, 2014a], [3][Qimaging, 2014b], [4][PointGrey, Jul, 2010c],[5] [Johansson et al., 2011],[6] [Chae et al., 2010], [7][Seo et al., 2012]

After the long history of CCD cameras, CMOS cameras have recently become very popular in the microscope imaging market with Scientific CMOS (sCMOS) cameras. Before that, none of the microscopy manufacturers provided CMOS cameras, which would make sense to use for some applications due to a huge cost reduction. In Table 3.4, performance of the sCMOS cameras that are available in the market are presented. Among all, Andor Tecnlogy's Zyla FSI 4.2 [Andor, 2014a] camera has the highest quantum efficiency (%72), highest full-well capacity (30000e^-), almost the lowest read noise (9e^-), and highest DR (90.45dB). PCO AG's Edge Gold 5.5 [PCO, 2014c] sCMOS camera also provides similar to the previous one, only with a slightly less quantum efficiency. The performance of all the listed sCMOS cameras are better than the CCD cameras presented in Table 3.2 and slightly lower than the EMCCD cameras presented in Table 3.3 in terms of QE, full-well capacity, and as a result DR. However, as mentioned earlier, since there are no sCMOS cameras providing pixel pitches as high as the ones of the EMCCDs (16µm), the full-well capacity and dynamic range parameters cannot be compared for these

two different type of cameras. In fact, by increasing the pixel-pitch in sCMOS cameras, it should be evident to increase the full-well capacity and the DR; this is of course a matter of application, requirement, and market demand.

Finally, although there is no microscopic imaging market share, in Table 3.5, performances of the standard CMOS image sensors that are available in the market and in the literature are presented. In terms of spatial resolution, read noise, QE, and digital resolution, it is seen that these CMOS image sensors can also perform as good as standard CCD cameras. Moreover, by empowering the standard CMOS camera images with image processing algorithms, it has been shown that CMOS cameras can also be used for low-light imaging of fluorescence samples [Köklü et al., 2013b].

3.4 Summary

The comparison tables above have shown that sCMOS cameras perform as good as EMCCDs and much better than standard CCDs. There is no doubt that, for very high quality imaging applications both EMCCDs and sCMOS cameras can serve very well. Only if the target application requires very high DR and N_{sat}, EMCCDs may be preferred since the EMCCD cameras that are currently available in the market offer larger pixels than sCMOS cameras. However, sCMOS cameras are also quite costly like EMCCDs and CCDs and they are not appropriate for applications, where the target is to reach low cost biomedical imaging devices. That is why standard CMOS alternatives should be considered for such applications. Still, as seen in the tables above, standard CMOS cameras perform similar to standard CCDs and with a special attention on the noise reduction and the target molecule extraction, these detectors may be good enough to analyze the samples and make quantitative measurements.

In the following chapter, in order to show the reliability of standard CMOS cameras in microscopy, I make a comparative study of a standard CMOS and a CCD camera by acquiring images of different fluorescent samples with both of these cameras. In order to improve the quality of the collected images, I benefit from different image processing algorithms especially to reduce the noise in the collected images and to improve the visibility of the target molecules.

4 Comparative Fluorescence Imaging Study of a CMOS and a CCD Camera

The target of this chapter is to provide a proof-of-concept in the sense that standard CMOS cameras provide comparable results with CCDs and can be used even for low-light microscopy applications despite their low-cost. This chapter does not aim to make a comprehensive image processing study but uses the widely known processing algorithms to draw a conclusion. I introduce an application-based comparative study between the default CCD camera of an inverted microscope (Nikon Ti-S Eclipse) and a CMOS camera that I have built by using a CMOS image sensor that is available in the market. This study clearly provides a more reliable conclusion than a straightforward comparison based on the camera data-sheets.

4.1 Introduction

In this chapter, I imaged different fluorescent samples by using a conventional inverted microscope, Nikon Eclipse Ti (Nikon Instruments, Inc. Melville, N.Y.) integrated with a CMOS and a CCD camera. The chosen CCD camera has been widely sold by Nikon for conventional microscopy applications and the CMOS camera includes a mid-performance CMOS image sensor (Micron-MT9V032 [Aptina, 2014c]) and an FPGA platform. For this experiment, I used real cell samples such as breast cancer diagnostic tissue cell and Caco-2 cell samples.

In the following sections, first, I describe the process of building a CMOS camera and then, compare the CMOS camera with the commercially available Nikon CCD camera. Then, I present image processing algorithms that are used in this experiment such as noise reduction, auto-thresholding, image registration, and image resizing. Finally, I explain the biological fluorescent samples in detail and show their comparative results with collected and processed images.

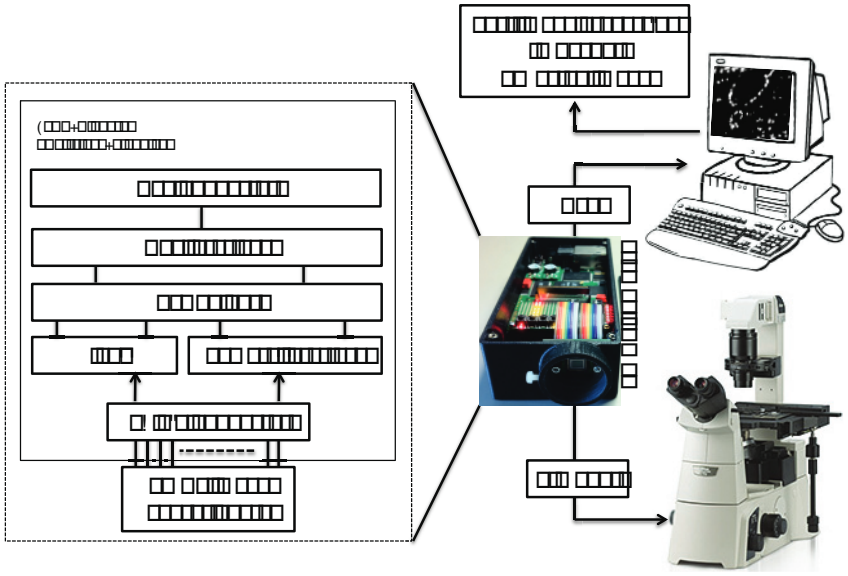


Figure 4.1: System Level Representation of Image Collection by CMOS Camera

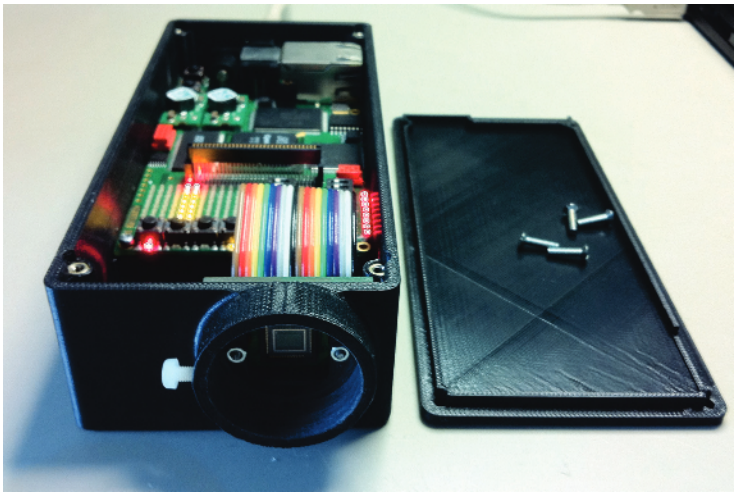


Figure 4.2: Self-made CMOS Camera

4.2 Fluorescence Imaging System with a Custom-Designed CMOS and a CCD Camera

Fig. 4.1 represents a block diagram of the entire fluorescence imaging system with the CMOS camera that I have built. A more detailed picture of this CMOS camera is shown in Fig. 4.2, where the CMOS image sensor and the FPGA4U [Favi et al., 2009] board is visible.

The CMOS camera enclosure integrates a control unit, i.e., FPGA platform, and a CMOS sensor, i.e., Micron-MT9V032 [Aptina, 2014c], inside one case and has two openings from the back and the front, where the former is for the USB connector and the latter is for interfacing output

Table 4.1: Comparison of CMOS and CCD Cameras Used in this experiment

	Nikon CCD Camera	CD CMOS [Aptina, 2014c]
Sensor	Sony ICX274AL [Sony, 2014b]	MT9V032 [Aptina, 2014c]
Optical Format (in)	1/1.8	1/3
Pixel Size (µm × µm)	4.40 × 4.40	6.0 × 6.0
Sensor Area (H × V)(mm^2)	57.8	12.99
Number of pixels (H × V)	1628 × 1236	752 × 480
Dynamic Range (dB)	56	55
Quantum Efficiency (QE) @515nm	%54	%44
Pixel Read Noise (e^-)	12	25
Digital Output bits	8/12	10
Price CHF	11490	1949 [Lumenera, 2014]

CCD Camera CMOS Camera

optics of the microscope using a C-mount system. The screw on the left side of the C-mount system is used to adjust coarsely the depth of focus.

As seen in Fig. 4.1, the camera system includes an FPGA4u board and a Printed Circuit Board (PCB) specifically built for this CMOS image sensor (Micron-MT9V032 [Aptina, 2014c]). The FPGA4U board includes a USB interface, which allows the connection of the board to a computer in order to both program the CMOS sensor and transfer the collected images. I later post-processed the collected images by using MATLAB software. The image sensor in the camera is a mid-performance black and white CMOS image sensor with 752 × 480 active pixels and 10 bits Analog to Digital Converter (ADC) resolution [Aptina, 2014c]. The sensor is connected to the FPGA board through a 20 pin connector, which carries the Inter-Integrated Circuit (I^2C) bus and the camera control signals. The I^2C interface is used to configure the internal registers of the sensor and more specifically the exposure time and analog gain for this application. I used the Altera Design Software to write the VHDL codes for the camera control and synchronization units and to test them.

Table 4.1 provides a comparison between the CMOS camera that I have built and the CCD camera that is bought from the market. According to this table, obviously, the CCD camera is expected to result in better quality images due to its higher QE and lower NF. However, as seen in Chapter 3, much better performing standard CMOS or sCMOS sensors from the market can also be chosen depending on the application [Aptina, 2014b], [Aptina, 2014a]. Since I have built the CMOS camera and it is not from the market, I estimated the cost of this camera based on a camera with similar performance that is available in the market. According to this estimation, the CMOS camera costs almost one order of magnitude less than the CCD. Moreover, since our CMOS camera is integrated with an FPGA platform, it not only allows a low cost replacement of the CCD camera but also provides a highly flexible and re-programmable

camera unit. It also supports the implementation of additional functionality and possibly image processing algorithms directly and rapidly on board.

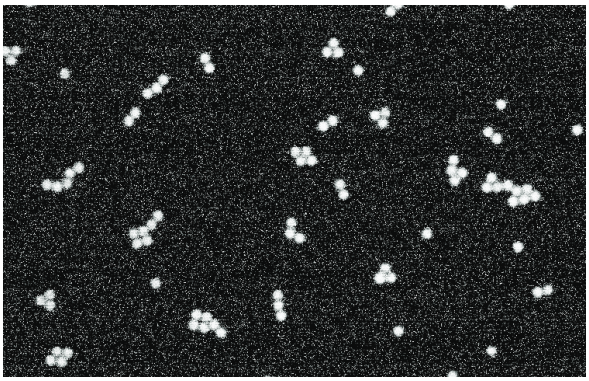
4.3 Noise Removal

Image sensors suffer from several fundamental and technology related non-idealities that limit their performance[El Gamal and Eltoukhy, 2005]. The goal of many conventional fluorescence microscopy imaging is to deal with low light emitting samples and applications. This is why noise contributors should be dealt with by reducing their impact on the useful signals. In most of the microscopy software, no matter which type of camera is being used, images are post-processed to remove most of the noise sources. Thus, the scientists who are willing to use standard CMOS cameras and to reduce the cost of their instruments, should post-process their collected images by one or more of the below algorithms.

CMOS imagers are known to suffer from various noise sources which can be classified either as temporal noise or Fixed Pattern Noise (FPN) [Bigas et al., 2006]. Temporal noise, as defined in Section 3.2 results from a stochastic process and cannot be fully determined nor mitigated for every pixel and it sets the ultimate limit on signal fidelity [El Gamal and Eltoukhy, 2005]. However, the FPN is not a function of time and can be determined. It forms a constant pattern among the pixels/columns of the image sensor. This problem arises from small differences in the individual responsivity of the pixels or the column amplifiers that are mostly caused by non-homogeneity in the manufacturing process.

4.3.1 Fixed Pattern and Temporal Noise Reduction for Standard CMOS Camera Images

The FPN is generally divided into two components: offset FPN and gain FPN. Offset FPN can be due to device mismatches in active circuits (Q_{FPN}) and dark current variability which is referred as Dark Signal Non-Uniformity (DSNU) (Q_{DSNU}). In a CMOS image sensor, Q_{FPN} is corrected at the circuit level, usually in column level, by use of the Correlated Double Sampling (CDS) or the Delta Double Sampling (DDS) circuits. With this method, each pixel output is sampled twice and registered on capacitors; once when the pixel is under reset and once after the integration. At the end of this double sampling phase, the pixel value after integration is subtracted from the pixel value after reset, which suppresses the offset FPN (Q_{FPN}). The CDS technique also suppresses the reset transistor related noise in active pixel sensors as will be explained in Chapter 7, Section 7.2.5. However, some of the Q_{DSNU} still remains after this circuit level noise reduction process and it can be the main performance degradation source for CMOS image sensors especially under low light levels. That is why Q_{DSNU} is usually dealt by calibrating the sensor in dark before taking the useful images. However, since Q_{DSNU} is due to the variation in dark current, which highly relates with temperature, it is not easy to fully calibrate this noise since the temperature of the device also varies in time especially in non-cooled cameras.



(a) Raw Image: original image of fluorescence micro-beads including dark signal non-uniformity

(b) Master Dark Frame: averaged image of multiple images when camera is under dark

(c) Corrected Image:image achieved after the subtraction of master dark frame from the raw image

Figure 4.3: DSNU Noise Elimination (Contrast and Brightness Increased Images)

Thus, DSNU is an offset related FPN and it is due to the offset between pixels in dark, is independent of the pixel signal, and varies with temperature. In addition to offset related FPN, there is also gain related FPN which is seen as a responsivity variation among pixels under illumination and it increases with the signal level. This type of FPN is called Photo Response Non-uniformity (Q_{PRNU}). Since Q_{PRNU} increases with the signal level, this type of noise becomes more important at high illumination levels but not at low light imaging. This is why, the Q_{DSNU} is more of a focus for fluorescence imaging than the Q_{PRNU} and will be dealt with the following method.

When the light intensity received by the CMOS sensor through the fluorescence microscope is weak, it is required to program the CMOS image sensor at high exposure time and analog gain. This causes a huge FPN to appear and a classic method to mitigate part of the DSNU is applied on the CMOS images [Schöberl et al., 2009] .

First of all, a Master Dark Frame (MDF) is generated by computing the median or the average frame out of a set of N dark frames. Second, the MDF is subtracted from any regular captured raw frame (F_{raw}) at the same exposure and gain as the MDF. This technique is similar to the circuit level noise reduction techniques (CDS and DDS) and can be considered as the off-chip version of these techniques. The de-noised frames can be computed using;

$$F_{corrected} = max(0, F_{raw} - MDF). \tag{4.1}$$

In order to have the sensor temperature stable during the calibration process (since the Q_{DSNU} varies with temperature), the system is kept “on” for a few minutes before capturing the dark frames. The result of this FPN removal is depicted in Fig. 4.3, where the CMOS camera is exposed to light for around 320ms with an analog gain of 7x.

In high-end cameras, Q_{PRNU} and Q_{DSNU} are usually calibrated by interpolating the data written in the sensor memory as a reference, i.e., the Q_{PRNU} is calibrated as a gain property, by multiplying each pixel signal with a factor stored for that pixel in a memory [Purll, 1984]. However, this calibration usually needs to be re-calibrated after a short period of time due to the changes in the level of background flux or temperature [Scribner et al., 1991]. Thus, this type of reference-based calibration techniques are later replaced by adaptive/dynamic scene-based non-uniformity correction techniques, which eliminate the need for re-calibration [Scribner et al., 1991] and the halt of the normal operation of the system [Torres et al., 2003], by continuously updating the correction coefficients based on radiance levels of the scene being viewed [Scribner et al., 1991]. In the literature, more algorithms on the scene-based techniques may be found, which is important especially in live-cell imaging [Scribner et al., 1991],[Torres et al., 2003],[Vera and Torres, 2005].

Finally, as stated earlier, temporal noise is a function of time and includes different noise sources such as photon shot noise, pixel reset circuit noise, readout circuit thermal and flicker noise, and quantization noise. By collecting multiple images and averaging the collected

images, temporal noise can be reduced but not fully eliminated.

4.3.2 Removal of Hot Spots/Pixels and Dead Pixels

There are dead and hot pixels in every CMOS and CCD camera. The amount of these defective pixels depends on temperature, technology, design, layout, and micro-lenses. They may also appear due to aging of the sensor. Hot pixels generate higher leakage or dark current than normal. When an image is taken under long-exposure time, longer than causing the pixel exceeding its linear charge capacity, they appear as bright spots and cause salt and pepper type noise on the image. This type of noise cannot be removed by MDF generation and subtraction, since they are only visible at high exposure time with light present on the sensor. On the other hand, dead pixels are unresponsive stuck pixels and no matter what the light intensity or exposure time, they do not respond to light. A common method to remove hot pixels or dead pixels is replacing them by the median value of the surrounding pixels. This remapping operation can be done by MATLAB median filtering, medfilt2 operand [Lim, 1990], or by an outlier removal algorithm. For this experiment, I used the following outlier removal algorithm;

$$\Delta = (|I_{ij} - m|) \tag{4.2}$$

$$\forall i \in [1,v], \forall j \in [1,h] : I_{i,j} = \begin{cases} m & \text{if } \Delta > Th, \\ I_{ij} & \text{else.} \end{cases} \tag{4.3}$$

I: Intensity value of a pixel
h: Number of pixels at the horizontal direction
v: Number of pixels at the vertical direction
Th: Intensity threshold
window: Defined array size (radius × radius).
m: Median value of the intensity values of pixels in a certain window around the chosen pixel I_{ij}
If the Δ value is above a defined threshold (Th), the intensity value of the chosen pixel (I_{ij}) is replaced by the calculated median (m) and else the pixel value is kept as it is. This method can be applied for both hot and dead pixels. Hot pixels are the pixels that exceed the level of the brightest neighboring pixel by more than the Th and the dead pixels are the pixels that are darker than the darkest neighboring pixel by more than the Th. In both cases, they are replaced by the median of the surrounding pixels.

Thus by using the algorithms mentioned above on the collected images, the temporal noise and the FPN can be reduced and the hot and the dead pixels can be removed, which results

in enough good quality images to do quantitative analysis by using standard low-cost CMOS cameras.

4.4 Image Processing Algorithms

4.4.1 Morphological Pattern Localization

In addition to the noise removal algorithms, for the localization of the target molecules and to be able to make quantitative calculations, Otsu's auto-thresholding algorithm [Otsu, 1975] is commonly used. Thus, for the experiments that are stated in this section, I used automatic thresholding method introduced by N.Otsu [Otsu, 1975] by using MATLAB's graythresh function.

During the thresholding process, individual pixels in an image with an intensity value larger than a defined threshold value are converted to 1 ("object" pixels), where all the other pixel values below this threshold are converted to 0 ("background" pixels).

Otsu's thresholding method is a nonparametric method automatically selecting a threshold level for a gray-level image based on its histogram. The algorithm considers the image to be thresholded consisting of two classes of pixels as foreground and background and tries to achieve a thresholding value which minimizes the intra-class variation while at the same time allowing the maximization of the inter-class variation.

Shortly, the algorithm aims to select a threshold by maximizing a criterion measure that evaluates the "goodness" of that threshold. The original mathematical formulation and discussion can be found in [Otsu, 1975]. The following presents few equations for understanding Otsu's automated processing concept.

The only input of the method is the normalized gray-level histogram of the image, which can also been seen as a probability distribution. The algorithm is aiming at solving an optimization problem by maximizing the "goodness" of the threshold. Given a threshold value, the L bins of the histogram can be grouped in two classes; C_0 gathering the bins indexed by $[0,..,k-1]$ and C_1 gathering the bins indexed by $[k,..,L-1]$. The gray level corresponding the bin k corresponds to the selected threshold.

Finding the optimal threshold k* is reduced to solving

$$\max_{S^*} \left[\sigma_B^2(k) \right] \tag{4.4}$$

where S* is the range of k over which the maximum is sought

$$S^* = \{k; \omega_0 \omega_1 > 0, or, 0 < \omega_0 < 1\} \tag{4.5}$$

and σ_B^2 is referred to as the between-class variance defined by

$$\sigma_B^2 = \omega_0\omega_1 \left[\mu_1 - \mu_0\right]^2 \tag{4.6}$$

for which ω_0 and ω_1 are the probability of class occurrences and μ_0 and μ_1 and the class mean levels.

4.4.2 Image Registration

The last phase, before comparing the two camera images is registration and resizing of the images in order to make a fair comparison between these two cameras, which have different array size, pixel pitch, and digital resolution.

Image registration is the process of aligning the pixels of two or more images of the same scene when one image is considered as a reference. In this experiment, the image registration algorithms basically include rotation, cropping, resizing ,and intensity scaling. Below are the steps that I used for the registration of the CCD camera images to the CMOS camera images in order to reach highest correlation between the two.

1) Rotation of the image to solve the low or high angles of tilt issues that may appear when mounting the cameras (with MATLAB's imrotate function).

2) Cropping of the CCD camera image to reach same area of interest with the CMOS camera image. In this experiment, MATLAB's imcrop function is used to crop the CCD camera image of 1628×1236 according to the field of view of the CMOS camera image and finally an image with an array size of 989×631 is reached.

3) Re-sizing/ Scaling of the CCD camera image. The scaling factor for horizontal and vertical directions should be calculated separately depending on the size of the each camera pixel. In this experiment, both of the camera pixels are in square shape which results in the same horizontal and vertical scaling factors. The scaling factor is calculated by dividing the CMOS pixel size to the CCD pixel size which is 1.3159 (CMOS pixel size / CCD pixel size = 5.79μm / 4.4μm = 1.3159). By using the scaling factor, the cropped CCD image of 989×631 is re-sized to an image with an array size of 752×480.

4) Intensity Scaling. Since the CMOS camera has 10 bits resolution and the CCD has 12 bits, their intensity is represented differently in the images. Thus, the CCD camera images are downgraded for a fair comparison between the two.

4.5 Fluorescence Imaging of Tissue and Caco-2 Cell Samples

In this section, the image processing algorithms explained in the previous section are applied on the CMOS and/or CCD camera images step by step. First, due to the high exposure time in

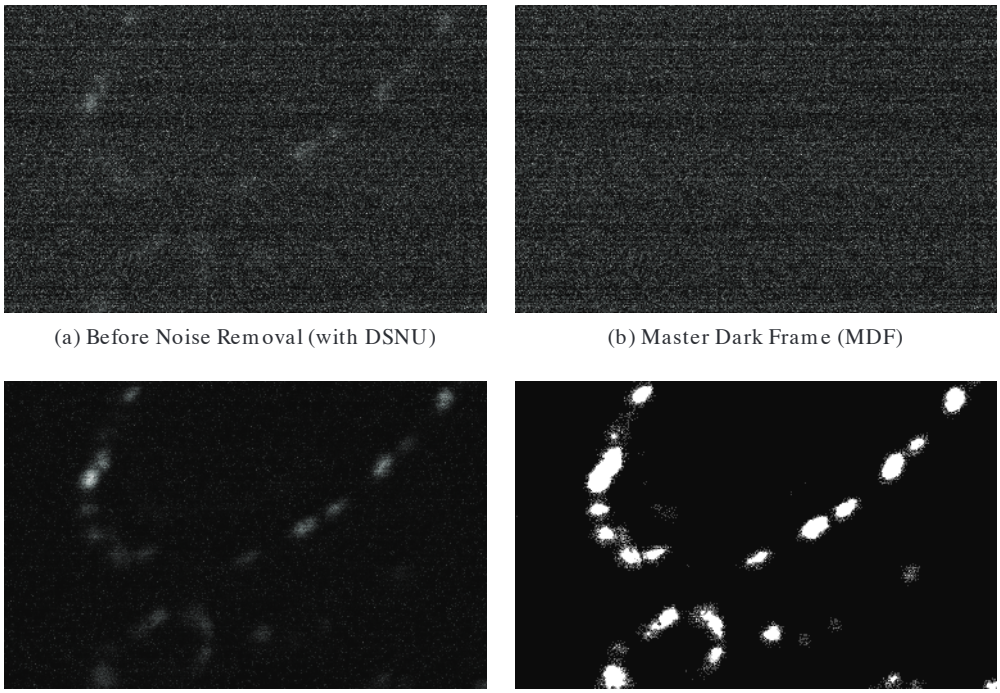
CMOS camera, FPN noise becomes critical. Thus, I applied FPN noise reduction algorithm on both Tissue and Caco-2 cells' CMOS camera images. Second, to remove both hot and dead pixel outliers which are numerically distant from the surrounding pixel values on the image, I used an outlier removal algorithm on the CMOS and CCD camera images. Later, I applied auto-thresholding algorithm for both camera images for quantitative calculations and comparison as well as for better visibility of the morphological patterns expressed on the cells. Finally, I registered and resized the CCD camera images according to the CMOS camera images since the two cameras have different resolution and pixel pitches. With this method, the CCD images of 1200V × 1600H are converted to images of 480V × 752H. In order to keep the experimental setup the same for both cameras, the same light intensity (Neutral Density (ND) Filter= 1) and microscope optics and objectives (40X, Numerical Aperture=0.75) are used for both camera image acquisitions. The light emitted from the Estrogen Receptor (ER) expression in tissue cells and the Gabdh expression in Caco-2 cells both emit very low light intensity. That is why the samples have been imaged at very high exposure time (1s) and analog gain (8X/ 16X) for both camera experiments.

4.5.0.1 Tissue Sample Imaging

The sample is a breast cancer diagnostic sample that the nuclear Estrogen Receptor (ER) expression is marked with fluorescence light at 665nm. ER is detected by indirect immunohistochemical reaction [Song et al., 2009], [Ciftlik et al., 2010] using monoclonal mouse anti-human anti-ER receptor antibody as primary antibody (clone 6F11, Leica Microsystems) and Alexa-Fluor 647 conjugated goat anti-mouse polyclonal IgG antibody (Invitrogen) as secondary anti-body. First, I subtracted the MDF in Fig. 4.4b from the CMOS camera row images (Fig. 4.4a) and obtained the corrected image as seen in Fig. 4.4c. I enhanced the contrast of the image to increase the visibility of hot pixels/spots. Later, I used outlier removal algorithm on this image.

In order to compare the intensity distribution of the two camera images, I extract the histogram of the same row of the gray-scale images and obtained the data in Fig. 4.5a and Fig. 4.5b. In this plot, X axis represents the intensity values distributed over 65536 values and the Y axis represents the pixel counts corresponding to that specific intensity. For clarity purposes, the black pixels at 0 level intensity are left out of this graph and so the rest of the graph represent the biological information on the images. According to these figures, large majority of the pixels fall at low level intensities in both images since they are predominantly dark and the tissues show a large intensity distribution ranging from 3000 to 16000. It is seen by these histograms that both images extract a very similar intensity distribution.

Finally, after the thresholding method, I achieved the image in Fig.4.4d with improved localization of the morphological pattern. For the CCD images seen in Fig. 4.6, I again applied the outlier removal algorithm as well as the auto-thresholding method. Resulting image after auto-thresholding is seen in Fig.4.6b.



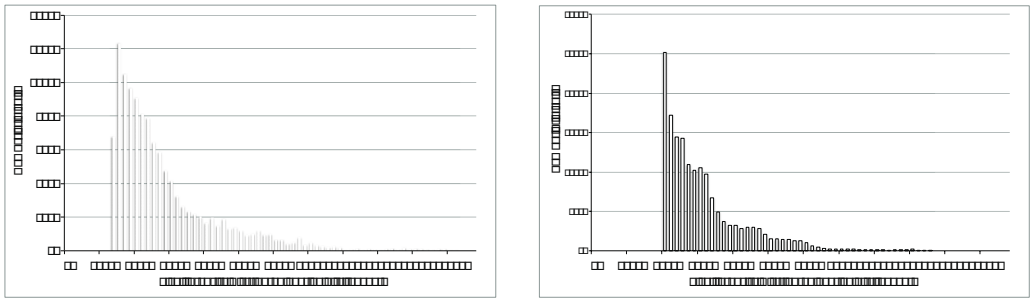
(a) Before Noise Removal (with DSNU)

(b) Master Dark Frame (MDF)

(c) After FPN Removal (without DSNU) (Contrast Enhancement for Better Display of Salt and Pepper Noise Caused by Hot Pixels

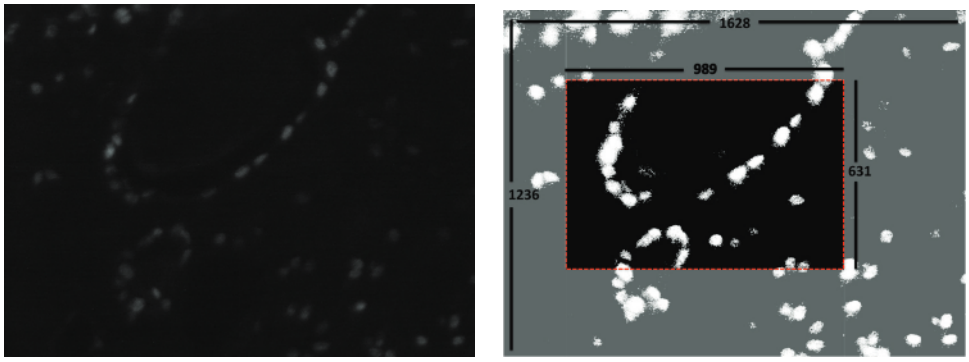
(d) After Otsu Auto - Thresholding Method

Figure 4.4: Tissue Sample Imaged by CMOS Camera (Exposure=1s, Gain=8x) [Köklü et al., 2012].



(a) CMOS Camera (b) CCD Camera

Figure 4.5: Histograms on Tissue Images Collected by the CMOS and CCD Cameras (Exposure=1s Analog Gain=8x)



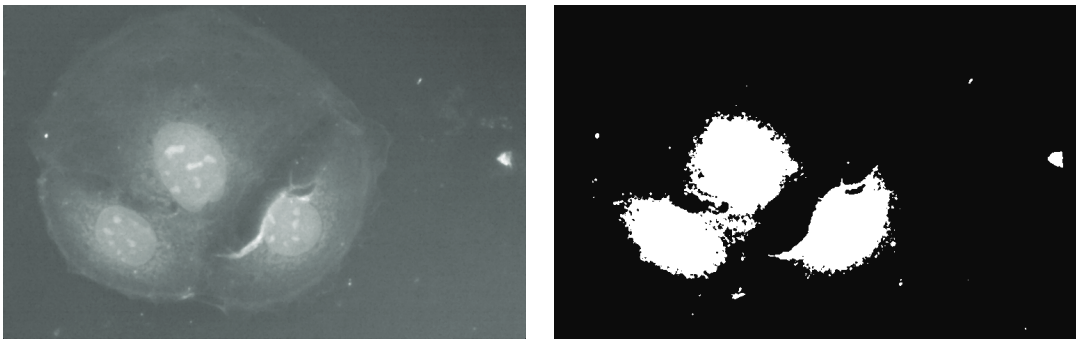
(a) Gray-Scale Image (Enhanced Contrast) (b) Black and White Image after Otsu's Auto-Thresholding Method

Figure 4.6: ER detection from Tissue Samples: Imaged by CCD Camera (Exposure=1s, Gain=8x) [Köklü et al., 2012].

4.5.0.2 Gabdh Gene Expression on Caco-2 Cells

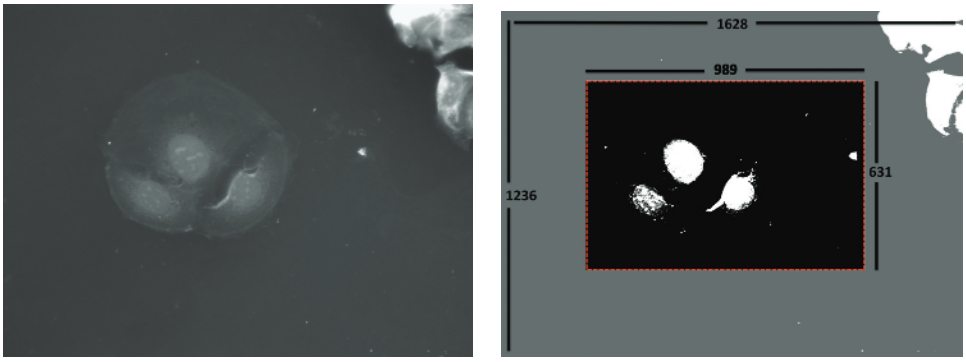
Human colon adenocarcinoma (Caco-2) cells are very important for new human health systems as well as for examinations for uptake and transport of the drug, Ferrum (iron), and other nutrients through the gut barrier. Since the culturing of mature intestinal epithelial cells are very difficult, recently Caco-2 cell lines have taken a lot of attention. In the literature, there are many examples of Caco-2 cell monolayers being proposed as a model for drug transport across the intestinal mucosa [Hilgers et al., 1990] and being used in investigations for the postpandrial i.e., after meal, inflammation in Gastro-Intestinal Tract (GIT) epithelial cells [Vergeres et al., 2012]. Thus, successful imaging of these cells with CMOS camera system has high importance for applications related to human uptake and transport phenomena through the gut walls.

Similar to the tissue sample images, again I corrected the CMOS camera images with the FPN removal algorithm and converted them to black and white with the auto-thresholding



(a) After FPN Removal (without DSNU) (b) After Otsu's Auto-Thresholding Method

Figure 4.7: Detection of Gabdh protein expression on Caco-2 cells. Imaged by CMOS Camera (Exposure=1s, Gain=16x) [Köklü et al., 2012].



(a) Gray-Scale Image (b) Black and White Image after Applying Otsu's Thresholding Method

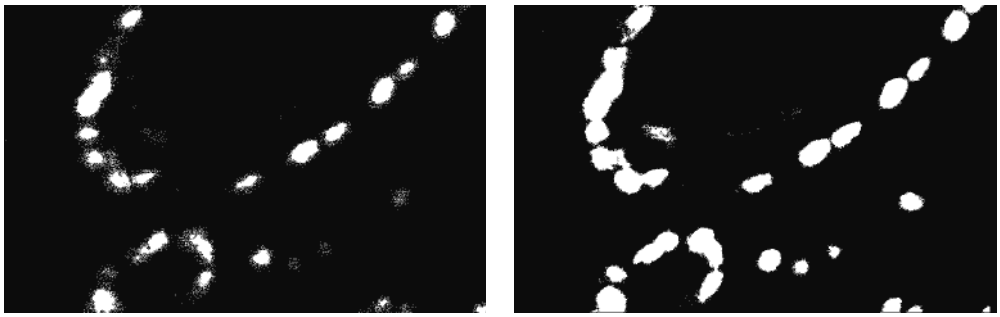
Figure 4.8: Image of Gabdh expression on Caco-2 cells: Imaged by CCD Camera (Exposure=1s, Gain=16x) [Köklü et al., 2012]

algorithm as seen in Figure 4.7. For the CCD camera Caco-2 cell images, I applied the same procedure as in the tissue sample imaging and results are shown in Figure 4.8. Three Caco-2 Cells are visible in these images and the Gabdh protein is expressed in the nucleus of the cells.

4.5.0.3 Comparison of CCD and CMOS camera images

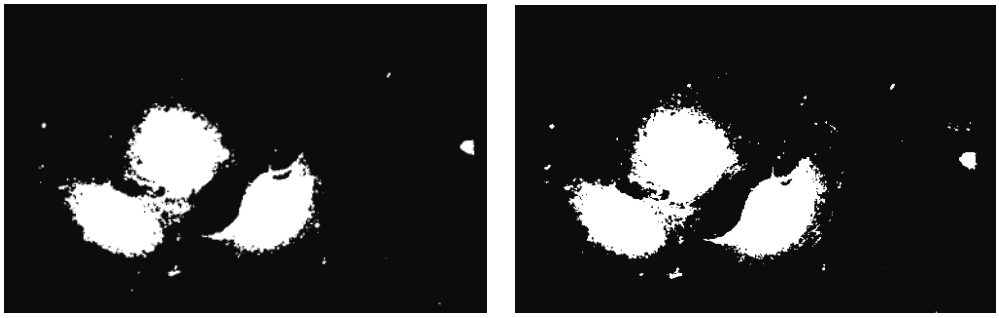
Fig. 4.9 helps to make a direct comparison on the CMOS and registered and resized CCD camera tissue and Caco-2 cell images.

In Figures, 4.9a and 4.9b, it is seen that both cameras are capable of detecting the morphological pattern of the ER receptor expression at the nucleus level that can be found in the breast tissue. I calcualted the correlation among the images by using the 2 dimensional cross-correlation function corr2 of MATLAB. This function calculates the correlation among matrices or vectors of the same size and the result returns a scalar value. The calculated coefficient



(a) Tissue Sample Image with CMOS camera

(b) Registered and Resized CCD Camera Tissue Sample Image (752 × 480)



(c) Caco-2 Cell Line CMOS Camera Image

(d) Registered and Resized CCD Camera Caco-2 Cell Line Image (752 × 480)

Figure 4.9: CMOS and CCD Camera Image Comparison [Köklü et al., 2012]

among these two images is 0.65.

In Figures, 4.9c and 4.9d, it is again visibly possible to conclude that both cameras are capable of detecting the morphological pattern of the Gabdh protein expression at the Caco-2 cell nucleus level. A correlation value among these two black and white images is 0.84.

These high correlation values confirm the conclusion that was drawn earlier that the CMOS cameras when empowered with image processing algorithms should be considered for cellular level optical studies on localization.

4.6 Conclusion and Novelty

All fluorescence imaging systems are believed to require high-quality cameras like CCDs, which are one of the most costly of all the other instruments of these systems. That is why I introduce a self-assembled CMOS camera as a replacement of the default CCD camera of our optical microscope and discuss the performance of it while decreasing the cost by approximately one order of magnitude. Since most of the biological applications focuses on the localization of the internal features of the cells, I have mentioned that the performance of the image sensors are mostly the key parameter in the success of these investigations. Even though the CMOS image

sensor used in this experiment is not the best of the market or the literature, it was capable of extracting information from the tissue and Caco-2 cell samples. I made a comparative study between these CCD and CMOS cameras with respect to their performances for imaging of these tissue and Caco-2 cell samples by using the optical microscope. For the cell samples, since ER expression for the tissue cell and Gabdh expression for the Caco-2 cell emit very low fluorescence light, the effect of the noise reduction algorithms have become very crucial and visible. At this high exposure rates, although the initial CMOS image has been very noisy, after applying proper image-processing algorithms, the CMOS camera was capable of generating the same morphological pattern as the CCD camera image.

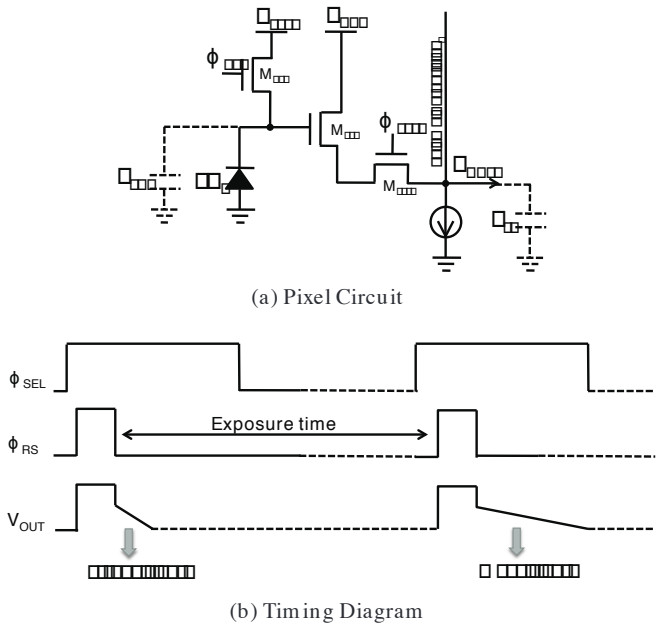
Despite what is said in the literature about the CCDs being the recommended technology for low-light biomedical applications, the results obtained in this chapter proves us that the standard CMOS cameras are also good candidates in high quality imaging applications for investigations on cells and tissues when empowered with efficient noise reduction algorithms [Köklü et al., 2012], [Köklü et al., 2013b]. Thus, within the frame of these obtained results, I recommend to the scientists a better analysis of their camera options before making a default decision. Undoubtedly, the trend towards using low-cost CMOS cameras is even more important when standard microscopy is replaced by (possibly disposable) LoCs since CMOS cameras make a good compromise between the cost and the performance. As expected, an application specific CMOS sensor would always perform better than a standard sensor from the market. Due to this reason, in the following chapters, I will introduce details of different pixel architectures for CMOS image sensors together with our proposed design solutions and designed and tested camera chips.

5 CMOS Active and Digital Pixel Sensor Designs

CMOS image sensors can be grouped as Active Pixel Sensor (APS) and Digital Pixel Sensor - (DPS). Both of these pixel architectures have advantages and disadvantages with respect to each other which requires a good analysis to be made for the concerned application. This challenge has led to many different APS and DPS designs to emerge. Below is a summary of well-known APS and DPS pixel and read-out architectures together with a summary at the end of this chapter explaining the ones that are designed and tested during this thesis.

5.1 Introduction

After the first introduction of electronic camera-on-a-chip concept, many techniques and designs have been proposed by scientists to overcome the disadvantages of the state of the art CMOS image sensor designs in order to reach compatible results with CCDs. Adding chip or pixel level new features, designing for more application specific constraints, reducing the noise and increasing the sensitivity are some of the achievements of these proposed designs. Among these proposed designs, APS designs with few number (3-4) of transistors have been the ones that are used most due to their simplicity and low area overhead. However, the APS designs suffer from the analog design limitations since the output of each pixel value is represented by an analog voltage signal and require a column or chip level ADC. To overcome the limitations of APS designs, different types of DPS designs are proposed. The DPS designs suffers less from analog design limitations since the pixel output is carried out as a digital signal and these designs do not require extra ADC units per column or per chip. DPS designs are known to achieve high speeds, over 10K [Kleinfelder et al., 2001], [Posch et al., 2010] and wide dynamic range over 100 dB [Bidermann et al., 2003], [Posch et al., 2010] and propose additional features such as adaptive dynamic range [Kitchen et al., 2005] and change detection [Posch et al., 2010]. Pulse Width Modulation (PWM) and Pulse Frequency Modulation (PFM) image sensors can also considered within DPS architectures. These sensors produce an output signal when the input signal reaches a certain value, as opposed to the APS designs where the output signal value is read after a certain time has passed. Also these sensor's result in superior SNR performance since the SNR is fairly constant at different light levels since the



(a) Pixel Circuit

(b) Timing Diagram

Figure 5.1: 3T APS Design

amount of charge to generate an event is always fixed [Posch et al., 2010].

Similarly, these type of architectures no longer represent the pixel value in voltage domain but in time or frequency domain [Nagata et al., 1999], [Shouho et al., 2005], [Yang, 1994], [Culurciello et al., 2003].

In this chapter, I will explore state of the art APS and DPS architectures with the advantages and disadvantages of each design.

5.2 CMOS APS Designs

5.2.1 APS Pixel Circuits

5.2.1.1 3T APS Pixel Circuit

3 Transistor (3T) APS has three transistors for each pixel as the name recalls. The first transistor is the reset transistor (M_{RS}) that resets the junction capacitance of the photo-device. The second transistor is the source follower transistor (M_{SF}) that converts the accumulated charges at the photo-device to voltage at its gate. It also makes the output voltage to follow the photo device voltage and works as a buffer to drive the high load capacitance of the column output line without having the load capacitance interfering in the voltage gain of the pixel as in Transversal Signal Line (TSL) type PPS designs [Noda et al., 1986]. Finally, the third transistor is the row select transistor (M_{SEL}). Fig. 5.1 illustrates the pixel circuit and the timing of the 3T APS design.

Thus, this pixel architecture introduces pixel level amplification and a conversion gain that is independent of the load capacitance. The output voltage of the 3T APS is depicted with the following formula:

$$V_{out} = G_{SF} \frac{1}{C_{PD}} \int I_{PD} dt \tag{5.1}$$

where G_{SF} is the source follower gain, C_{PD} is the photodiode capacitance, which is in fact the junction capacitance, and I_{PD} is the photodiode current. The junction capacitance can be expressed as below and the required parameters can be found in the model parameters of each design and calculated accordingly:

$$C_{jdep} = \frac{C_{J0} A_D}{(1 - (\frac{V_d}{v_j}))^m} + \frac{C_{J0sw} P_D}{(1 - (\frac{V_d}{v_{jsw}}))^{m_{jsw}}} \tag{5.2}$$

where C_{J0} and C_{J0sw} represent zero-bias capacitance at the bottom and sidewall components, V_d is the voltage applied to the photo-diode, v_j and v_{jsw} stand for the built-in potential of the bottom and the sidewall respectively, m and m_{jsw} are the grading coefficients of the bottom and the sidewalls, A_D is the photodiode area in m^2 and P_D represents the photodiode perimeter in m.

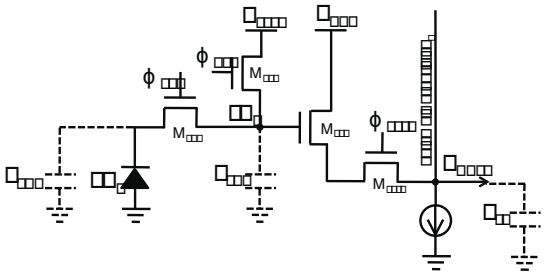
However, 3T APS pixels have many issues that should be addressed. The first of these problems is the difficulty in suppressing the kTC noise caused by the reset transistor. With 3T APS pixel circuit, it is possible to reduce offset that causes FPN in the image by using the noise reduction method of Delta Double Sampling (DDS), however, this technique does not totally eliminate the kTC or the reset noise. Second problem of 3T APS pixels is having the photon collection and conversion regions at the same node, which causes the photodiode junction capacitance in relation with the output voltage as seen in Eq. 5.1. This creates a trade-off in between the responsivity, N_{sat}, DR and the conversion gain, which are the most important performance parameters in image sensors. N_{sat} of a 3T APS design as in Fig. 2.5 can be calculated by the following formula [Nakamura, 2005]:

$$N_{sat} = \frac{1}{q} \int_{V_{PD}(min)}^{V_{reset}} C_{PD}(V) dV \tag{5.3}$$

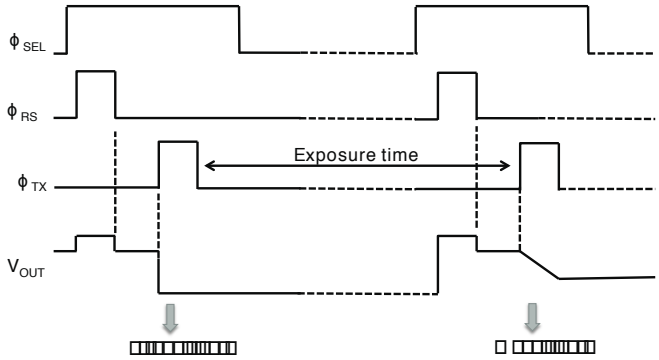
where q is electron charge, V_{reset} is the reset voltage of PD, $V_{PD}(min)$ is the minimum detectable voltage, defined by noise floor, I_{PD} is the photo current and C_{PD} is the capacitance of the photo-device.

In 3T APS circuits, there is also a direct relation between the N_{sat} and the noise in the pixel, since the kTC noise is inversely proportional with the value of the capacitance. Thus, having a larger photodiode will result not only in increased responsivity, FWC and DR but also will reduce the kTC noise but as mentioned earlier, it will decrease the conversion gain.

Thus, to overcome the intrinsic limitations of 3T APS pixel circuit, later 3T APS transistors are



(a) Pixel Circuit



(b) Timing Diagram

Figure 5.2: 4T APS Design

evolved to 4 Transistor (4T) APS pixels, which will be explained in the next section.

5.2.1.2 4T APS Pixel Circuit

4T APS pixels alleviate the issues of 3T APS with only one additional transistor. Although this additional transistor, M_{TX}, has caused the fill-factor to decrease compared to the 3T APS pixel, it has many advantages. First, it separates the photo collection region, i.e., photon-to-charge conversion region, and the charge to voltage conversion region. The separation of these two regions allow a more efficient method for noise reduction. This technique is called Correlated Double Sampling (CDS) method, which allows the reduction of not only the FPN noise but also the kTC noise by making two sampling correlated in terms of time or frame as opposed to the Delta Double Sampling (DDS) method. I will provide more details on the differences of these two noise reduction circuits in Section 5.2.2. Moreover, the N_{sat} of this design no longer depends on the junction capacitance of the photo-device, but it is dependent on the floating diffusion capacitance, which is the total capacitance at the FD node as shown in Fig. 5.2a and formulized in Eq. 5.4 [Nakamura, 2005]. This makes the N_{sat} usually smaller than the 3T APS pixels since the FD capacitance is a parasitic capacitance and expected to be lower than the PD capacitance unless an external capacitance is added to the FD node. That is why, other design techniques are usually applied to improve the DR in 4T APS designs [Yadid-Pecht and

Fossum, 1997], [Mase et al., 2005].

$$N_{sat} = \frac{1}{q} \int_{V_{FD(min)}}^{V_{reset}} C_{FD}(V) dV \tag{5.4}$$

The output voltage of the 4T APS pixel is depicted by the following formula:

$$V_{out} = G_{SF} \frac{1}{C_{FD}} \int I_{PD} dt \tag{5.5}$$

The equation 5.5 shows that there is no longer a trade-off between the photo-device capacitance and the conversion gain in 4T APS pixels since the conversion gain depends on the C_{FD} but not on the C_{PD}. This allows us to design larger photo-devices to improve collection efficiency without reducing the conversion gain. However, increasing the C_{PD} will no longer decrease the kTC noise, on the contrary, the kTC noise gets worse in the 4T APS pixels since the C_{FD} is a parasitic capacitance on the order of 5fF, which is usually lower than the photo-device capacitance and is on the order of 20fF. However, as mentioned earlier, 4T APS pixels allow a more effective noise reduction technique (CDS), which totally eliminates the kTC noise. So, the low capacitance at the FD node does not cause a problem in terms of noise. The main disadvantage of this implementation is the risk of incomplete transfer of the accumulated signal charge from the PD node to the FD node. This incomplete charge transfer may cause image lag and noise and worsens the performance of the device. The photodiodes implemented by the CMOS Image Sensor (CIS) dedicated technologies (Pinned PhotoDiodes (PPD) guarantee the complete transfer of the charge but with standard CMOS implementations, this is not certain. We will provide more details about the PPDs in Chapter 7, where I explain the working principle of 4T APS pixels with p^+/n-well/p-sub type photodiodes in standard CMOS technology.

In the literature, the 4T APS pixels are always implemented with buried or Pinned Photodiodes (PPD), which solves the incomplete charge transfer issue. The PPDs require a special image sensor dedicated technology called as CIS dedicated technologies. Almost all the foundries provide CIS dedicated technologies. However, these technologies cost much more than standard CMOS technologies. More specifically, according to the 2014 general run prices of Europractice-IC, the price for a 5mmx5mm block with UMC 0.18µm standard CMOS technology for standard customers is 13300EUR while with UMC 0.18µm CIS dedicated technology with conventional and buried photodiode option is 21600EUR. Although, the integration of the pixel with a photo-device implemented with a standard CMOS process but not with a CIS dedicated process would worsen the incomplete charge transfer issue from the PD node to the FD node, this is a compromise to be made in order to reduce the cost while keeping the advantage of making a true CDS noise reduction.

The demands for high performance image sensors, such as low-power, low-noise, wide-dynamic-range have led to the exploration of different pixel architectures e.g. 5T and 6T APS

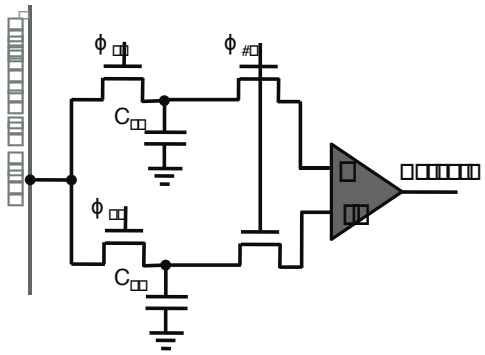


Figure 5.3: Traditional Noise Reduction with Two Sampling Capacitances

pixels [Tsai and Hornsey, 2011], [Pates et al., 2011]. Especially for the implementation of the global shutter technique in CMOS image sensors, additional transistors are required [Furuta et al., 2007].

In the next section (Section 5.2.2), we will introduce well-known DPS architectures that have been the inspiration of our novel DPS designs which will be covered in Chapter 9.

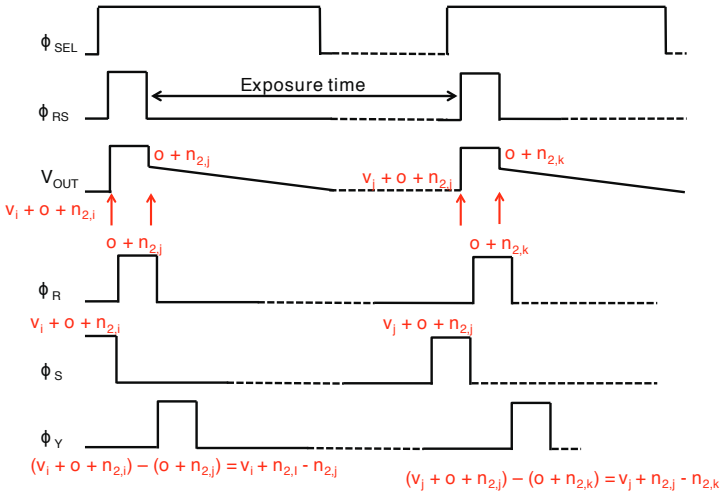
5.2.2 APS Noise Reduction Circuits

The APS noise reduction circuits implement either Differential Delta Sampling (DDS) also called Delta Double Sampling or Correlated Double Sampling (CDS) operations. However, these two terms may be used differently in the literature e.g. [Nakamura, 2005] vs [Ohta, 2010] and [Theuwissen, 2008].

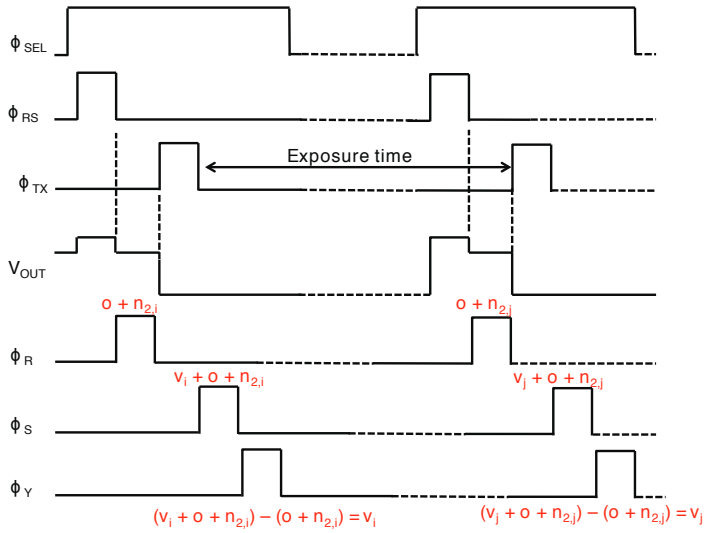
In this thesis, I call the DDS operation for noise reduction circuits integrated with 3T APS pixels which only omits the pixel offset but not the reset noise and the CDS (true CDS) operation for noise reduction circuits integrated with 4T APS pixels which omits both pixel offset and the reset noise by having correlated reset noise at two sampling phases.

Assuming that the same simple noise reduction circuit as shown in Fig. 5.3 is used for both 3T APS pixel and 4T APS pixel circuits, the timing diagrams in Fig. 5.4 show the result of the DDS and the true CDS operations. Thus, DDS technique results in $v_i + n_i - n_j$ during the ϕ_Y where n_i is the reset noise of the current frame and n_j is the reset noise of the next frame. As opposed, the true CDS results in only the required signal itself as v_i since it samples the reset noise of the same frame during both ϕ_R and ϕ_S phases.

Thus, the use of a transfer transistor and the addition of FD node in a 4T APS pixel has enabled true CDS operation and improved the noise performance of the sensor. The CDS operation is usually done per column in the literature in order to be able to have column-parallel noise reduction operations and speed up the process. However, due to the mismatch in the



(a) 3T APS with DDS



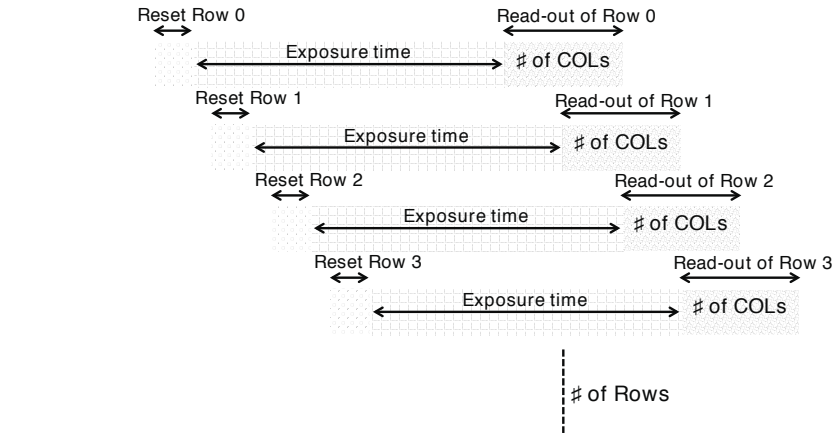
(b) 4T APS with CDS

Figure 5.4: Timing Diagram of DDS and CDS Noise Reduction Operations

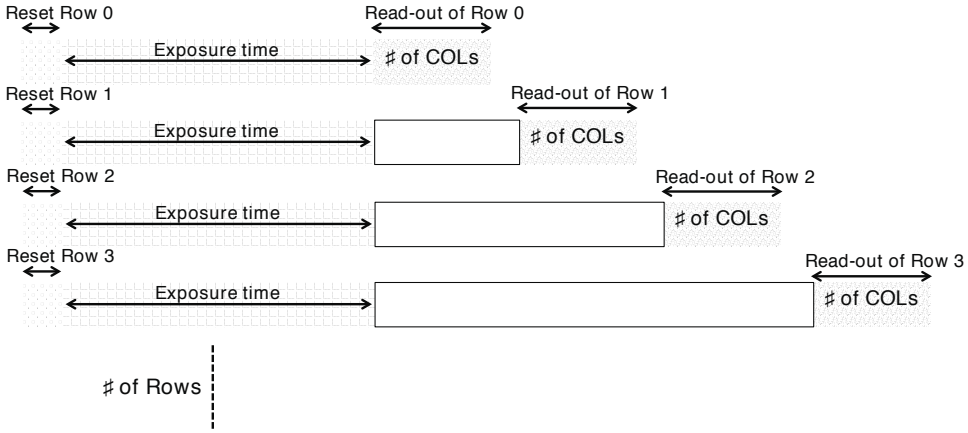
amplifiers of the CDS operation, this would cause additional column-parallel FPN to appear in the system.

5.2.3 APS Read-out Techniques

The read-out of the pixel outputs in CMOS image sensors can be done in column parallel or serial. Usually, the noise reduction circuits are implemented in column parallel. For the rest, serial or parallel readout approach can be applied. The serial approach requires the column parallel CDS outputs to be serialized, then connected to a chip level programmable gain stage and an ADC unit. This method is preferable for slow to high speed read-out imaging applications. It requires less area than column parallel processing and at the same time it



(a) Rolling Shutter



(b) Global Shutter

Figure 5.5: Shutter Techniques in CMOS Image Sensors

reduces the column level FPN by using a chip level amplifier. The alternative to the serial processing is the column parallel processing. This implementation uses column parallel programmable gain amplifiers and ADC units. This method achieves fully parallel read-out and is preferred for very high speed applications. Since it requires chip level memory to store the column level digital data, and column level amplifiers and ADCs, the area overhead with this approach is high compared to serial processing and it introduces extra column level FPN.

After introducing the two read-out techniques, now we mention the two shutter techniques in CMOS image sensors: rolling shutter and global shutter. In rolling shutter method, the rows and columns of the pixel array are scanned with horizontal and vertical scanning circuits. This technique can start and stop exposure of one row of a pixel array at a time. This technique is very efficient in slow scenes but creates problems in imaging of fast moving objects. With global shutter technique, the problem in rolling shutter technique with fast moving objects have been solved since the method allows all the pixels in the imaging array to start and stop the exposure at the same time. The timing diagram of these two shutter techniques is shown

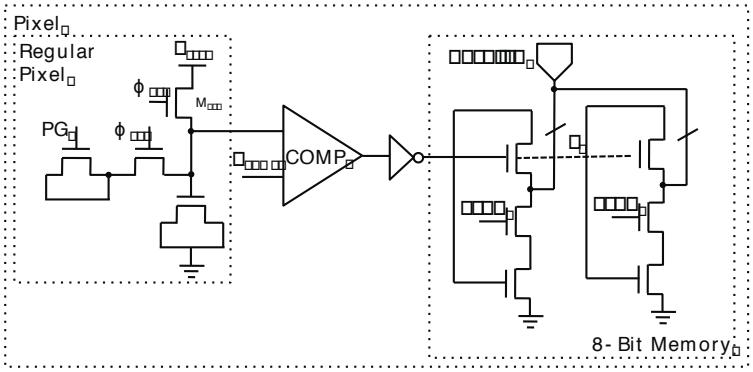


Figure 5.6: A 10 000 Frames/s CMOS Digital Pixel Sensor [Kleinfelder et al., 2001]

in Fig. 5.5.

5.3 CMOS DPS Designs

The CMOS DPS designs can be grouped as how their exposure time is defined. Regular DPS designs use fixed exposure time intervals for every pixel similar to the APS designs and outputs a result according to the pixel value at the end of that exposure time. As opposed, Pulse Width Modulation (PWM) and Pulse Frequency Modulation (PFM) type image sensors generate outputs when the signal value reaches a certain value. The simple principle of DPS designs have been presented in Fig. 2.6 in Section 2.2.2.3. In the following sections, first, we will give an example to a regular DPS design, then introduce PFM and PWM type image sensors and show examples of these type of sensors from the literature.

5.3.1 A High Speed DPS Design with Pixel Level Memory

Despite the high number of transistors and lower fill factor, DPS pixels can still be very useful for many applications. By employing an ADC and memory at each pixel, massively parallel A/D conversion and high-speed digital readout, DPS designs provide potential for high-speed imaging applications [Kleinfelder et al., 2001]. This type of sensors offer very high speed imaging over 10000 frames/sec [Kleinfelder et al., 2001] and most frequently find use in the high-speed video cameras, while sacrificing from the resolution and spectral sensitivity due to the increased pixel size. In Fig. 5.6, the DPS pixel presented in [Kleinfelder et al., 2001] that offers parallel 8-bit A/D conversion, and digital readout at continuous rate of 10 000 frames/s is shown.

As shown in Fig. 5.6, the pixel circuit consists of a photo-gate device, a comparator, and an 8-bit memory. The 8 bit memory is controlled by the output of the comparator and the exposure time interval of the pixel is fixed, which is controlled by the TX transistor. The pixel has a data I/O node, that is connected to the gray-scale counter that registers the value in the counter when the comparator output is high. The pixel-level memory was implemented using

three transistor dynamic memory cells [Kang and Leblebici, 2003], with a single read/write port which achieves small area and high-speed readout. The fill factor of this pixel is 15% and the memory was designed for a maximum data hold time of 10ms, which was enough for high speed applications. The top level design includes a memory row read pointer in order to choose one single row memory to be read at a time. Finally, for the serialization of the outputs, shift registers have been used.

Obviously, this design suffers from large metallic area in the pixel due to the high number of transistors at each pixel mainly because of the 8-bit pixel level memory. The storage of the digital value of each pixel inside the pixel also limits the digital resolution since a 12-bit design would require 36 transistors instead of 24.

5.3.2 PWM and PFM Image Sensors

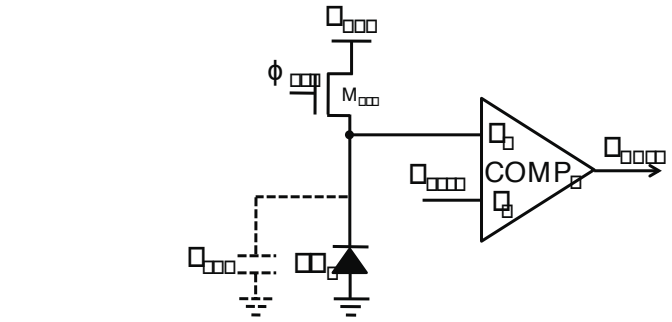
PWM and PFM sensors operate asynchronously since each pixel can make its own decision without depending on a clock. These sensors reach very high speed operations but are limited in terms of area and may result in time collisions when multiple events happen at the same time. These sensors are named as Time to First Spike Sensors, Time to Saturation Sensors or Address Event Representation Sensors. In figures 5.7 and 5.8, the pixel circuits of PWM and PFM type image sensors are presented together with their timing diagrams.

In the PWM pixel, one of the inputs of the comparator is connected to a fix reference voltage or a ramp voltage. In the PFM pixel, the comparators are used as modulators. These pixels can also be implemented by replacing the comparator with inverter chains, where the threshold voltage of the inverter can be considered as the reference voltage of the comparator.

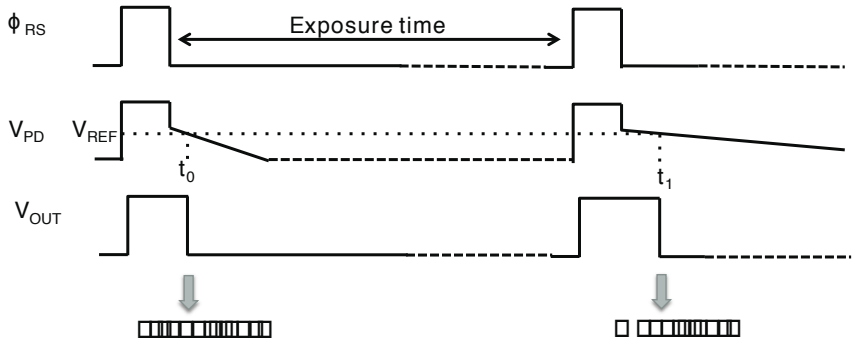
In the literature, many examples of PFM based sensors for bio-medical applications, more specifically for ultra low light detection of bioluminescence samples [Nivens et al., 2004], [Islam et al., 2007] and retinal prosthesis [Ohta et al., 2002] can be found. In addition to those, extra features have been added to the PFM pixels such as change detection [Culurciello et al., 2003], [Mallik et al., 2005], [Chi et al., 2006], [Posch et al., 2010], [Delbruck et al., 2010], [Posch et al., 2011]. In the following section, I will explain one of the examples of a change detection PFM sensor in more detail [Posch et al., 2011].

5.3.2.1 A QVGA PWM Sensor with Change Detection

This design has been proposed by C. Posch et al., which has two pixel parts one for exposure measurements and one for change detection [Posch et al., 2011]. A representation of the exposure measurement pixel circuit of this design is shown in Fig. 5.9a and the change detection pixel circuit is shown in Fig. 5.9b. The exposure-measurement device is realized as a time-based PWM circuit with an additional logic block that is used to allow true correlated double sampling based on two global integration thresholds. The differential operation with two different reference voltages within one integration cycle eliminates both comparator

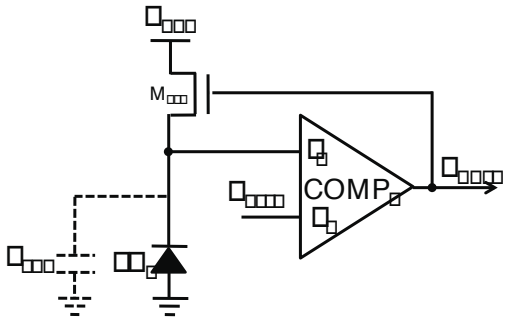


(a) Pixel Circuit

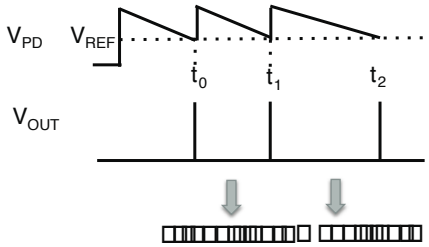


(b) Timing Diagram

Figure 5.7: PWM Image Sensors



(a) Pixel Circuit

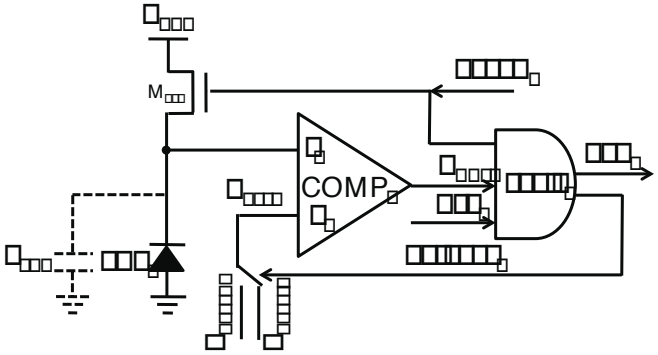


(b) Timing Diagram

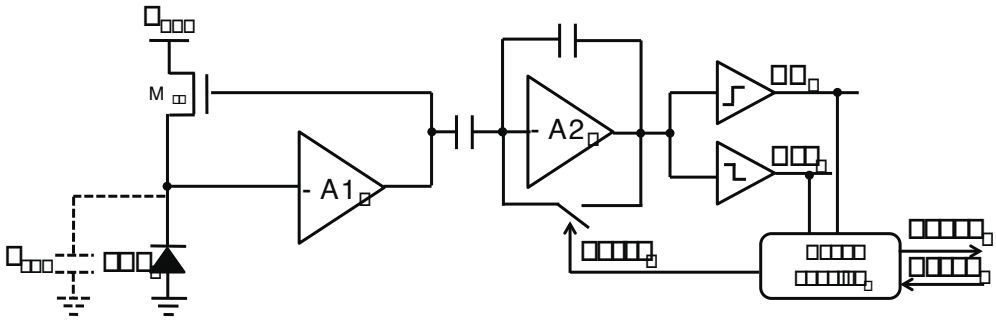
Figure 5.8: PFM Image Sensors

offset FPN and reset kTC noise. The change detector pixel in Fig. 5.9b responds to a relative change in illumination by triggering the Address Event Represent (AER) protocol and the reset switch. With this trigger, the exposure measurements are re-initiated. AER is used in order to provide efficient allocation of the output transmit of the active pixels by using Request and Acknowledge signals.

The change detector pixel circuit consists of a photodiode, a differencing switched-capacitor amplifier and a comparator-based event generator. With this method, the change detector



(a) Exposure Measurement Pixel



(b) Change Detector Pixel

Figure 5.9: A QVGA PWM Sensor Pixel Design with Change Detection

generates output only when there is a relative change compared to the previous voltage output of the pixel. This design reaches a fill-factor of %30, where %20 belongs to the exposure measurement pixel and %10 to the change detector pixel. Obviously, the change detector pixel has immensely increased the area and reduced the fill-factor.

5.4 Summary and Discussion

In this chapter, I introduced different APS and DPS designs and explained their advantages and disadvantages with respect to each other.

Within the frame of this research, I designed, implemented and tested three APS chips, i.e., a characterization chip, a small array camera chip, and a VGA camera chip by using a standard CMOS technology. For the characterization chip, I used 3T APS pixel circuit (see Fig. 5.1) in order to characterize different photodiodes with different types, sizes and shapes. I will provide more details of this chip design and its silicon results in Chapter 6. For the small array and VGA camera chips, I used 4T APS pixel circuit since this design solves the trade-off issues of 3T APS and allows the implementation of true CDS noise reduction. As mentioned earlier, APS pixels with higher number of transistors can also be found in the literature, e.g., high gain APS pixels and global shutter pixels. However, these designs have not been considered

for the fabricated chips in order to keep the number of transistors as low as possible and reach a high fill factor and photon collection efficiency. Moreover, I implemented all camera chips with a novel column parallel CDS noise reduction circuits. I will give the details of this design in Chapter 7. With this implementation, I succeed in reducing both pixel level FPN and reset noise. However, the column parallel amplifiers have resulted in column level FPN, which can be deducted by post-processing. For the read-out of these camera chips, I used the serialized read-out approach with rolling shutter since biomedical applications do not require very high speed imaging, and I aim to spend as small as possible silicon area to increase the fill-factor and the photon collection efficiency. Finally, all these camera chips are fabricated with a low-cost standard CMOS technology instead of a high cost CIS dedicated technology. This approach has dramatically reduced the fabrication cost of the chips and made them applicable to for low-cost biomedical devices.

Within this chapter, I also investigated different DPS designs from the literature, which provide additional features with higher number of transistors in the pixel. Thus, within this research, the designs with higher number of transistors have only been considered for digital pixel implementations, where the target is to reduce the analog design limitations and bring additional pixel level functionality. By considering these additional features and their applicability to biomedical applications, in Chapter 9, I will propose novel DPS designs, which are inspired by the designs shown in Fig. 5.6 and Fig. 5.9 and optimized for biomedical applications.

6 Chip 1: Standard CMOS Compatible Photodiodes Characterization Chip

The performance parameters of CMOS compatible photodiodes depend on the size, type and the geometry of the photodiode layout and varies for each technology. In this part of the thesis, I present a comparative analysis of standard CMOS compatible photodiode types with different areas. I sent this characterization chip for fabrication as one mini-asic block with an area of 1525µm × 1525µm. The silicon results of this camera chip have shown that n-well/p-sub type photodiode with $5 \times 5\ \mu m^2$ diffusion area achieves the highest sensitivity ($69.81 \times 10^{12}\ V.s^{-1}.cm^{-2}/W.cm^{-2}$) and with $40 \times 40\ \mu m^2$ diffusion area, highest SNR (72.26dB) at 630 nm, while the p^+/n-well/p-sub type photodiode with $40 \times 40\ \mu m^2$ diffusion area results in highest responsivity ($0.466\ A.cm^{-2}/W.cm^{-2}$) and QE (%63) at the same wavelength [Köklü et al., 2013a].

6.1 Introduction

Each technology has different characteristics and different photon response. Moreover, none of the foundries provide photodiode characterization data for the designers. Therefore, the designers are left alone to characterize their own chip for the chosen technology. Thus, the need for characterization of photodiodes for each technology always remain. In this part of the thesis, with the measurement results obtained from our characterization chip, I provide a quantitative comparison for performance parameters of CMOS compatible photodiode structures with different areas for UMC 0.18µm standard CMOS process. With these results, I aim to fulfill the need for the characterization data of UMC 0.18µm 6-metal 1-poly standard CMOS process before going any further with the image sensor design. With this study, to the best of my knowledge, I provide for the first time in the literature characterization results for a 0.18µm standard CMOS process.

6.2 CMOS Compatible Pixel Design

Three main photodiode structures, i.e., n^+/p-sub, n-well/p-sub, and p^+/n-well/p-sub, are available to be used in standard n-well CMOS processes. In this chapter, I provide the test results of these photodiodes by using 3T APS pixel circuit, which is the simplest of all APS pixels and I show the Dark Signal, Sensitivity, Responsivity, Quantum Efficiency, and Signal to Noise Ratio results of each of these photodiodes.

The literature reports some examples of similar studies that quantitatively compare different photodiode structures e.g. dimensional effects in different photodiode types are explored for 2μm n-well analog low noise process [Brouk and Nemirovsky, 2002] and different photodiode structures were compared for a 0.5μm 3-metal, 2-poly, n-well process [Murari et al., 2009a]. However, as mentioned earlier, each of these studies are unique for the process that the sensor is designed with and in both of these processes Local Oxidation (LOCOS) isolation is used where as in sub-micron technologies, i.e., UMC 0.18μm , Shallow Trench Isolation (STI) is used, which immensely affects photodiode dark noise. Therefore, I provide the characterization data for available photodiodes for UMC 0.18μm technology with LOCOS, which may be consistent for other sub-micron technologies as well.

6.2.1 Performance Parameters of CMOS Photodiodes and Pixels

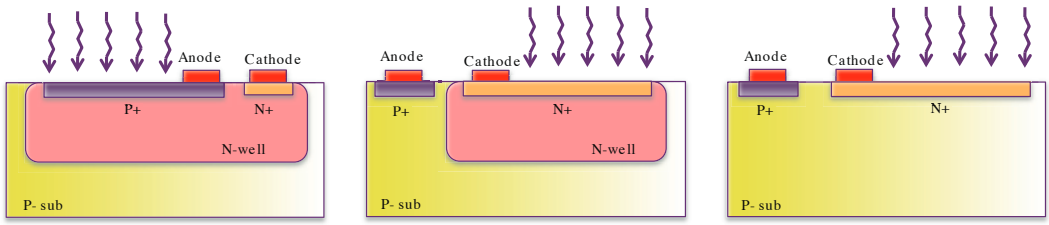
Sensitivity and dark current are the most important parameters in low-light imaging. In the literature, the sensitivity parameter of a sensor may be referred in different ways. In this research, I use sensitivity parameter for denoting pixel performance in Volts per unit area and time per incident optical input power per unit area in $V.cm^{-2}.sec^{-1}/W.cm^{-2}$ and responsivity parameter for expressing photodiode performance, which is defined as the ratio of the photocurrent to the optical input power, in $A.cm^{-2}/W.cm^{-2}$.

Dark current refers to photodiode or pixel leakage current when the sensor is under dark and ideally no photons are entering the device. In this study, I use dark signal notation to demonstrate the pixel level leakage signal under dark in mV/sec, which is pixel specific but can be used to estimate photodiode dark current density.

6.2.2 Design of CMOS Compatible Photodiodes

Fig. 6.1 presents the cross section of p^+/n-well/p-sub, n-well/p-sub, and n^+/p-sub photodiodes.

The n^+/p-sub type photodiode is the most straightforward photodiode type and achieves the smallest area. However, it suffers from low collection efficiency due to the highly doped n region and expected to result in low responsivity and sensitivity compared to the other two structures.



(a) p^+/n-well/p-sub (b) n-well/p-sub (c) n^+/p-sub

Figure 6.1: Cross Section of Three Different Photodiode Types Compatible with Standard CMOS

The n-well/p-sub type photodiode benefits from the lower doping concentration of n-well, so it achieves higher collection efficiency. However, for the same area of n^+ diffusion region, when designed according to the minimum spacing of n-well to n^+, this type of photodiode occupies larger area than n^+/p-sub type.

The required spacing of extra well and implant make the area even higher for p^+/n-well/p-sub type photodiode. This type of photodiode is called as Partially Pinned PhotoDiode (P-PPD) in the literature [Guidash et al., 1999]. It has a buried-diode structure with a p^+ cap layer and two junctions as p^+ to n-well and n-well to p-sub. These two junctions increase the total junction capacitance of this type of photodiode and makes it much higher than the other types. However, this makes the effective depletion region also much larger and enhances the collection efficiency. Thus, I expect the p^+/n-well/p-sub type photodiode to achieve higher responsivity than the other two, but due to the large junction capacitance, conversion gain will again be lower for 3T APS design.

Since the n-well diffusion is deeper than n^+ diffusion, the junction is also deeper. Thus, it is expected for both the p^+/n-well/p-sub and n-well/p-sub type photodiodes to be more efficient in capturing photons at longer wavelengths.

I drew the layouts of these photodiodes by using Cadence Virtuoso Analog Design Environment and used the schematics and models of the regular diodes from the UMC library named as DION_MM, DIOP_MM and DIONW_MM to match the layouts and the schematics. I placed metal contacts only on the side of the active areas in order to increase the fill factor. Also, I covered the diffusion areas of the photo-diodes with salicide block layer (SAB) with minimum required distance from the metal layer. Salicide layer is normally used when creating contacts with low-resistivity and it is an opaque layer. Thus, placing a SAB layer will block the salicide formation on the area it is placed. The SAB layer is generally used on the poly resistors to increase the sheet resistance of these resistors. When a SAB layer is put on the diffusion area, the resistivity of the diffusion area is increased and heavy contamination during salicide formation is avoided. Thus, the dark current caused by heavy metal defect is suppressed.

The read-out of the corresponding photodiodes as mentioned in the previous section are

Table 6.1: Junction Capacitance (fF) of p^+/n-well/p-sub, n-well/p-sub and n^+/p-sub Type Photodiodes with Different Diffusion Areas at Pixel Reset (VSET = 1.4V)

Type	5x5µm^2	10x10µm^2	20x20µm^2	40x40µm^2
p+/n-well/p-sub	21.29	80.33	311.7	1227
n-well/p-sub	2.28	7.84	28.85	110.5
n+/p-sub	19.71	74.6	209	1143

all realized by using traditional 3T APS pixel circuit with the same sizing. The formulas for calculating the output voltage of this circuit and the junction capacitance of the photodiode have already been provided in Chapter 5, Eq. 5.1 and Eq. 5.2 respectively. In the junction capacitance equation, I have used the same notations for the parameters given in Cadence Spectre Model Parameters. Thus, the depletion capacitance for each photodiode can be calculated by using the model parameters given in Cadence. The calculated junction capacitors of the three photodiode structures with different diffusion areas during the reset of the pixel are given in Table 6.1. In the next section, I will introduce the experimental setup that I have built and later used to test my characterization chip.

6.3 Experimental Setup

Depending on the required precision of an optical experimental setup, the instruments can become quite costly and bulky. Conversely, I built a very low-cost experimental setup and tried to achieve a good balance between the cost and the precision.

In this setup, incident light is controlled using an epoxy encased LED - Light Emitting Diode together with a Neutral Density (ND) filter wheel. Light intensity is measured using Thorlabs optical power meter (PM 120D). I used various LEDs at different wavelengths from 465 nm to 940 nm wavelengths to cover a wide spectrum. This implementation offered us a very cost-efficient solution compared to spectro-fluorometers and Xenon light sources with controlled spectrums. Moreover, I used a square pattern diffuser to increase the uniformity of the generated beam by the LEDs. I used two different cube mounted beam splitters for 400 nm - 700 nm and 700 nm - 1100 nm to split the beam equally (“ideally") into two channels, where one is connected to the silicon detector of the optical power meter and the other to the PCB - Printed Circuit Board of our test chip. The optical power meter is capable of measuring light sources from 50nW to 50mW at wavelengths between 400 nm to 1100 nm. Finally, I used an 8 bit Tektronix TDS 2004C oscilloscope to measure the pixel voltage outputs that are integrated with different photodiodes. Fig. 6.2 illustrates the experimental setup.

Fig. 6.3a, Fig. 6.3b, and Fig. 6.3c show the picture of the experimental setup, the layout of this chip, and the PCB that is used to test this characterization chip respectively.

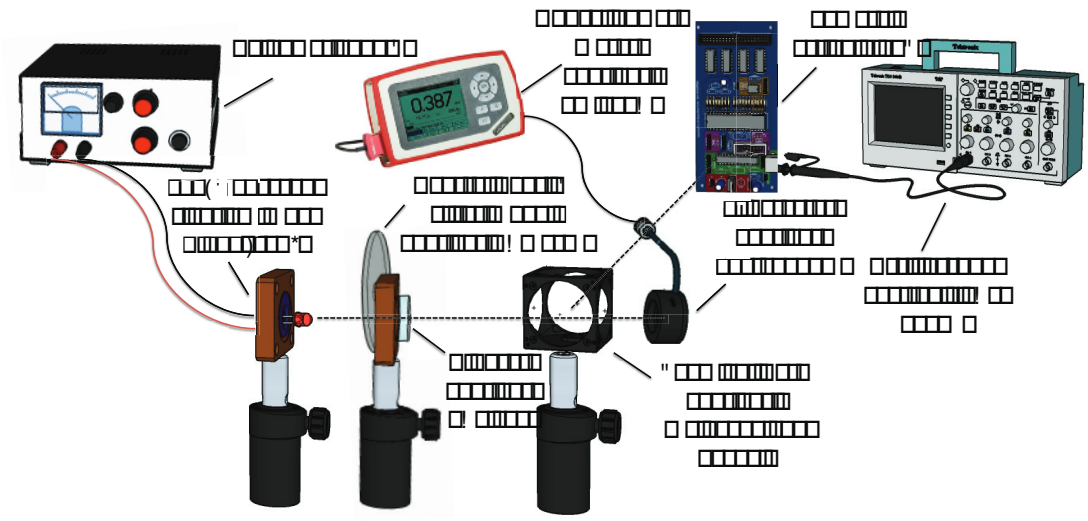


Figure 6.2: Optical Setup for the Characterization of the CMOS Compatible Photodiodes

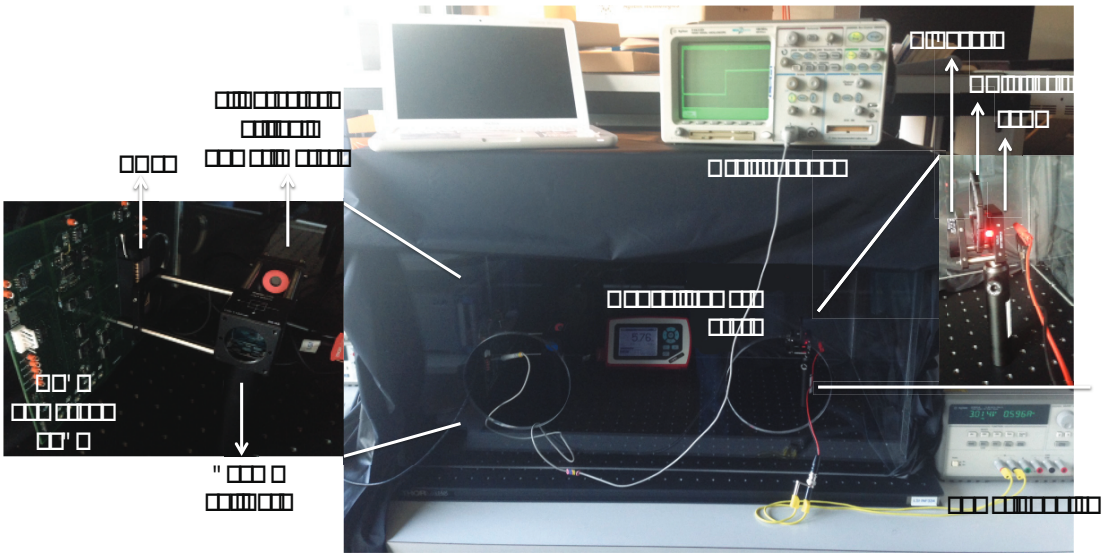
6.4 Results and Discussion

After introducing the experimental setup, I now present the measurement results of this characterization chip. I first provide the transient measurement result of the 3T APS pixel at different light intensities and then present the performance parameters, which are obtained by using this pixel.

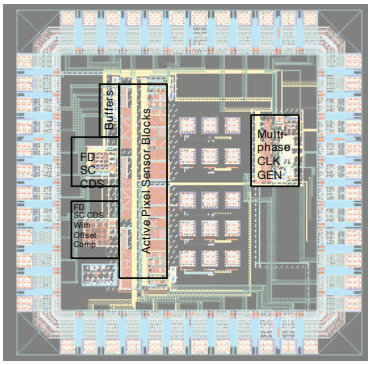
Fig. 6.4 presents the measured transient response of the 3T APS pixel with a $5 \times 5 \mu m^2$ p^+/n-well/p-sub type photodiode. In this measurement, the sampling rate is kept at 4.8ms and the intensity of the light is varied by changing the Neutral Density (ND) filter value. By increasing the ND filter value, the light present on the sensor is decreased. Thus, the photodiode capacitance discharges more slowly when there is less light present on the sensor. In Fig. 6.5, the same behavior is shown by the pictures collected from the oscilloscopes screen. With this figure, I present the measurement results of the pixel under dark and under two different light intensities.

The sensitivity parameter is calculated by normalizing the pixel voltage output discharging slope to the incidence irradiance present on the sensor and the photodiode area. I repeated this experiment for each type of photodiode with different diffusion areas, i.e, $5\mu m \times 5\mu m$, $10\mu m \times 10\mu m$, $20\mu m \times 20\mu m$ and $40\mu m \times 40\mu m$. Moreover, I calculated the data over a wide spectral range from 465nm to 940nm by varying the light source among LEDs with different centre wavelengths. Figures 6.6, 6.7, and 6.8 present the sensitivity results of each type of photodiodes separately. According to these results, the n-well/p-sub type photodiodes reach the highest sensitivity for each active area and the highest sensitivity is achieved with the smallest (5×5) photodiode which is (69.81×10^{12} $V.s^{-1}.cm^{-2}/W.cm^{-2}$).

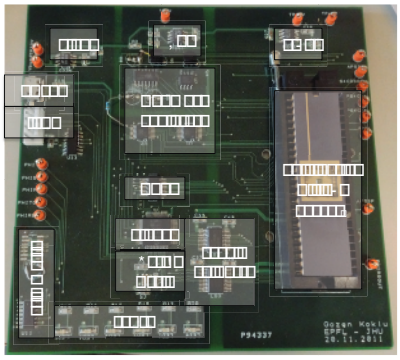
Responsivity is calculated by multiplying the sensitivity results with the junction capacitance



(a) Picture of the Optical Setup



(b) Top Level Layout



(c) Test Board

Figure 6.3: Pictures of the Experimental Setup, Layout and the Test Board of the Characterization Chip

of each photodiode according to Eq. 5.1 and Eq. 5.2. The results are shown for two different diffusion areas i.e. 5µm × 5µm and 40µm × 40µm and given in Fig. 6.9. According to these results, p^+/n-well/p-sub type photodiode achieves the highest responsivity as expected due to its increased collection efficiency with two pn junctions, p^+/n-well and n-well/p-sub. However, as I have explained earlier, due to the increased junction capacitance of p^+/n-well/p-sub type photodiodes, they result in lower conversion gain and reduced sensitivity than n-well/p-sub type photodiodes in 3T APS designs despite their higher responsivity. Moreover, as expected, as diffusion area is increased, responsivity also increases, which is due to the fact that the photo carriers generated in the neutral ("dead") regions are also collected by the diffusion [Brouk and Nemirovsky, 2002]. Fig. 6.9 shows that at higher wavelengths, both p^+/n-well/p-sub and n-well/p-sub type photodiodes result similarly. This is due to the deeper n-well junctions in both of these devices which result in better collection efficiency than n^+/p-sub type photodiodes at longer wavelengths and have caused the second bump at the 870nm

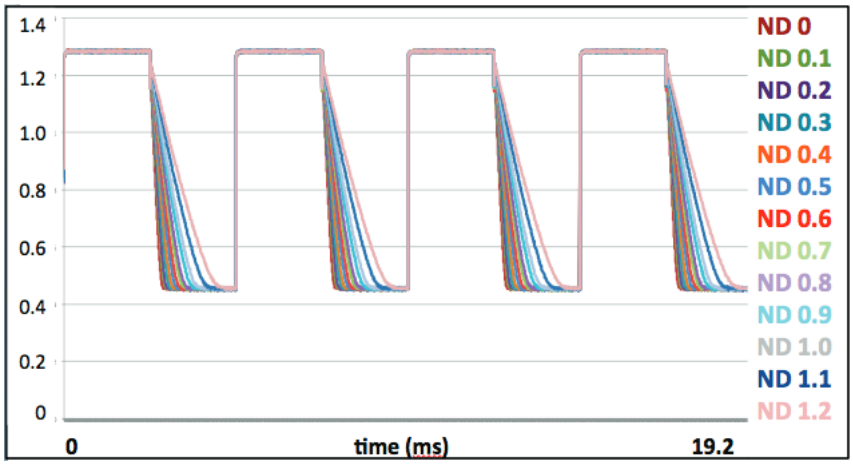
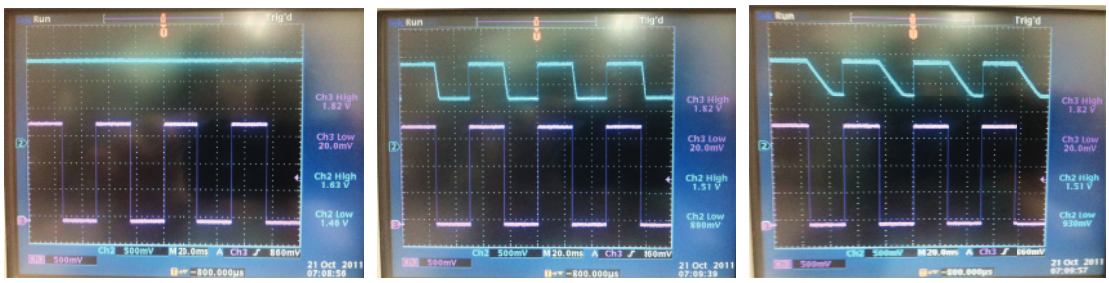


Figure 6.4: Measurement - Transient Response of 3T APS Pixel



(a) Sensor under dark

(b) Sensor is exposed to regular office light

(c) Sensor surface is covered to limit the light

Figure 6.5: Pictures of the Measurement Results Obtained from the Oscilloscope

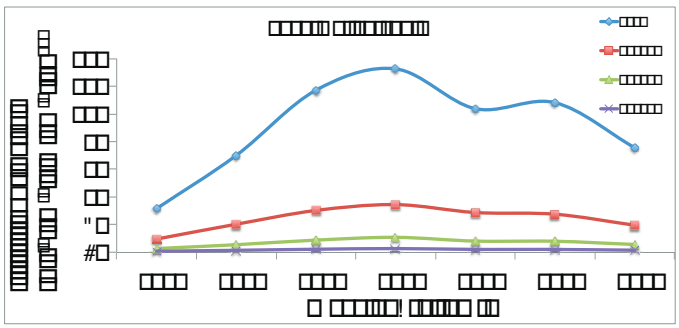


Figure 6.6: Measured Spectral Sensitivity of p^+/n-well/p-sub type photodiodes with different diffusion areas

wavelength. Quantum Efficiency (QE) is calculated by using the responsivity data according to Eq. 3.6. According to Fig. 6.10, the p^+/n-well/p-sub type photodiode with 40µm × 40µm diffusion area reaches the highest QE, which is %63.

Dark signal is measured by keeping the sensor under dark during a long integration period

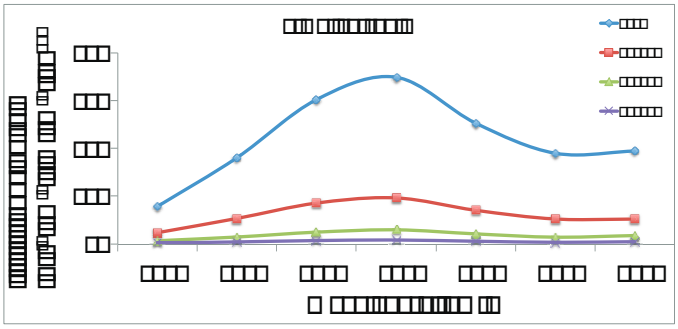


Figure 6.7: Measured Spectral Sensitivity of n-well/p-sub type photodiodes with different diffusion areas

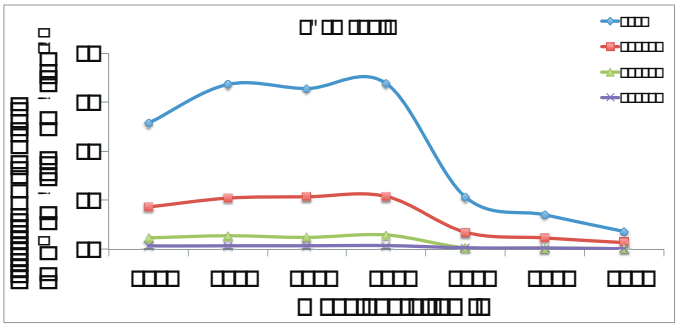


Figure 6.8: Measured Spectral Sensitivity of n^+/p-sub type photodiodes with different diffusion areas

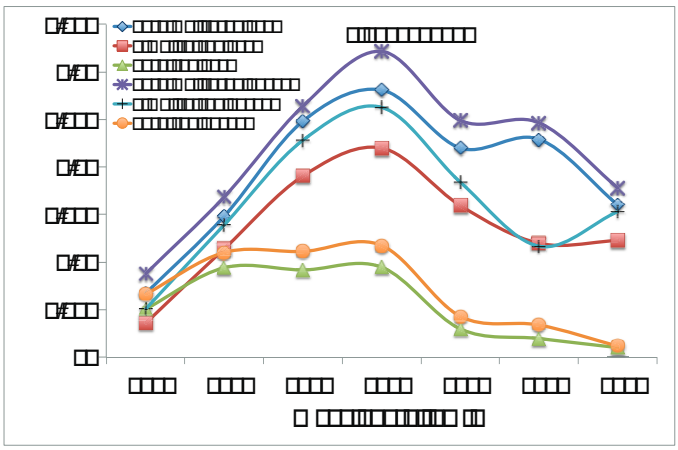


Figure 6.9: Calculated Responsivity comparison of different photodiode types with different diffusion areas

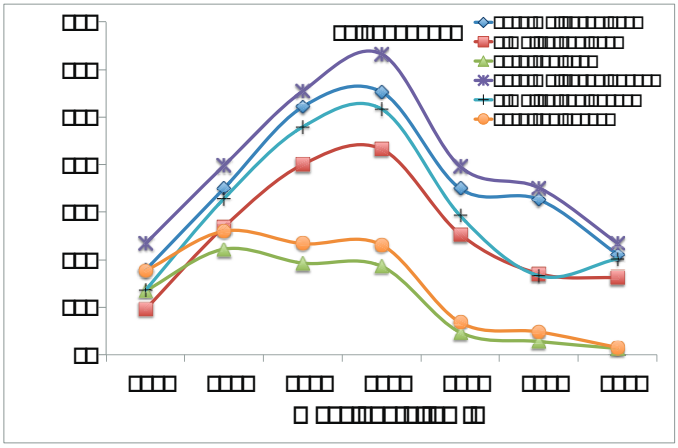
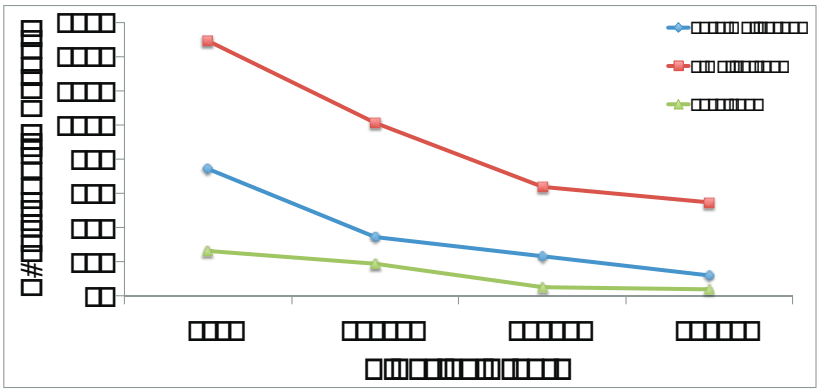
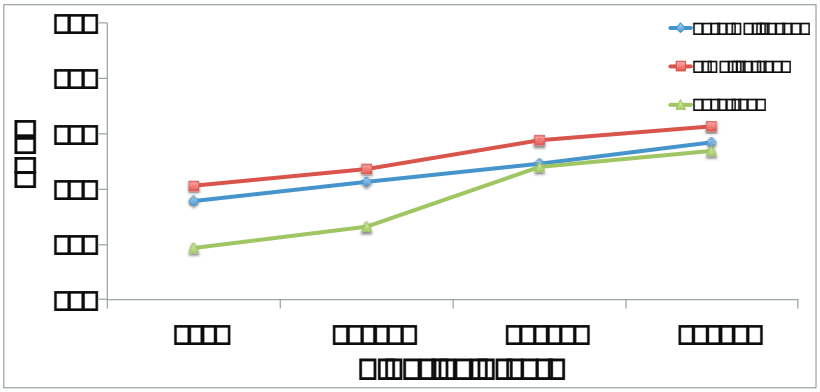


Figure 6.10: Calculated Quantum Efficiency of Different Photodiodes



(a) Dark Signal



(b) SNR

Figure 6.11: Comparison of Dark Signal and SNR of Photodiodes with Different Diffusion Areas

and the slope of the voltage output under dark is calculated. However, this noise signal is not only due to the photodiode dark current but also partially generated due to the photon shot noise, reset (kTC) noise, and the CMOS device noise. In this design, since there are no noise reduction circuits, all the noise sources are present at the output. However, in order to partially remove the shot noise, the collected data is averaged among 128 samples. Fig. 6.11a illustrates the dependency of dark signal over diffusion areas. The decrease of the dark signal by the increase of the photodiode area indicates that the main noise sources contributing to the dark signal is the photodiode dark current and the reset noise since they are both inversely proportional to the photodiode capacitance. In addition, dark current decreases by the decrease of the reverse bias voltage. However, there is a trade-off between the dynamic range of the sensor and the reverse bias voltage.

Finally, SNR parameter provides a relative comparison of the sensitivity and the dark signal. Fig. 6.11b presents that SNR increases with the increase of the photodiode area, which implies that the sensitivity decreases slower than the dark current with respect to the photodiode area.

6.5 Conclusion and Novelty

This comparative study provides preliminary data for the first time for CMOS image sensor designers working with UMC 0.18µm standard CMOS process. With this study, I not only decided which photodiode to use for our camera chips but also helped other designers to choose the right diffusion area for the required performance in terms of responsivity, sensitivity or SNR in order to achieve a good balance between resolution, cost and area [Köklü et al., 2013a].

This study stresses the dimensional effects on CMOS compatible photodiode structures and recommends the use of n-well/p-sub type photodiodes for higher sensitivity and SNR results while achieving lower area than p^+/n-well/p-sub type photodiodes for 3T APS pixels. By resulting with highest responsivity and QE, I recommend the use of p^+/n-well/p-sub type photodiodes when the photodiode junction capacitance is no longer a limiting factor for the conversion gain like in 4T APS pixels or similar designs. In addition, when used with 4T APS pixels, p^+/n-well/p-sub type photodiodes allow a more effective noise reduction circuit implementation (CDS). I will give more details on the p^+/n-well/p-sub type photodiodes when I provide the details of our first camera chip in Chapter 7. n^+/p-sub type photodiodes have the smallest area but due to their 20 times less sensitivity and 2 times less responsivity than n-well/p-sub type photodiodes and 4 times less sensitivity and responsivity than p^+/n-well/p-sub type photodiodes, n^+/p-sub type photodiode is out of discussion for low light imaging applications.

Finally, I have shows that this sensor performs best at wavelengths from 630nm to 780nm by reaching the highest responsivity and sensitivity among other wavelengths.

During this thesis, I designed and optimized the other camera chips, i.e., the small array cam-

era chip and the VGA camera chip, according to the results obtained from this characterization chip.

7 Chip 2: A 64x60 4T APS Camera Chip

This part of the thesis explains the design, implementation, and image acquisition process of the camera prototype that integrates a small active pixel array (64 × 60) with photodiodes and surrounding pixel electronics, noise reduction circuits, and vertical and horizontal access circuits. I have implemented this chip according to the data obtained from the characterization chip. This camera chip provides a fully functional prototype of a low-cost high quality CMOS camera fabricated with UMC 0.18µm standard n-well process, where the total area of the camera is 3240µm × 1525µm .

7.1 Top Level Design

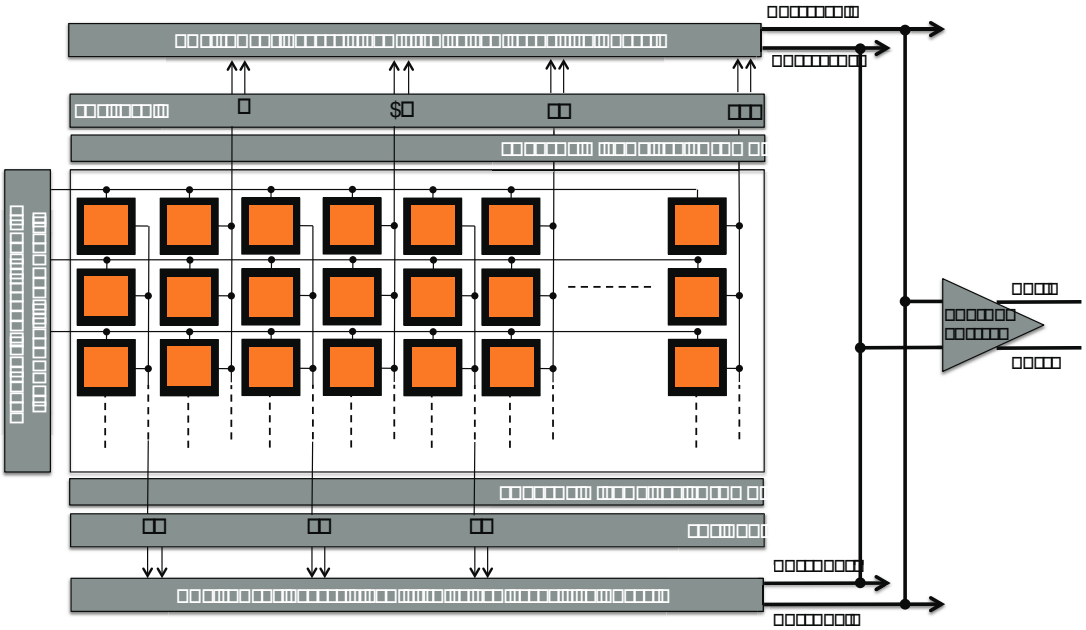


Figure 7.1: Top Level Schematic of the 64 x 60 Camera Chip

Fig. 7.1 shows the top level schematic of this camera chip.

The chip includes a 64×60 4T APS pixel array with a total pixel array area of $852 \times 616 \mu m^2$. There are column level current mirrors and switched capacitor CDS noise reduction circuits at the top and bottom of the pixel array. CDS circuits at the top are connected to the even numbered columns and the CDS circuits at the bottom are connected to the odd numbered columns. This implementation of splitting the CDS part into two block reduces the horizontal dimension of the column parallel CDS circuits and helps to reach a more compact layout while having equal sized wires for connecting the column outputs to the CDS circuits. The horizontal access circuit also exists both at the top and the bottom of the pixel array, which are used to serialize the column parallel output of the CDS circuits. They consist of shift register circuits and two transmission gates for each column output. The vertical access circuit consists of a 6 bit counter and a decoder, where the select lines of the decoder are determined by the value of the counter at the time being. The differential outputs of the top and bottom CDS are connected to the same bus, and this differential signal is amplified by the differential analog buffer at the right side of the pixel area.

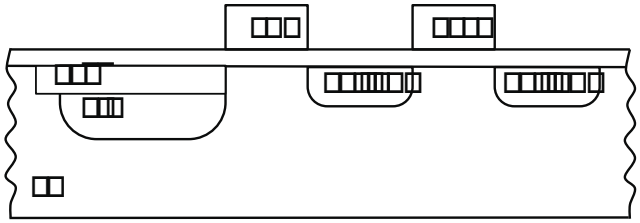
7.2 Pixel Design

In this section, I explain the pixel design details of our first array camera and calculate the performance parameters according to the designed pixel.

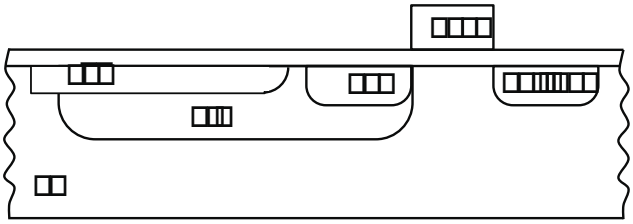
7.2.1 Implementation of 4T APS Pixel in Standard CMOS

As mentioned in Chapter 6, 4T APS pixels are the pixel choice for this and the VGA camera chip (see Chapter 8 for details), since these pixels solve the trade-off between the photodiode capacitance and the conversion gain, and allow implementation of true CDS. However, 4T APS designs especially in standard CMOS processes may suffer from image lag problems when the charges at the photodiode node are not completely transferred to the floating diffusion node. To solve the image lag problems in CMOS image sensors, the pinned photodiode (PPD) technique was suggested for CMOS image sensors [Fossum, 1994], which was already a well-known technique for CCDs [Fossum and Hondongwa, 2014]. The PPD technique eliminates the image lag by creating a buried-diode structure with a p^+ cap layer. Then, the n layer could fully be depleted [Fossum and Hondongwa, 2014]. The emerging structure is a p^+np, which is similar to our p^+/n-well/p-sub type photodiode except that our photodiode has a lightly doped n-well beneath the p-cap instead of a well defined n^- region as in CIS dedicated technologies. Fig. 7.2a shows the standard implementation of PPD.

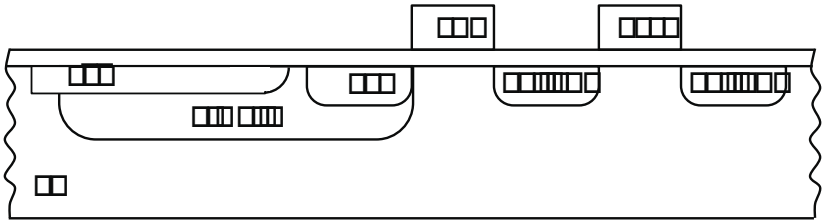
The Partially Pinned PhotoDiode (P-PPD) was introduced as an adaptation of the PPD to 3T APS designs in order to increase the fill factor by eliminating the transfer transistor between the photodiode node and the floating diffusion node [Guidash et al., 1999]. As seen in Fig. 7.2b, this design has p^+ cap layer as a channel stopper on top of a n^- diffusion layer similar



(a) Pinned Photodiode



(b) Partially Pinned Photodiode [Guidash et al., 1999]



(c) Proposed Partially Pinned Photodiode in Standard CMOS with 4T APS Pixel

Figure 7.2: Cross Section of Different Photodiode

to the standard PPDs. However, it also includes the source diffusion of the reset transistor represented by n^+ region within the photon collection region.

The p^+/n-well/p-sub type photodiode that I have used for the camera chips throughout this thesis is basically the adaptation of the PPD to standard CMOS technology. Since in standard CMOS technology, the implementation of PPD as in Fig. 7.2a is not possible, we are obliged to transfer the design towards a P-PPD [Guidash et al., 1999]. However, as mentioned earlier, the 3T APS does not allow true correlated CDS so that the P-PPD does not eliminate the reset noise. Thus, we implemented a P-PPD with 4T APS pixel, which is shown in Fig. 7.2c by using the p^+/n-well/p-sub type photodiode. This type of photodiode also reaches the highest responsivity according to the characterization chip's silicon results that I have presented in Chapter 6.

Fig. 7.3 illustrates the charge transfer mechanism in this adapted P-PPD implementation. As seen in the figure, this method also transfers the complete charge from the PD node with the help of the channel stopper p^+ cap. Since the parasitic capacitance of the n^+ diffusion inside n-well is much smaller than the floating diffusion capacitance, the charge sharing between these two diffusion regions will be neglected during the calculations.

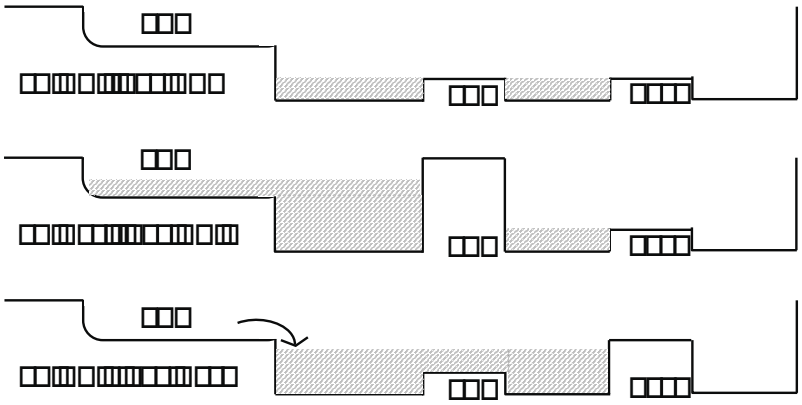


Figure 7.3: Charge Transfer Mechanism in 4T APS P-PPD

Fig. 7.4 presents the pixel schematic and 2×2 pixel array layout of this small array camera chip. I estimate the required pixel size by using the optical resolution formula in Eq.3.2 since the use of smaller pixels than what this formula gives does not improve output quality. Considering the use of a 100X magnification objective with NA=1.4 and wavelength at 550nm, I find the required pixel pitch as 11.95µm, which guarantees to reach the diffraction limit.

$$\text{Required Pixel Pitch} = \frac{1}{2} \times Roptical \times Magnification$$

$$= \frac{1}{2} \times 239nm \times 100$$

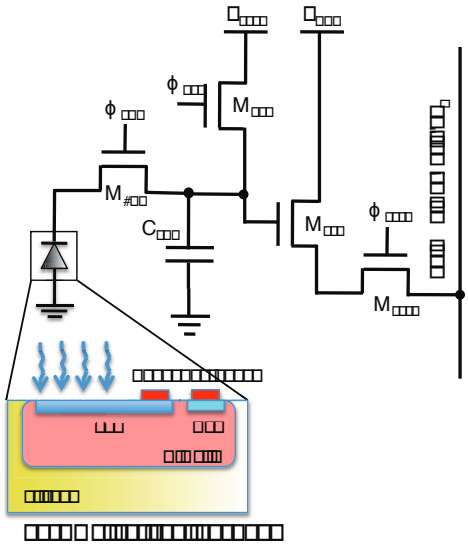
$$= 11.95\mu m$$

When I optimize the pixel size with the defined sensor area, I reach a pixel size of 9.14µm × 14.63µm, which provides spatial resolution of 239nm and 293nm in horizontal and vertical directions respectively.

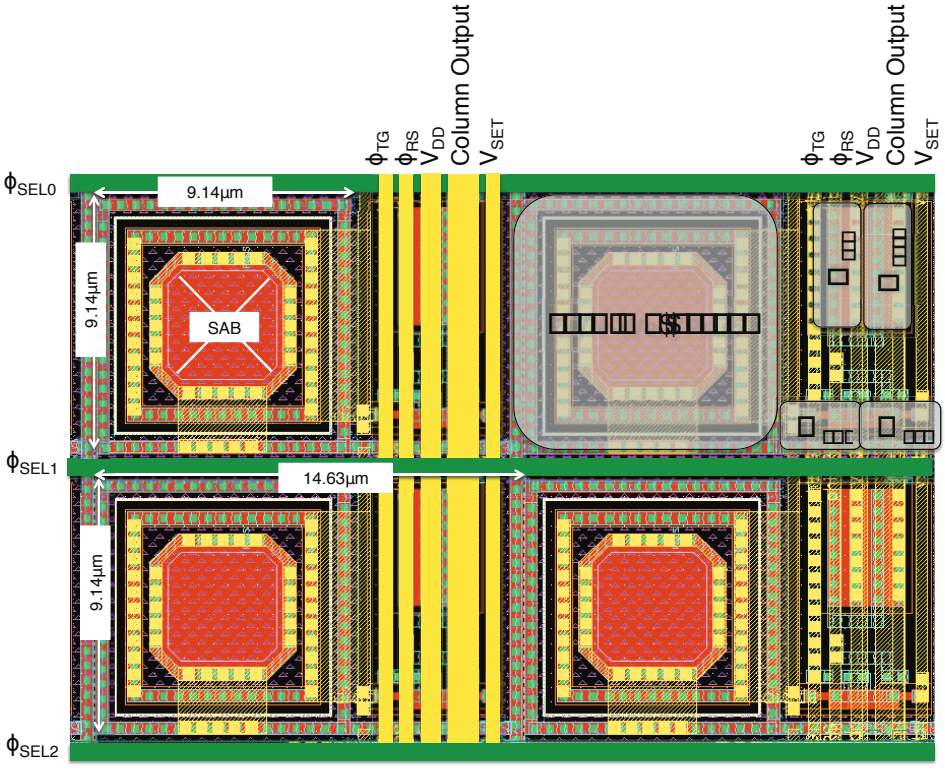
The diffusion area of the design has rounded corners to reduce the dark current, since it was shown in the literature that a finger type photodiode with three fingers and all inner and outer corners rounded (6 corners of each) have reached %30 lower dark current than the same photodiode with no rounded corner [Shcherback et al., 2002]. Also, the diffusion area of each photodiode is covered with a salicide block layer (SAB) with minimum required distance from the metal layer. This area is marked by SAB on the left top photodiode in Fig. 7.4b. Finally, all photodiodes are surrounded by guard rings (contacts to substrate) to avoid cross talk between the pixels and to reduce the dark current [Beiley and Clark, 1999].

7.2.2 Fill Factor

The photodiode area is considered as the area inside the guard ring surrounded by the n-well layer, which has a total area of 9.14µm × 9.14µm. The total pixel area of this design is 14.63µm × 9.14µm. Thus, the pixel fill factor of this design can be calculated as $\frac{9.14 \times 9.14}{14.63 \times 9.14}$ which



(a) Pixel Schematic



(b) Pixel Layout

Figure 7.4: Pixel Design of Our First Camera Chip

results in %62 fill factor.

7.2.3 Full Well Capacity

The N_{sat} of a 4T APS pixel is calculated by Eq.5.4. As shown by the formula, the N_{sat} of this design only depends on the floating diffusion capacitance (C_{FD}) but not on the photodiode capacitance (C_{PD}). C_{FD} which is the total parasitic capacitance at node FD as shown in Fig. 5.2a and is calculated by using Cadence Parasitics option after the parasitic extraction of the pixel layout. According to this calculation, the total C_{FD} is found as 1.622fF. The N_{sat} when calculated with Eq. 5.4 and considering the pixel in soft-reset with V_{SET} at 1.8V, i.e., FD node voltage of 1.7V according to simulations, results in a N_{sat} of:

$$N_{sat} = \frac{1.622fF \times 1.7V}{1.60217657 \times 10^{-19}C}$$

$$= 17212e^{-}.$$

And the N_{sat} when calculated with Eq. 5.4 and considering the pixel in hard-reset with V_{SET} at 1.2V i.e., FD node voltage of 1.14V according to simulations, results in a N_{sat} of:

$$N_{sat} = \frac{1.622fF \times 1.14V}{1.60217657 \times 10^{-19}C}$$

$$= 11542e^{-}.$$

In this design, I control the V_{SET} voltage externally through an off-chip DAC, thus I have the flexibility to change the pixel reset mode as well as the N_{sat}.

7.2.4 Conversion Gain

The Conversion Gain (CG) of the 4T APS is $G_{SF} \times \frac{1}{C_{FD}}$ as mentioned earlier. When the gain of the source follower transistor (G_{SF}) is simulated by Cadence Spectre Simulator, it is found as 0.865 (V/V). Thus, the resulting CG for this design is

$$CG = 0.865 \times \frac{1}{1.622fF} = 0.865 \times \frac{1}{1.622 \times 10^{-15}}(V/C) = 85.43(\mu V/e^{-}).$$

$$(1Columb = 6.24150965(16) \times 10^{18}(e^{-}))$$

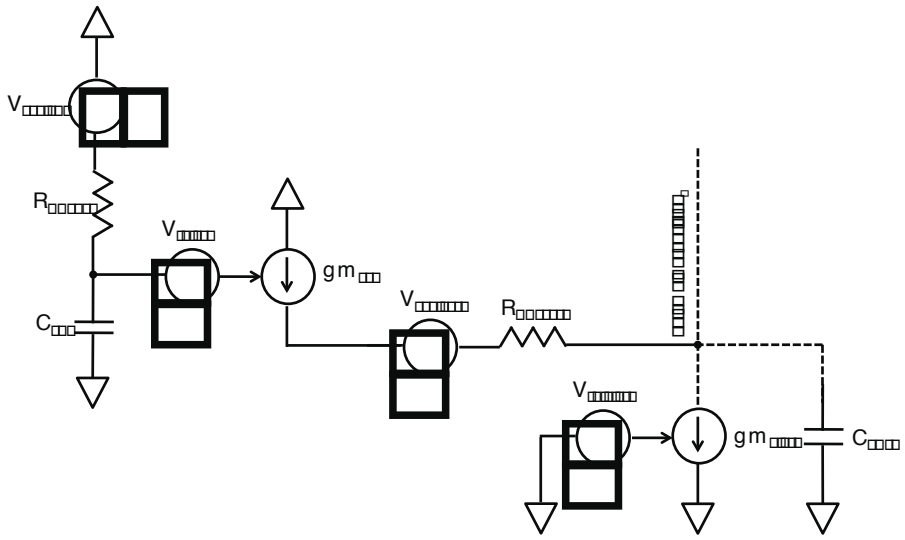


Figure 7.5: 4T APS Pixel Noise Model

7.2.5 Noise Sources

I have already defined the noise sources that are present in CMOS image sensors in Chapter 3, which are mainly grouped under temporal and spatial noise sources. In this section, I will explain the relationship of these noise sources with the pixel level transistors.

For the calculations of the noise in the pixel, following parameters shall be needed:
k: Boltzman's constant (1.38×10^{-23}(J/K))
T: Absolute temperature (K) (i.e. 300(K))
q: Elementary charge (1.6×10^{-19} (C))

7.2.5.1 Temporal Noise

Temporal noise in a pixel contains photon shot noise, dark current shot noise, flicker noise, reset noise, and thermal noise. Since each of these noise sources are independent from each other, the total temporal noise power is the total noise power of each of these noises and can be approximated as

$$\overline{v_{pixel}^2} = \overline{v_{photon,shot}^2} + \overline{v_{darkcurrent,shot}^2} + \overline{v_{flicker}^2} + \overline{v_{reset}^2} + \overline{v_{thermal}^2} \tag{7.1}$$

The temporal noise sources in this pixel can be modeled as in Fig. 7.5. Since the charge transfer from the photodiode node to the floating diffusion node is considered to be noiseless, the M_{TG} transistor is not included in the noise model. In addition, the column level noise contributors, e.g. bias transistor's thermal noise, should also be neglected for pixel level noise calculations although it is presented in this figure.

Reset Noise or kTC Noise due to M_{RS} Reset noise originates from the uncertainity of the amount of charge on a capacitor after charging that capacitor through a resistor. Thus, the reset noise due to the M_{RS} is caused by the reset of the FD capacitor through the on-resistance of the M_{RS} switch. The reset noise in this case depends on the operation mode of the reset transistor (M_{RS}). If M_{RS} transistor works in the saturation region by having its $V_{DS} \geq V_{GS} - V_{th}$, then this type of reset is called soft reset. On the other hand, if the M_{RS} transistor works in the linear region by having its $V_{DS} < V_{GS} - V_{th}$, then this type of reset is called hard reset. Both of these reset types have advantages and disadvantages. A soft reset results in approximately $1/\sqrt{2}$ less noise than a hard reset, while it causes image lag due to a longer time required for the reset voltage to settle [Nakamura, 2005]. On the other hand, hard reset suffers from higher reset noise but it has no image lag issue.

In this pixel design, I used a different voltage than V_{DD} for controlling the drain voltage of the M_{RS} transistor in order to test the camera both in hard and soft reset. In any case, since the design is implemented with a true CDS operation, it is expected to see no burden in terms of the reset noise. Still, the design has the flexibility in changing the V_{SET} voltage controlled by an off-chip Digital to Analog Converter (DAC). The M_{RS} transistor's threshold voltage (V_{th}) is approximately equal to 600mV. Thus, while the V_{DD} of the pixel and the high voltage value of the RST pulse are 1.8V, any V_{SET} voltage lower than 1.2V will guarantee hard reset operation and higher than 1.2V will put the device under soft reset. We will present the relationship with the noise generated on the FD capacitance with respect to the V_{SET} voltage in Section 7.5.

The reset noise in rms voltage and in number of electrons when the reset is sampled on the floating diffusion capacitance are calculated by the following formulas respectively [Nakamura, 2005]

$$v_{kTC,FD} = \sqrt{\frac{kT}{C_{FD}}} \quad [V] \tag{7.2}$$

$$n_{kTC,FD} = \frac{CG}{v_{kTC,FD}} = \frac{\sqrt{kTC_{FD}}}{q} \quad [e^-] \tag{7.3}$$

where CG represents the conversion gain that is calculated in section 7.2.4. It can be concluded from these equations that this noise is a function of the temperature and the capacitance value only, and thus it is called kTC noise.

Thermal Noise or Johnson Noise on the M_{SF} This type of noise is generated in resistors and the channel of MOS transistors. In this pixel architecture, the source follower transistor M_{SF}'s channel cause the thermal noise to appear.

The thermal noise at the gate of the M_{SF} transistor in (V) can be modeled with the following

formula [Nakamura, 2005]:

$$\frac{\overline{V_{th}}}{\sqrt{\Delta f}} = \sqrt{\frac{4kT \times \alpha}{gm}} \; [V/\sqrt{Hz}] \tag{7.4}$$

where Δf is the bandwidth in Hz, gm is the transconductance of the device, and α depends on the operating region of the transistor (considered 2/3 for device under saturation).

In order to reduce this type of noise, the operating temperature of the sensor should be kept under control, the bandwidth should be optimized or the bias current should be increased.

kTC Noise due to M_{SEL} Similar to the kTC noise due to the M_{RS} transistor, this noise appears due to the charging of the load capacitance through the M_{SEL} transistor. The load capacitance is determined by the total capacitance at the column, which is much larger than the FD node capacitance. Thus, the resulting kTC noise due to the M_{SEL} transistor is expected to be much smaller than the reset noise.

Flicker Noise Flicker noise is usually modeled as a voltage source at the gate of a transistor. In this pixel architecture, the flicker noise mainly appears at the M_{SF} transistor and can approximately calculated as [Nakamura, 2005]:

$$\overline{V_{1/f}} = \sqrt{\frac{K_f}{C_{ox}WL} \times \frac{\Delta f}{f}} \; [V] \tag{7.5}$$

where K_f is a process-dependent constant, and Cox, W, and L denote the gate capacitance per unit area, width, and length of the gate, respectively. Thus, this noise source is dominating in low frequencies (lower than 300kHz [Radmanesh, 2008]) since it is inversely proportional to the frequency. In this design, the size of the M_{SF} is relatively large compared to the other transistors, which decreases the flicker noise. In addition, the CDS circuit may generate extra flicker noise. In order to avoid that, the sampling in CDS should be faster than approximately 300kHz. Moreover, the sampling of the reset and the signal should be done as close as possible to each other to avoid introducing extra 1/f noise.

Photon Shot Noise and Dark Current Shot Noise Shot noise is an inevitable noise source for all the imaging systems since it originates due to the discreet nature of electric charge. The dark current shot noise originates from the statistical variation on the number of dark current generated electrons and the photon shot noise originates from the statistical variation on the number of photons falling on a pixel and this on the number of generated electrons. Dark current shot noise is a temporal noise and it can be reduced by lowering the temperature and having an optimized layout. On the other hand, photon shot noise is totally ramdom, it cannot be characterized or reduced and there is no countermeasure for that type of noise.

The photon shot noise and dark current shot noise both depend on the integration time (t_{int}) of the sensor, which are represented by the following formulas:

$$\overline{n_{photon,shot}} = \sqrt{\overline{N_{sig}}} = \sqrt{\frac{I_{photon} \times t_{int}}{q}} \quad [V] \tag{7.6}$$

$$\overline{n_{dark,shot}} = \sqrt{\overline{N_{dark}}} = \sqrt{\frac{I_{dark} \times t_{int}}{q}} \quad [e^-] \tag{7.7}$$

where I_{photon} is the current flowing on the photodiode when the sensor is exposed to a certain amount of light and I_{dark} is the current flowing on the photodiode when the sensor is in dark. When the photo or dark current is multiplied with the integration time (t_{int}), a certain amount of voltage drop can be observed at the pixel output. This can be formalized as following:

$$\overline{v^2_{photon,shot}} = \frac{q \times (V_{RESET} - V_{SIGNAL})}{C_{FD}} \quad [V^2] \tag{7.8}$$

$$\overline{v^2_{dark,shot}} = \frac{q \times (V_{RESET} - V_{DARK})}{C_{FD}} \quad [V^2] \tag{7.9}$$

where $V_{RESET} - V_{DARK}$ represents the voltage drop at the pixel output from the reset voltage after a certain integration time when the sensor is under dark and $V_{RESET} - V_{SIGNAL}$ represents the voltage drop from the reset voltage again after a certain integration time when the sensor is under light.

7.2.5.2 Spatial Noise

Pixel level FPN can be grouped as dark FPN (non-uniformities on dark current generation (Q_{DSNU})) and light FPN (non-uniformities on pixel response (Q_{PRNU})) both of which are generated due to the mismatches occurred during the fabrication of the chip and caused by the variations in gain and offset, V_{th} voltage, current, and parasitics between one pixel to another. As mentioned earlier, the Q_{DSNU} can be mostly canceled by both DDS and CDS operations. However, column level FPN may occur due to these column parallel DDS and CDS circuits or column parallel ADCs. This additional FPN can be canceled by off-chip processing or by chip level CDS operations.

7.3 Noise Reduction with CDS

Among the listed noise sources above, a true CDS implementation decreases reset noise, 1/f noise and offset of the source follower and leaves the photon shot noise, dark shot noise and noise due to the gain mismatch of the source follower unchanged. Although a DDS implementation succeeds in reducing most of the noise sources as CDS, it increases the reset noise since the reset and signal sampling are not correlated. Since the reset noise is the dominant noise source in a pixel, canceling this noise is as important as canceling FPN. Thus, instead of a DDS implementation, a true CDS should be implemented for low light imaging applications.

In Fig. 5.3, a simple implementation of true CDS has been shown with its timing diagram in Fig. 5.4b. The traditional CDS implementation consists of sample and hold capacitors, C_S and C_H, Sample and Hold (S/H) switches controlled by ϕ_S and ϕ_R clocks, a differencing switch ϕ_Y, and a differencing single ended amplifier as seen in Fig. 5.3. In most of the single ended pixels, CDS differencing operation is performed by two buffers [Degerli et al., 1999]. Another method is to use a unity gain configured switched capacitor single ended amplifier instead of two buffers [Chae et al., 2011]. However, both of these methods provide pseudo-differential outputs and they require an additional step to convert the pseudo-differential outputs to fully differential outputs before connecting them to the ADC stage, In order to that, extra conversion circuits integrated with fully differential OTAs are commonly used [Degerli et al., 1999]. Although, the extra pseudo-differential to fully differential conversion circuits give the flexibility to increase the gain with the capacitance ratios, they almost double the CDS area in each column and cause a decrease in the fill-factor. That is why, I propose two alternative circuits for true CDS operation, which use fully differential switch capacitor design method, provide fully differential output in nature, and do not require extra pseudo-differential to fully differential conversion step [Köklü et al., 2011]. In the literature, similar implementations can be found. However, these designs are either limited to differential pixels [Huang et al., 2007] or require complex switching operations and results in increased kTC noise [Decker et al., 1998]. As opposed, the two architectures that I propose within the scope of this thesis offer a very simple solution with an easy clocking scheme.

7.3.1 Fully Differential Switch Capacitor CDS Circuit

Fig. 7.6 shows the first proposed CDS circuit (CDS1) together with the pixel circuit. The amplifier basically operates as a unity gain buffer [Enz and Temes, 1996] with additional two sampling switches as ϕ_S and ϕ_R in order to charge the pixel value before and after integration.

In this architecture, first at ϕ_{RS}, the pixel is in reset condition through the MRS transistor. After the reset operation, when ϕ_R is high, pixel reset value is charged on the capacitor C_R together with the amplifier offset and the capacitor value becomes $V_{reset} + V_{os}/2$. Later, ϕ_{TG} becomes high and the photon-charges at the photodiode node is converted to voltage at the FD node of the pixel through the M_{TG} transistor. With this operation, the PD node is reset and

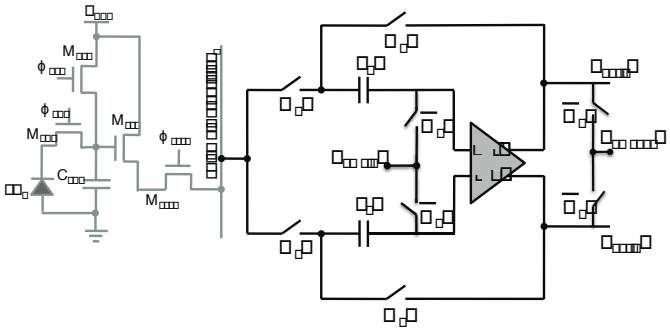


Figure 7.6: Proposed Fully Differential CDS Architecture - CDS1

its charges are transferred to the FD node. Then, the ϕ_S becomes active and the pixel value after integration is sampled on the capacitor at the negative input terminal of the amplifier and the capacitor is charged to $V_{sig} - V_{os}/2$. Finally, at ϕ_Y phase, pixel value after integration is subtracted from the pixel value at reset and the final value is found as $V_{reset} - V_{sig} - V_{os}$.

There are few problems about this CDS architecture that should be addressed. First of all, this architecture requires the op-amp output to be reset at each clock cycle, which decreases the effective timing of the op-amp by half and makes the slew rate and the settling time requirements of the op-amp difficult [Enz and Temes, 1996]. However, although this is an important concern for sample and hold circuits, analog memories and delay stages where unity gain buffers are widely used, it is not an issue for this application since the timing intervals are already determined in the pixel section, and a final "subtracting" clock ϕ_Y is inevitable. However, there are still two other problems that should require more careful examination which are amplifier offset problem and gain mismatch between column level amplifiers. The CDS1 architecture neither provides gain compensation nor offset compensation where both of these parameters introduce column level FPN to the image sensor. In the following section, I propose a new CDS design (CDS2) that solves the offset problem. I neglected the gain mismatch problem in between column level amplifiers since correcting this problem with a chip level correction circuit or with post-processing instead of a column level implementation would require less silicon area.

7.3.2 Offset Compensated Fully Differential Switch Capacitor CDS Circuit

The second CDS implementation (CDS2) has two additional capacitors to charge the offset of the amplifier during the $\overline{\phi_Y}$ phase. Then, while in ϕ_Y phase, offset that is charged on the offset capacitors are subtracted from the pixel voltage before and after integration. Fig. 7.7 presents the details of this architecture. In this architecture, during ϕ_R phase, not only the reset voltage of the pixel is charged on the C_R capacitor, but also the differential inputs of the amplifier are shorted to the differential outputs in order to avoid the floating gate problem at the amplifier input. Fig. 7.8 shows all switching phases of this circuit starting from the reset to the differential differencing operation.

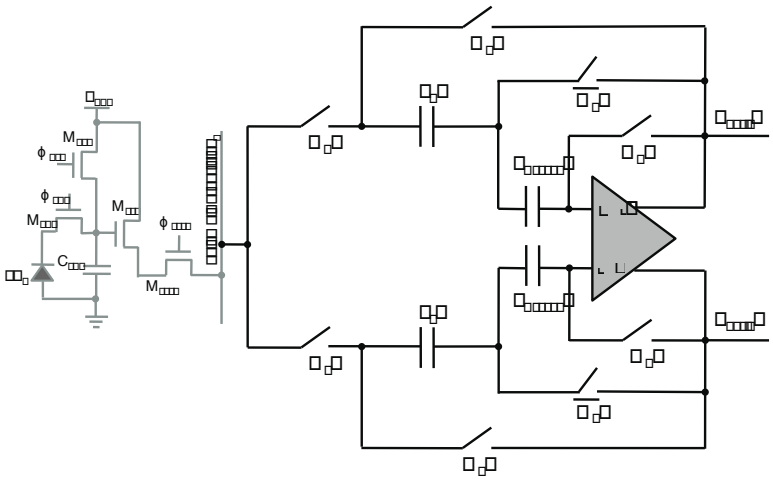
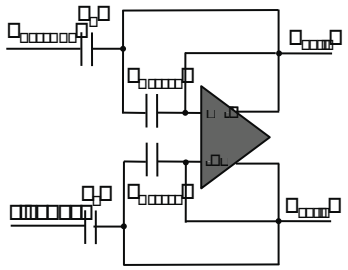
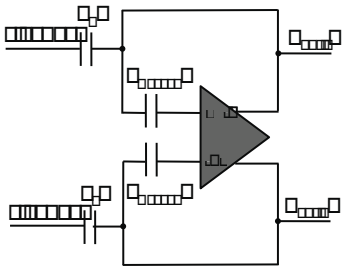


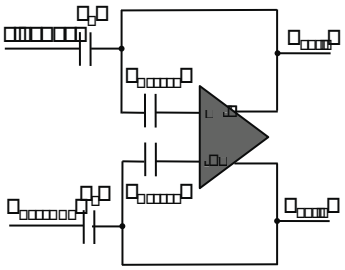
Figure 7.7: Improved Fully Differential CDS Architecture with Offset Compensation - CDS2



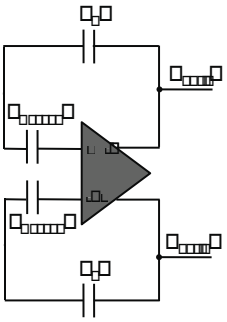
(a) ϕ_R is ON, pixel reset value is charged on C_R and initial values are set at the op-amp input terminals.



(b) ϕ_R and ϕ_S are both OFF, offset is charged on C_{offset}



(c) ϕ_S is ON, pixel voltage after integration is charged on C_S



(d) ϕ_Y is ON, pixel value after integration is subtracted from the pixel reset value together with amplifier offset.

Figure 7.8: Improved CDS Switching Phases

The first CDS architecture cancels pixel offset and the reset noise, while the second architecture cancels the amplifier internal offset as well and results in better performance with reduced column level FPN. However, since the design with offset compensation (CDS2), re-

quires 4 capacitors instead of 2, its area overhead is almost doubled. That is why, for our first and VGA camera chips, I used the first CDS implementation, which has no inner offset compensation. The amplifier offset, i.e., column level FPN, in this design will be canceled with image processing techniques.

7.3.3 kTC Noise due to the Double Sampling on the CDS capacitances

The CDS noise cancellation circuit introduces additional noise to the sensor. That is because, similar to the reset noise generated at the FD node, at both sampling activities during CDS operation, there will be kTC noise generated. This noise can be approximated with the following formula:

$$\overline{v_{kTC,R/S}} = \sqrt{\frac{kT}{C_{R/S}}} \tag{7.10}$$

$$n_{kTC,R/S} = \frac{CG}{\overline{v_{kTC,R/S}}} = \frac{\sqrt{kTC_{R/S}}}{q} \tag{7.11}$$

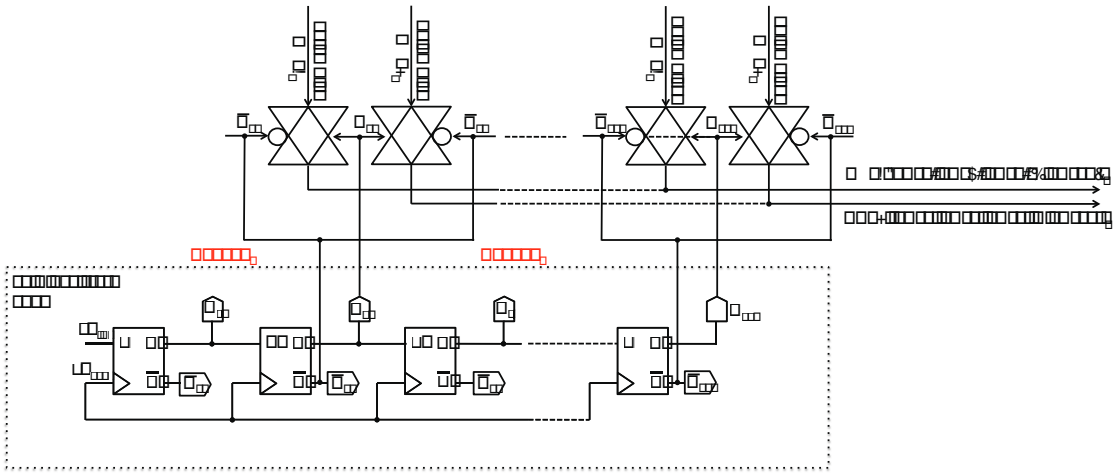
where the $C_{R/S}$ represents the reset or signal sampling capacitors at the CDS circuit. Since these two noise sources are not correlated, they will be increasing the total read-out noise. Due to this reason, these capacitors should be designed as large as possible, in order to keep their impact minimum. For this small array camera chip, I used 800fF capacitors, which results in relatively low kTC noise ($71.9\mu V_{rms}$ for each sampling phase), compared to the pixel reset noise ($1434\mu V_{rms}$). Thus, the double sampling operation will increase the noise approximately $101\mu V_{rms}$ ($\sqrt{2} \times 71.9\mu V_{rms}$) since the two phases are not correlated.

7.4 Horizontal and Vertical Access Circuits

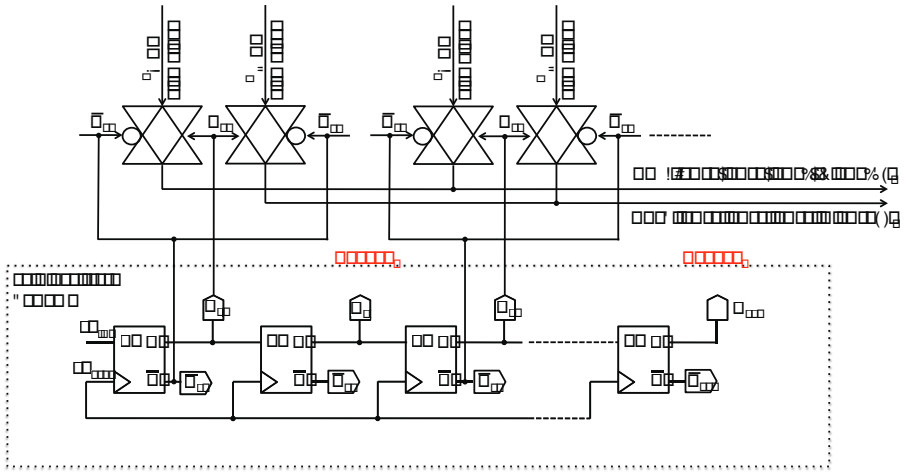
7.4.1 Horizontal Access Circuits

The top and bottom horizontal access circuits are the same except their input connections, the top one is connected to the even numbered CDS outputs, while the bottom one is connected to the odd numbered CDS outputs. Fig. 7.9 shows the schematic of the top and bottom horizontal access circuits.

Two transmission gates are used for each column in order to transfer the differential CDS outputs. The input of one of these transmission gates is connected to the positive output node of the differential output, while the input of the other is connected to the negative output node. The gates of the transmission gates are connected to the shift registers outputs. This action guarantees to read-out one column output at a time and converts the column parallel CDS outputs to serialized outputs. Since there are horizontal access circuits, at the top and



(a) Top



(b) Bottom

Figure 7.9: Horizontal Access Circuits

at the bottom, the serialized output at the top corresponds to the column outputs from the 2nd to the 60th column and the serialized output at the bottom corresponds to the column outputs from the 1st to the 59th column.

7.4.2 Vertical Access Circuit

The vertical access circuit consists of a 6to64 NOR based decoder and 6 bit ripple carry counter. Fig.7.10 illustrates the schematic of this circuit. The select lines of the decoder are controlled by the counter. Each output of the counter is synchronized with the clock of the counter by using additional flip-flops for each output. The NOR based decoder guarantees to have one select line to be active at a time by raising its voltage to V_{DD} through the weak pull-up PMOS transistor. This condition is only valid when all NMOS transistors on the same line are OFF so that the PMOS transistor can pull-up the line to V_{DD}. Thus, the select line of row63 is only

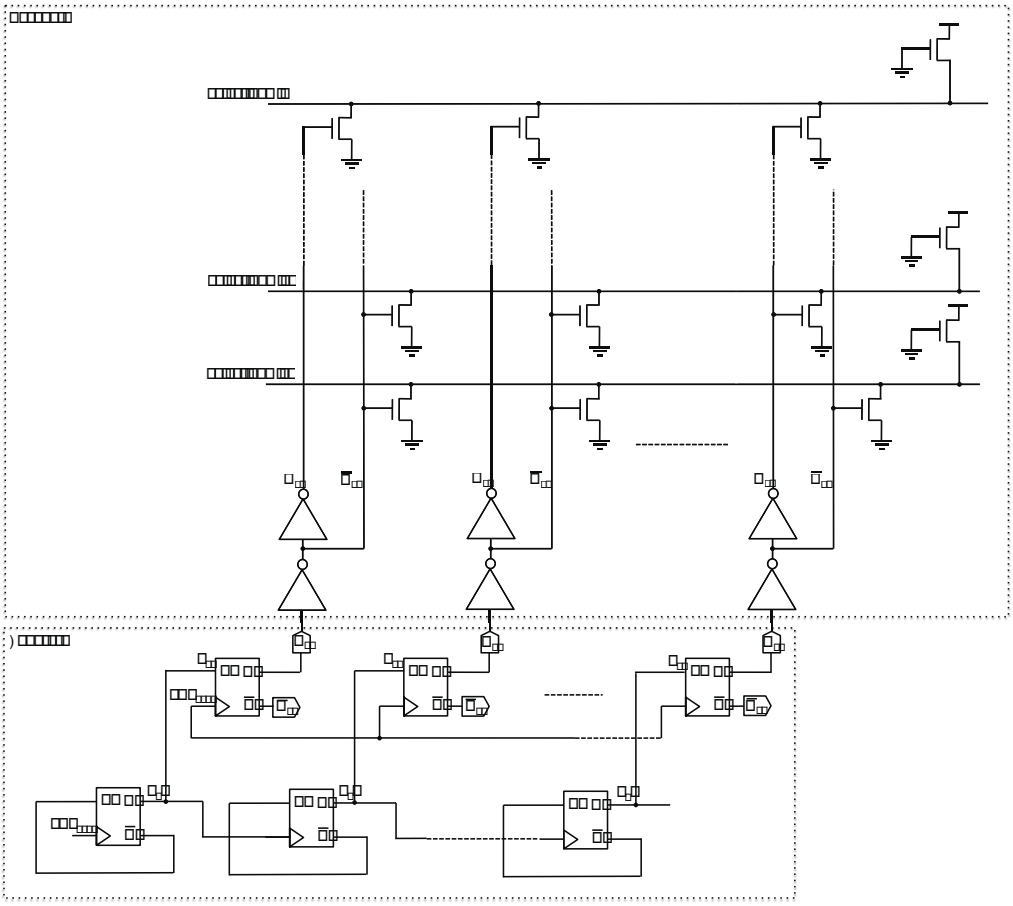


Figure 7.10: Vertical Access Circuit

valid when all the select inputs are 1 and the select line of row0 is only valid when all the select inputs are 0. With this implementation, at each rising edge of the clock of the counter, the value in the counter increments by 1, which changes the selected row through the decoder.

7.5 Simulation Results

7.5.1 Pixel

Transient Behavior Fig. 7.11 shows the transient behavior of the pixel at different photocurrents Iph, which is simulated by using Cadence Spectre Simulator's transient simulation option.

In this simulation, drain voltage of the reset transistor, V_{SET}, is kept at 1.4V. Moreover, in order to be able to show the behavior of the pixel circuit, the M_{TG} transistor is sampled twice, first to reset the photodiode junction capacitance and second to transfer the integrated voltage from the photodiode to the floating diffusion. In this figure, by increasing the Iph, the increase in

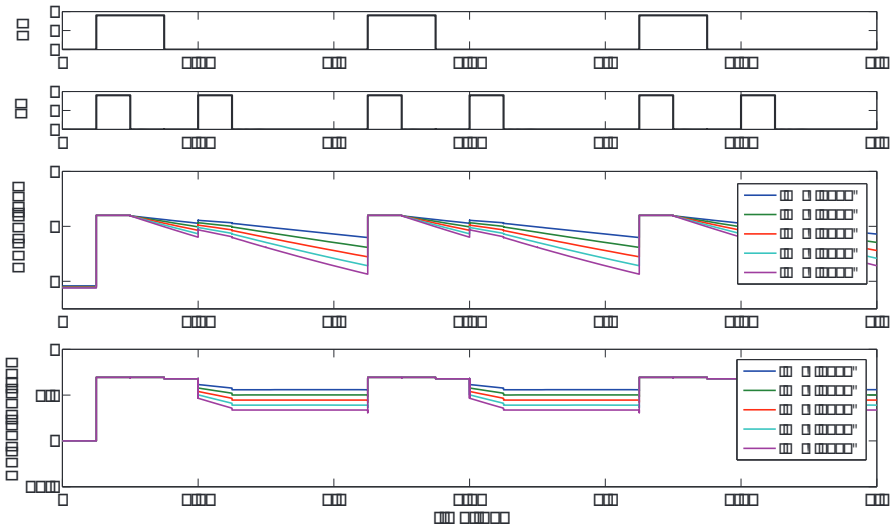


Figure 7.11: Transient Simulation of Pixel Circuit at Different Photodiode Current

the discharge speed of the photodiode capacitance value from the reset value can be observed. The behavior of the circuit at different clock phases is as follows:

- ϕ_{RS} and ϕ_{TG} are ON. The PD and FD node are both reset.
- ϕ_{RS} is ON, ϕ_{TG} is OFF. Keeping the FD node at reset but the PD node starts to discharge.
- ϕ_{RS} and ϕ_{TG} are OFF. The FD node reset voltage will be sampled to the CDS reset capacitor.
- ϕ_{RS} is OFF and ϕ_{TG} is ON. The PD node continues to discharge, this behavior is visible at the output node.
- ϕ_{RS} is OFF and ϕ_{TG} is OFF. The integrated voltage of the PD will be sampled to the CDS signal capacitor.

Thus, similar to the photodiode voltage graph, at the output voltage graph, we observe that by increasing the photo-current Iph, the pixel output voltage difference between the reset and signal sampling phases also increases.

Fig. 7.12 presents the input to output voltage characteristic of the pixel. This graph is obtained by providing a variable photon current (I_{ph}) through the PD node of the pixel, while preserving the usual operation of the pixel. By subtracting the clipped pixel output after reset operation from the clipped pixel output after the completion of the charge transfer from the PD node to the FD node, the pixel voltage change according to different illumination levels is obtained. This operation is repeated for multiple V_{SET} voltages. As seen by the graph, when the V_{SET} voltage is highest at 1.8V, the pixel can handle a voltage difference between reset and integrated voltage value up to 0.95V, while this value is limited to 0.6V when the V_{SET} voltage is at 1.2V. This graph shows us that for the pixel to detect a peak-to-peak voltage of $\approx$ 0.95V, while working in linear mode, the V_{SET} voltage should be at 1.8V.

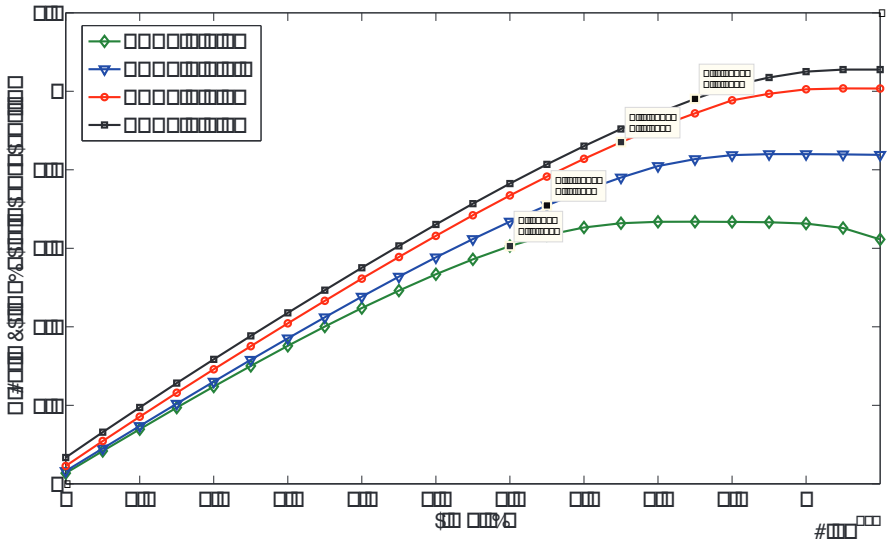


Figure 7.12: Input Output Transient Characteristic of Pixel Circuit at Different V_{SET} Voltages

Noise behavior Fig. 7.13 shows the kTC noise behavior of the reset transistor (M_{RS}), which is simulated by using Cadence Spectre Simulator's Periodic Steady State (PSS) and Periodic Noise (PNOISE) simulations together. In order to simulate the kTC noise or reset noise due to the switching activity of the M_{RS}, a sinusoidal signal with 1µV amplitude and a variable (V_{SET}) DC voltage through the drain of the M_{RS} transistor is applied. The operating frequency during this simulation is 1MHz. By sweeping the V_{SET} voltage, and integrating the noise from 1Hz to 1GHz frequency range, the integrated rms noise as represented in Fig. 7.13 is obtained. As expected, according to this simulation, kTC noise decreases by increasing the V_{SET} voltage. The value 1434µV_{rms} is reached when the transistor is in hard reset, which is close to the theoretical calculation value of 1597µV_{rms} when calculated with Eq. 7.2.

7.5.2 CDS Design Simulations

7.5.2.1 OTA Simulations

The Operational Transconductance Amplifier (OTA) simulations that are presented here are based on the extracted view, which includes the parasitics and provides a more realistic result. The designed OTA is common to both CDS implementations i.e., CDS with and without offset compensation. There are two different simulation setups for simulating the OTA. The first is the open loop configuration to simulate the open loop gain, the phase margin, the Power Supply Rejection Ratio (PSRR) and the Common Mode Rejection Ratio (CMRR) of the design and the second is the closed loop unity gain configuration to simulate the linearity of the design.

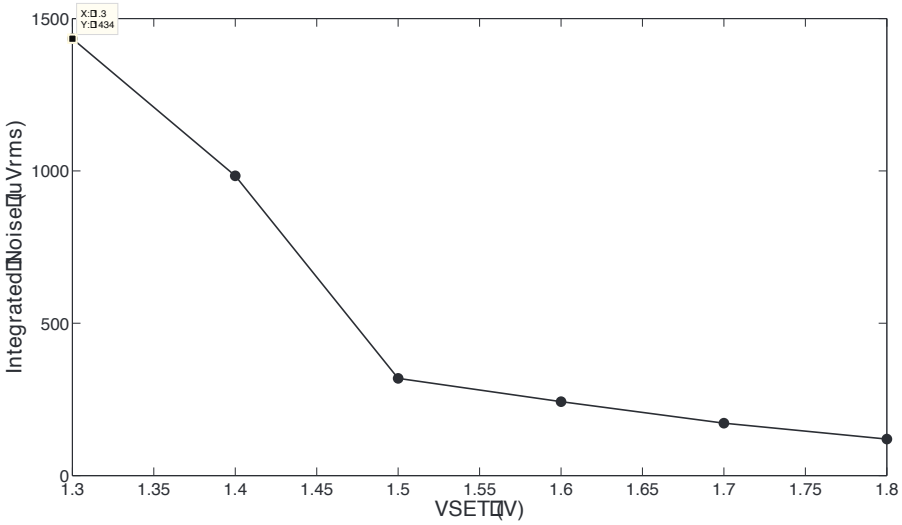


Figure 7.13: Integrated kTC Noise Result at Different VSET voltages

Open Loop The open loop simulation results show 65dB AC gain, 2.5GHz bandwidth, and 50 degree phase margin as shown in Fig. 7.14.

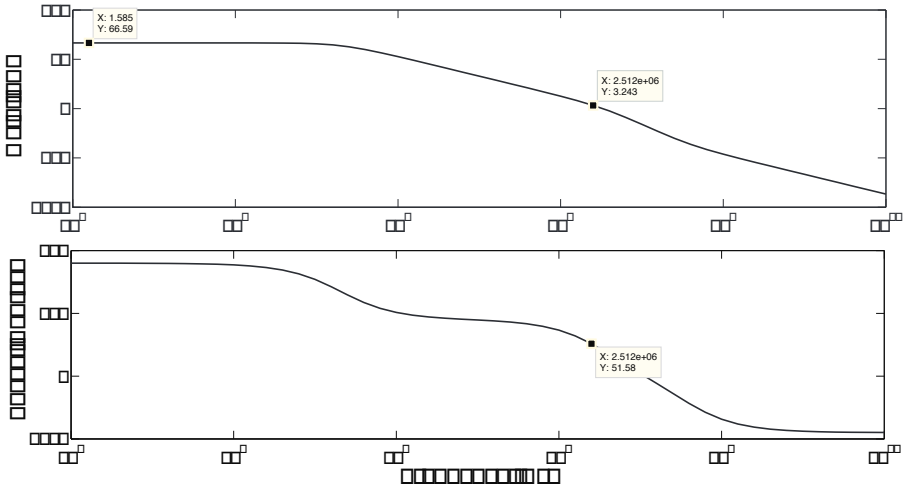


Figure 7.14: Open Loop Simulation of the OTA

Closed Loop The closed loop simulation shows the linearity graph of the OTA output with respect to the input. For this simulation, the OTA is kept at unity configuration and from the differential input terminals, a differential signal with a voltage swing from 0 to 1V is applied. Fig. 7.15 shows the differential output of the OTA being linear until the differential input

reaches 0.91V. Thus, the maximum detectable difference between the reset and the sampling signal at the pixel output should be 0.91V, in order for the CDS to provide linear results. This value is also compatible with the pixel output voltage, which is linear for voltage differences upto ≈ 0.95V.

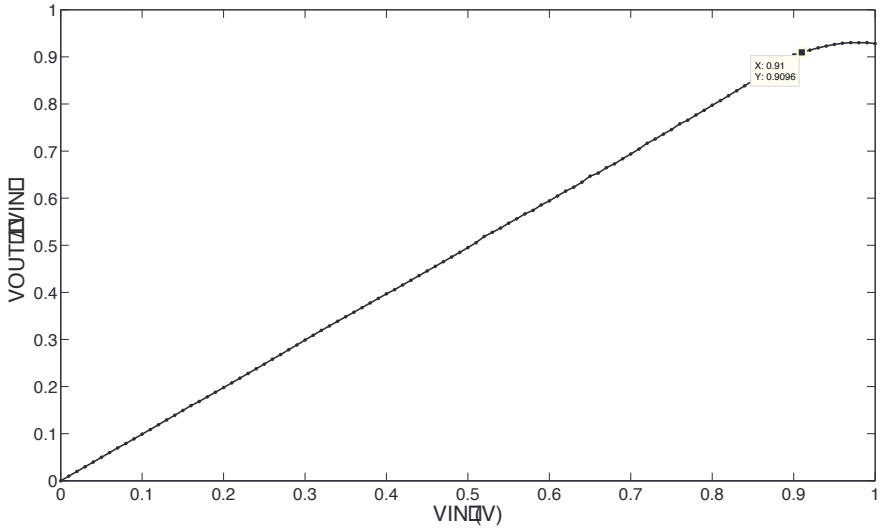


Figure 7.15: Closed Loop Simulation of the OTA in Unity Gain Configuration

Finally, I obtained the CMRR and PSRR results by simulating the process and mismatch variation in the circuit by using the Monte Carlo simulation option of Cadence Spectre Simulator. The results have shown PSRR and CMRR of 66.03dB and 75.05dB respectively. Of course the results presented here do not take into account the improvement in the full-custom layout, which I have payed special attention in designing for increasing the matching.

7.5.2.2 CDS Simulations

Transient Behavior The first simulation in Fig. 7.16 shows the transient behavior of two proposed CDS architectures when a 0.1V sinusoidal signal on a 1.2V DC voltage is applied through the sampling input node of the CDS circuit. The reset input node is kept at constant DC voltage of 1.2V. Fig. 7.16 shows the corresponding results, when the differential output of the CDS circuit is sampled with the activation of the ϕ_Y switch. The correct sampling behavior of the CDS circuit can even be observed for voltage differences of ≈ 0.5mV between the reset and the sampling voltages of the pixel.

The second simulation in Fig. 7.17 shows the comparison of the two CDS implementations with respect to their calculated SNR results at different input signals. This data is obtained by using sampled outputs of these two switched capacitor circuits at different input signals. Then, after corrupting the outputs by applying zero-mean random noise, the SNR graphs are

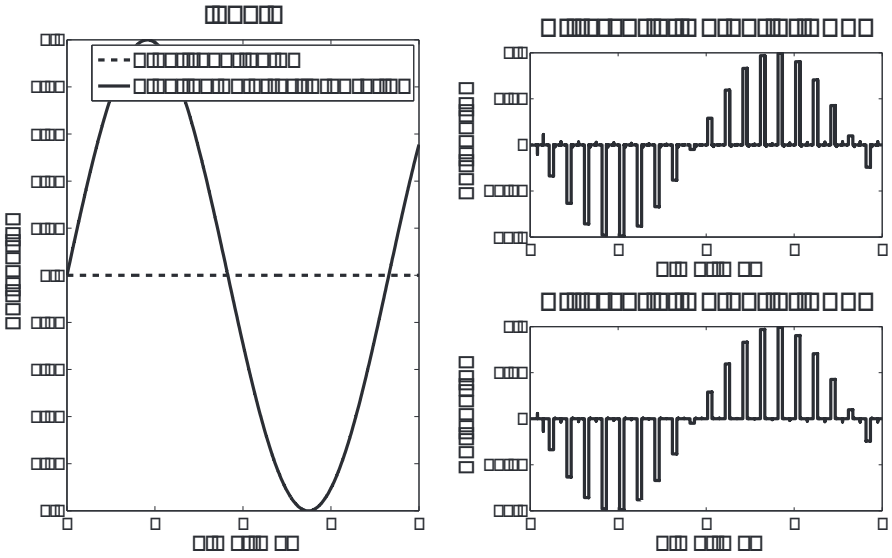


Figure 7.16: Transient Behavior of the Two CDS Architectures

obtained. In this simulation, the reset input is kept constant as in the real pixel and the input signal, which is the voltage drop due to the illumination is varied. When the input signal is 500mV, the highest SNR that is reached with the CDS1 becomes 74.12dB, while it is 81.79dB for the CDS2. Moreover, When the input signal is reduced to 1mV, the SNR achieved by CDS1 goes down to 22.23dB, while it is 32.4dB for the latter. When doing these simulations, the input frequency was set at 137Hz while the sampling frequency was 2.5kHz.

The next simulation in Fig. 7.18 presents a transient simulation for the cancellation of the pixel offset generated by the M_{SF} transistor. In the test bench of this simulation, 50mV DC offset voltage from the gate of the M_{SF} transistor is applied. This added offset does not bother the general behavior of the circuit. However, since its value will vary from one pixel to another, it will cause pixel level FPN and limit the DR of the sensor. This simulation shows us that although the added offset is visible at the pixel output when compared with the simulation result with no offset. However, at the end of the CDS operation, this offset is no longer visible, since the offset is sampled on both C_R and C_S capacitors, it is subtracted by the CDS operation. This behavior can be verified by both CDS architectures.

Noise Behavior Fig. 7.19 shows the noise simulations of the pixel circuit only, the CDS circuit only, and the pixel and the CDS circuit together. This simulation is performed by using Cadence Spectre Simulator's PSS and PNOISE simulations, with periodic beat frequency at 1MHz.

In order to obtain the noise behavior of the CDS circuit only, a sinusoidal input with 1mV amplitude from the common drain of the reset and signal sampling switches is provided. This configuration resulted in a total integrated noise of $283\mu V_{rms}$ at the differential output node

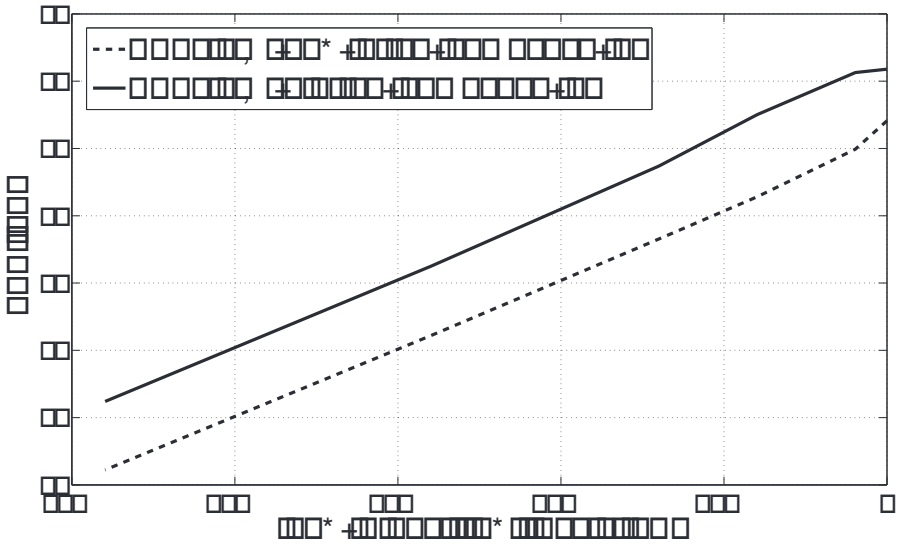


Figure 7.17: SNR Comparison of the Two Architectures

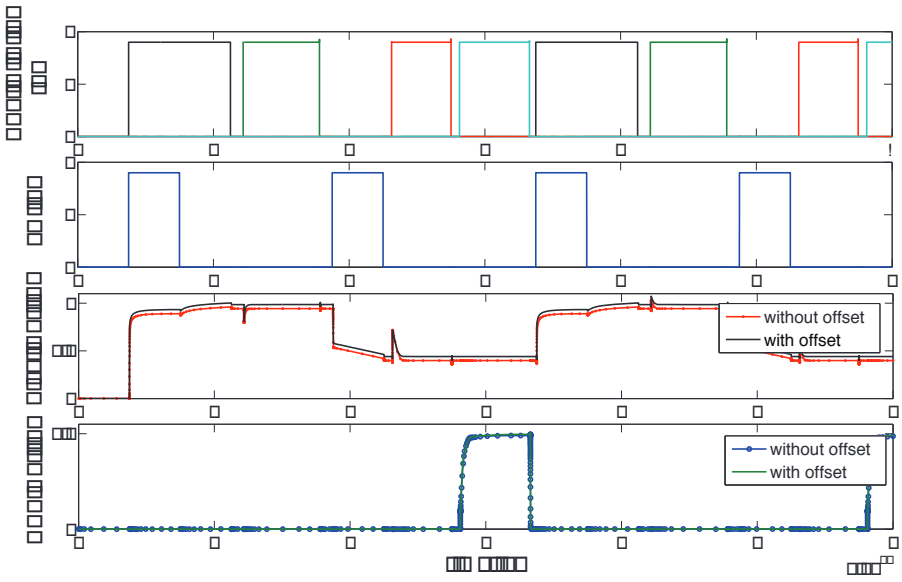


Figure 7.18: Cancellation of Offset with CDS

of the CDS circuit when the frequency is swept from 1Hz to 1GHz.

Then, in order to obtain the noise behavior of the pixel circuit only, a sinusoidal input with 1μV amplitude from the drain of the M_{RS} transistor is provided and the noise at the pixel output is measured. This configuration resulted in a total integrated noise of $1434\mu V_{rms}$ at the floating diffusion node and $1262\mu V_{rms}$ at the pixel output node with the same measurement setup as before.

Finally, in order to analyze the noise reduction with the CDS implementation, a noise simulation by combining the pixel circuit output to the input of the CDS circuit is performed. When these two blocks are connected to each other, a total integrated noise of $285\mu V_{rms}$ is obtained at the CDS output and the contribution of the M_{RS} kTC noise to the overall integrated noise has become negligible ($12\mu V_{rms}$).

Fig. 7.19 shows these noise simulation with the graphs named as Pixel only output noise, CDS only output noise, and Pixel + CDS output noise. It can be seen from this figure that, at the low frequency ranges, the Pixel + CDS output noise is lower than both CDS only output noise and Pixel only output noise, and at higher frequencies, Pixel only output noise becomes slightly higher than CDS only output noise but still much lower than Pixel only output noise.

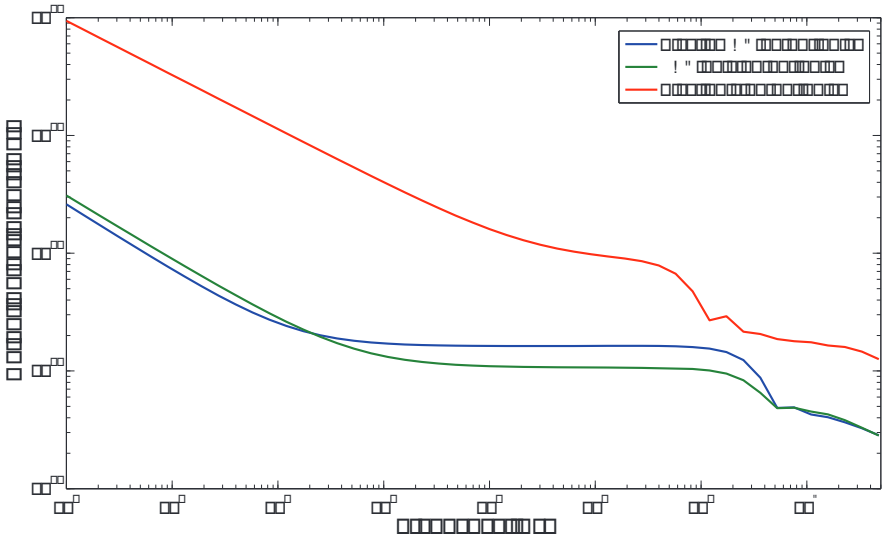


Figure 7.19: Cancellation of Output Noise with CDS

7.5.3 Vertical Access Circuit Simulation

Fig. 7.20 presents the transient simulation result of the vertical access circuit, which is a combined block of a 6 bit counter and 6 to 64 decoder. CLK_{CNT} represents the clock of the counter, which has the same the frequency as the other array clocks. With each rising edge of the CLK_{CNT}, the value in the counter increments by 1 so the select signal of the decoder.

Thus, at each rising edge of the CLK_{CNT}, the selected row within the pixel array is shifted from top to bottom. In this graph, at the beginning of the simulation, Row Sel $<0>$ is active, then with the 1st rising edge of the CLK_{CNT}, the selected row is shifted to the 1st row, Row Sel <1> becomes active, then with the 2nd rising edge of the CLK_{CNT}, the Row Sel $<2>$ becomes active. This continues until the last (63rd) row is selected. Thus, at the end of the 64th clock cycle, the counter is reset and the new frame starts.

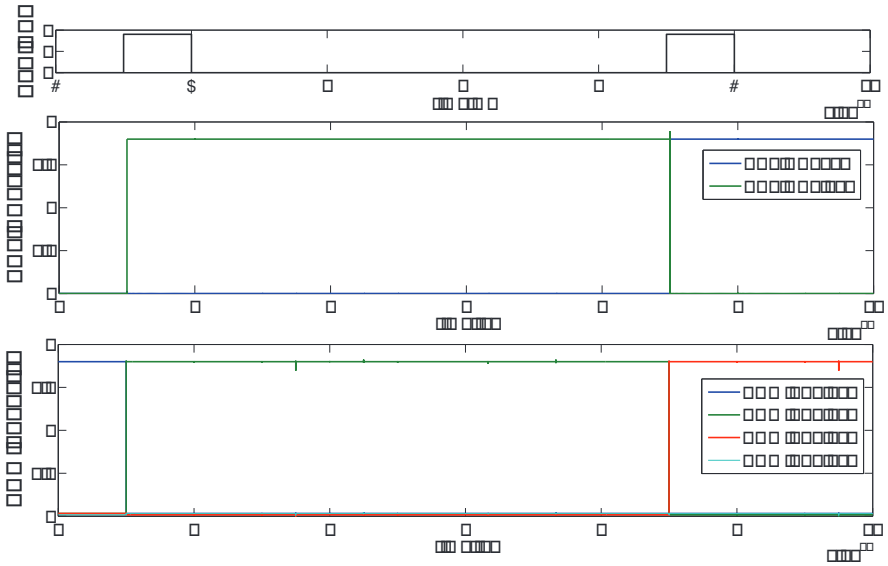


Figure 7.20: Vertical Access Circuit Transient Behavior

7.5.4 Horizontal Access Circuit Simulation

As mentioned earlier, there are two blocks of horizontal access circuits in this design, at the top and at the bottom of the pixel array. The horizontal access circuit at the top outputs the odd numbered Q signals, e.g. Q<1>, Q<3>, Q<5>, and the one at the bottom outputs the even numbered Q signals, e.g. Q<0>, Q<2>, Q<4>, which are used to shift the selected column from left to right. Fig. 7.21 represents the transient behavior of the two horizontal access circuits together. The shift registers require a trigger signal and a clock signal, which are named as Shift Reg Start and Shift Reg CLK in this figure. ϕ_Y signal is the period at which the CDS circuit subtracts the two sampled values and the pixel value is ready at the output. The inverse of the ϕ_Y signal is also connected to the reset of the shift registers. Thus, the whole horizontal access circuit operation is done during ϕ_Y signal clock period. The shift register outputs and their inverses are connected to the transmission gates' control inputs and with this implementation, the CDS output of the selected column is transferred to the output of the chip. The OUT<0:63> signals present the serialized CDS outputs. These output levels are the same for the whole columns for this simulation since there is no additional photon current provided to the system.

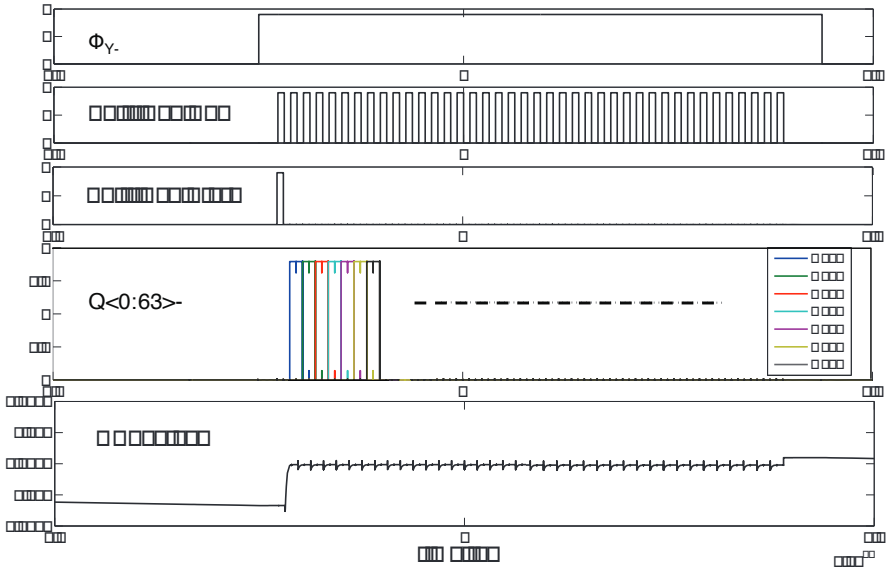


Figure 7.21: Horizontal Access Circuit Transient Behavior

7.5.5 Top Level Simulation

Fig. 7.22 and 7.23 represent the transient simulation of the top level circuit and show the overall behavior of the sensor design. As mentioned earlier, the design works in rolling shutter mode. Each frame starts with the read-out of the 1st row by the activation of the ROW SEL<0>. During this time period, ϕ_{RST} (pixel reset), ϕ_{TG} (pixel transfer), ϕ_R (CDS - reset sampling), ϕ_S (CDS - signal sampling) and ϕ_Y (CDS - subtracting) clocks become active one after the other. During the ϕ_Y phase, starting from the 1st column, each columns are scanned by using the horizontal access circuit. Then, when all columns of the 1st row is read-out, by the increase of the value in the counter in the vertical access circuit, the 2nd row is selected. Again, starting from the 1st column of the 2nd row, all the columns of this row is selected and read out one by one. This behavior continues until the last row (63rd) is selected. After all the columns of 63rd row is also read out, the counter is reset. After the counter reset, the data for the new frame arrives. In this simulation, since there are no photo current flowing through the photodiodes, all the pixel outputs are the same so are the column outputs. Thus, a low output voltage is observed with glitches at the $(TOP\_OUT+) - TOP\_OUT-)$ serialized differential output node. In this simulation, SR IN presents the Shift Register Start signal and SR TOP OUT and SR BOTTOM OUT represent the shift register outputs of the top and bottom horizontal access circuits respectively, which were named together in the previous simulations under Q<0:63>.

The total dc power consumption of the overall design is found as 37.512mW by using the Cadence DC analysis.

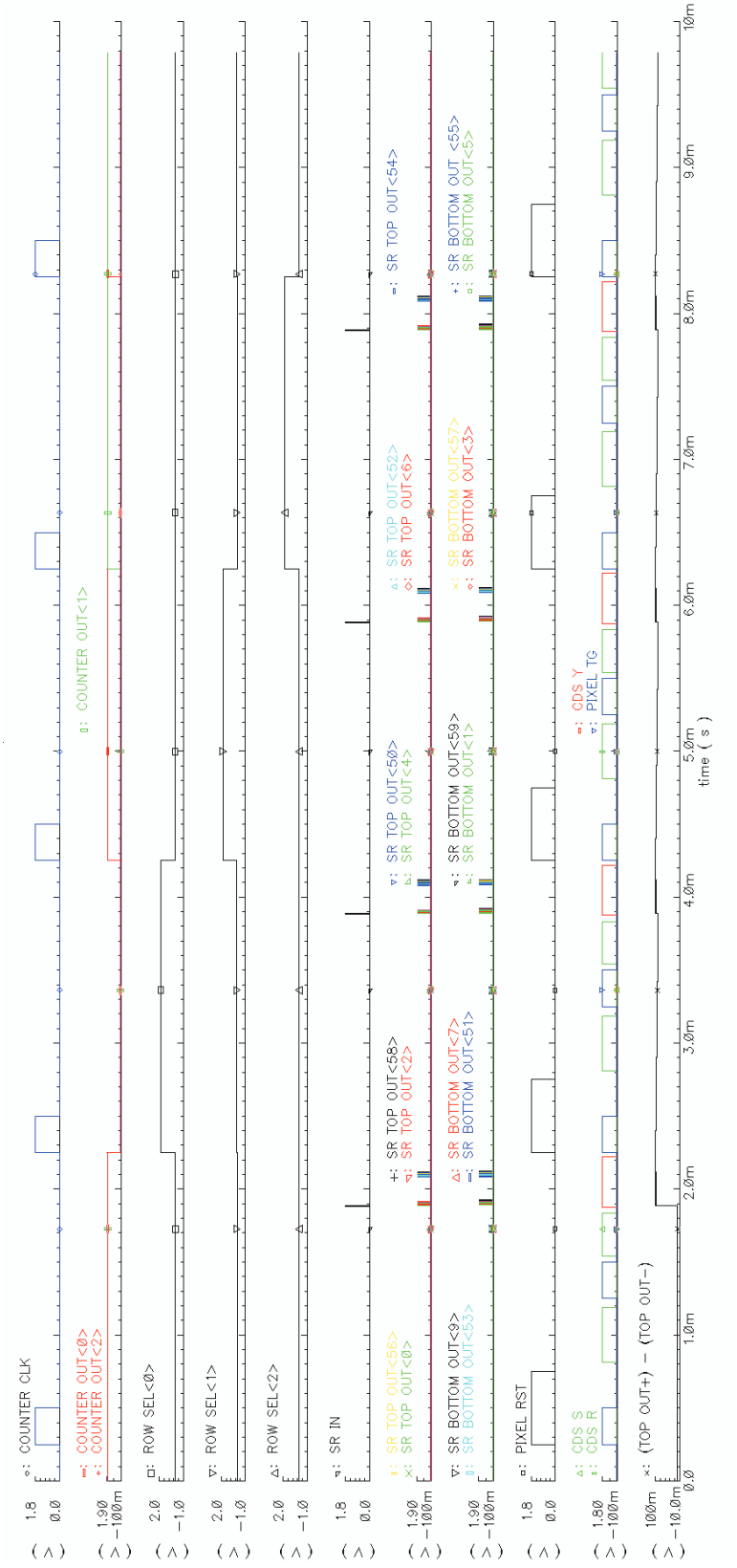


Figure 7.22: Top Level Simulation of the 2nd Camera Chip

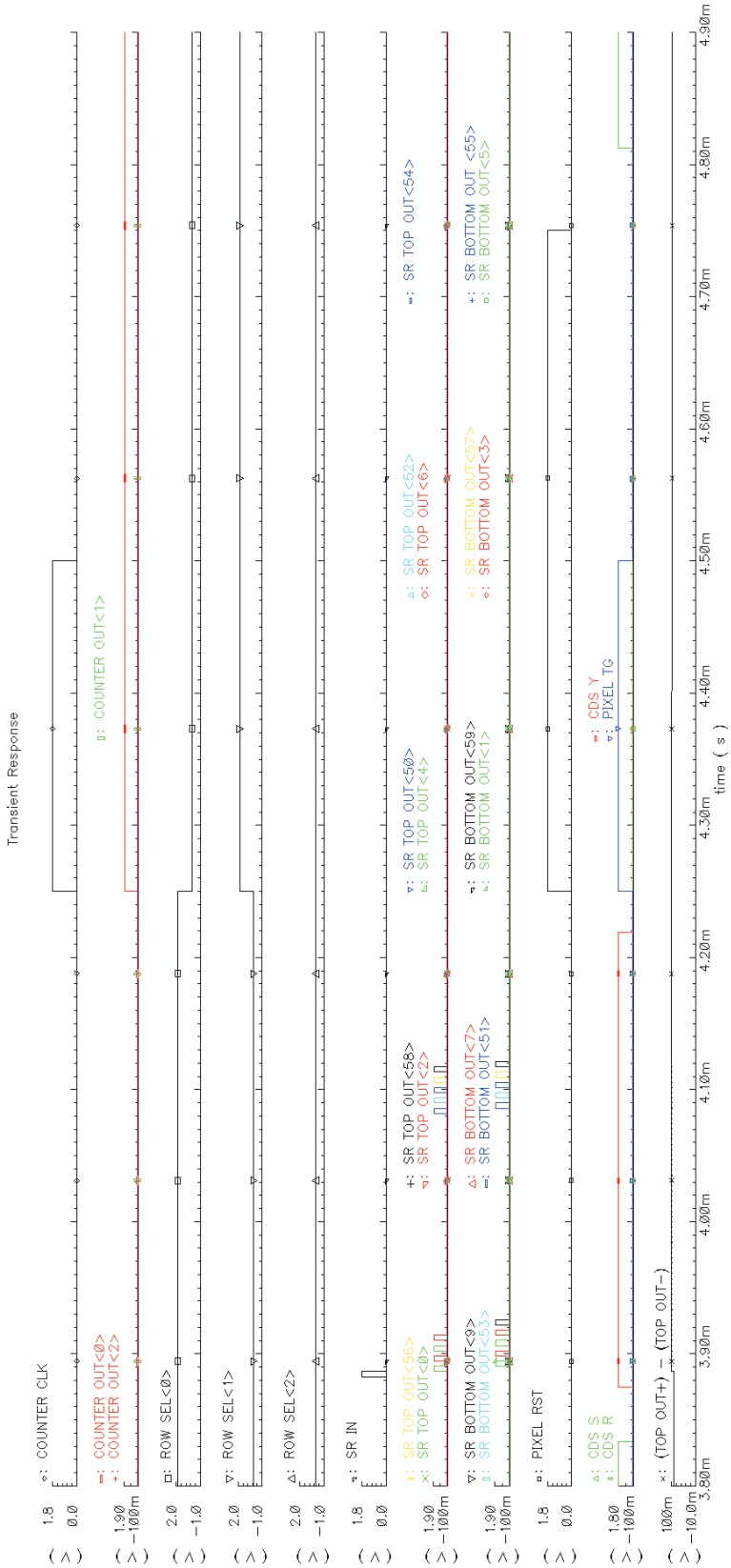
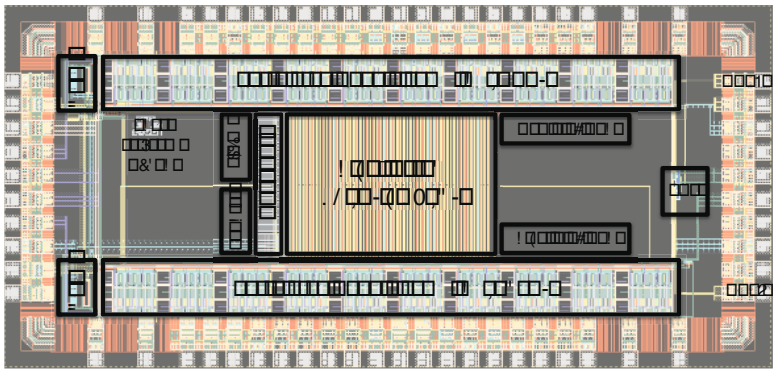


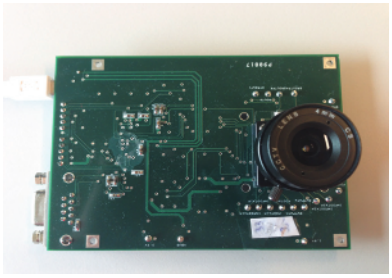
Figure 7.23: Top Level Simulation of the 2nd Camera Chip with More Details

7.6 Measurement Results

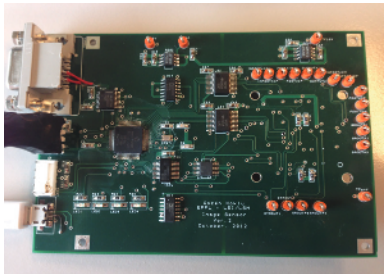
Fig. 7.24a shows the top level layout of this small array camera chip. Fig. 7.24b and Fig. 7.24c present the pictures of the top and the bottom of the PCB that is used to test this camera chip. More details on this PCB will be provided when explaining the image collection interface.



(a) Top Level Layout



(b) Test Board Top



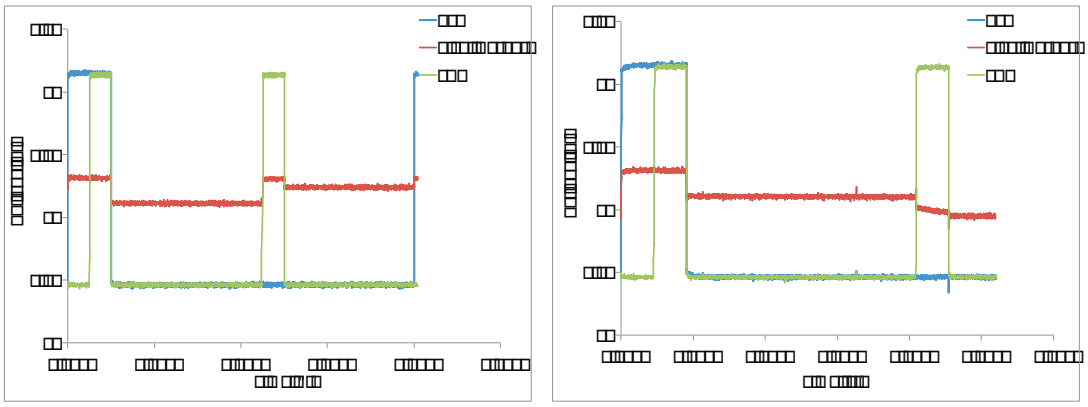
(c) Test Board Bottom

Figure 7.24: Pictures of Layout and the Test Board of the Array Camera Chip

Fig. 7.25a and 7.25b show the behavior of the 4T APS pixel under dark and light conditions. For the measurements under dark, the sensor integration time is 10ms, which results in a voltage drop of 60mV at the pixel output. For the measurements under low-light conditions, the exposure of sensor under the regular office light with ND filters of highest filtering capability results in 180mV of voltage drop at the pixel output for an integration time of 3.6ms.

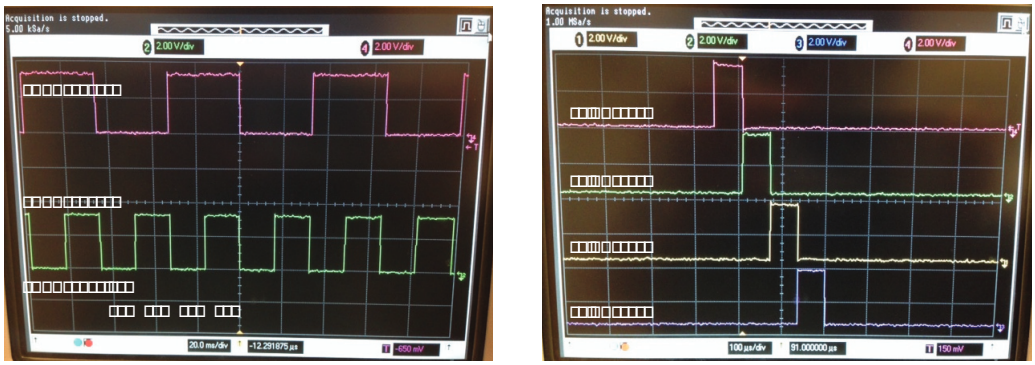
Fig. 7.26 shows the measurement results of the counter and the shift registers as part of the horizontal and vertical access circuits inside this camera chip. Fig. 7.26a presents the increment of the counter output at each clock cycle and Fig. 7.26b shows the shifting operation among the columns by use of the shift registers.

Fig. 7.27 shows the measurement results of the camera chip output at different light conditions. The figure corresponds to a time frame, where the ϕ_Y phase of the CDS operation is active,



(a) Under Dark (b) Under Light

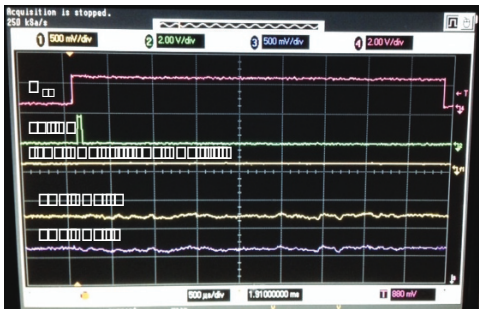
Figure 7.25: Measurement Results of the 4T APS Pixel



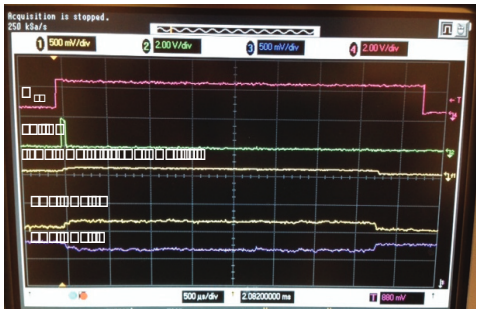
(a) Vertical Access Circuit: Counter (b) Horizontal Access Circuit: Shift Register

Figure 7.26: Measurement Results of Parts of the Access Circuits

one of the rows is selected and starting from the trigger of the shift registers, (SR_{IN}), at each clock cycle of the shift register, another column output is selected. The serialized differential output is represented by the signal named (CDS OUT+) - (CDS OUT-), which is obtained by subtracting the two outputs (CDS OUT+) and (CDS OUT-). The first measurement in Fig. 7.27a presents the serialized output of one of the rows, when the sensor is under dark. The resulting differential signal during this measurement is close to zero as shown in the figure. The second measurement 7.27b represents the serialized differential output, when the sensor is under regular office light without any lens. Since the light on the whole array is almost homogeneous during this measurement, the serialized differential output is positive but almost constant for all of the columns of the corresponding row. The third measurement 7.27c reveals the behavior of the camera chip when there is a lens on the sensor. Hence, the serialized differential output is no longer constant through the whole columns but is different from one column to another.



(a) Under Dark



(b) Under Homogeneous Light

(c) Under Light with Objective

Figure 7.27: Single Row Output Result

7.7 Image Collection

7.7.1 Image Collection Hardware

Fig. 7.28 illustrates the image collection board and the communication between different components on the board. The microcontroller (MCU), i.e.,PIC24FJ128GA106 from Microchip, builds the core of this board, together with the camera chip. The MCU receives an external clock from a 20MHz crystal oscillator and generates internal clocks for the USB and the output compare modules with its internal Phase Locked Loop (PLL) circuits. It provides reprogrammable non overlapping clocks to the camera chip through its output compare PWM channels, whose frequency can be varied according to the required exposure rate. The board includes a 10-bit DAC to generate variable DC voltages for the camera chip such as the drain voltage of the reset transistor (V_{SET}). The MCU controls the DAC block through its Serial Programmable Interface (SPI) and the DAC provides a V_{SET} voltage according to the program running on the MCU. The board also includes a 12-bit, 8 channel serial Successive Approximation Register (SAR) based ADC, which is used to digitize the differential analog output of the camera chip. In order to do that, the MCU controls the ADC block again through one of its SPIs. With a proper program running on the MCU, the MCU selects the corresponding channels of the ADC and initiates/ stops the conversion according to the timing of the camera chip. Thus, the ADC runs for each column and is triggered by the rising edge of the shift register clock. Since this camera chip does not target high speed rate operations, this offchip ADC is also selected for medium operation speed ranges. Thus, the maximum conversion rate of this ADC is 200kHz. Since the ADC works in serial mode, it requires 16-Clocks per conversion, which means the ADC requires 80µs per conversion. Thus, the minimum clock rate for the shift registers within the horizontal access circuits should be 160µs. Thus, the read-out of a single row would require the read-out of 60 columns within this time frame, which requires 9.6ms in total. Considering the read-out of 64 rows, the total time that is require to collect one frame would be 0.6s. Hence, the shortest exposure rate of the camera chip, which is reached when the ADC is working in its fastest mode, would become 16µs.

This MCU also allows to create a communication protocol by using Universal Serial Bus (USB) interface between the PC and the device. A standard USB cable provides the connection between the PC and the device. The cable has four wires: power, ground, D+ and D- and the signal wires D+ and D- operate in differential mode. There are two type of USB connectors: type A connectors, which are used in the host devices and supplies power and type B connectors, which are used on the target devices and receives power. Similarly, in our configuration, the USB connector on the PC is a standard type A USB connector, while the USB connector on the PCB is a type B micro-USB connector. Thus, the PC provides power to the image acquisition board through the USB cable. In addition, with the use of a micro-USB on the image acquisition board, the large size of the standard USB connector could be avoided.

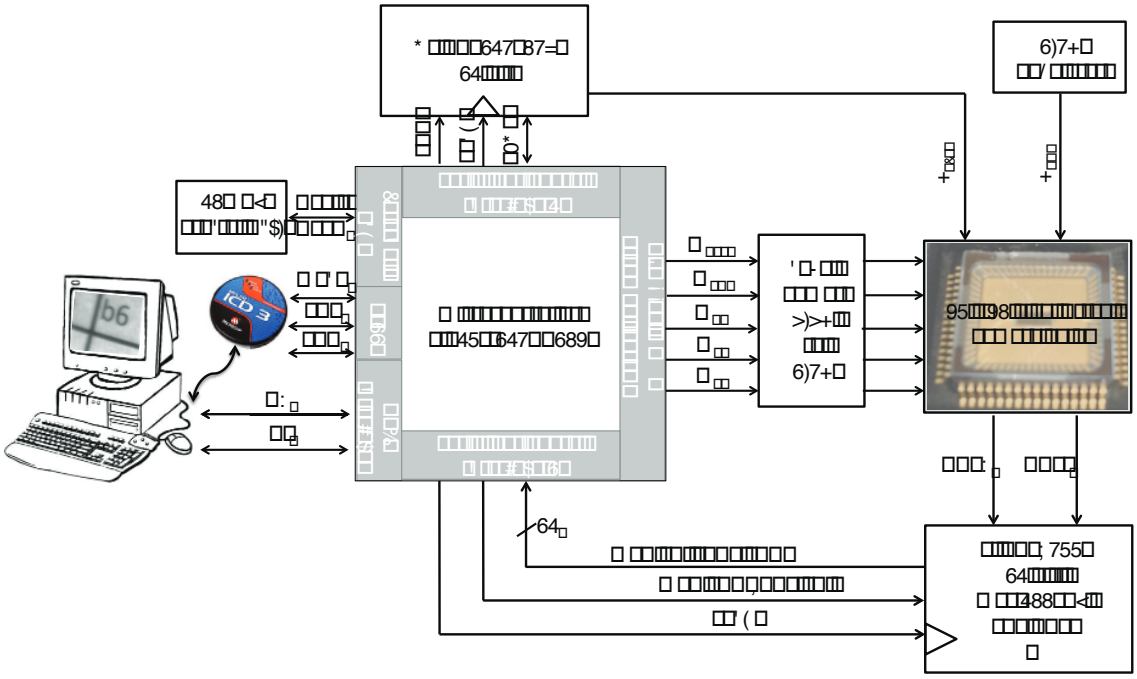


Figure 7.28: Illustration of the Image Collection Hardware Setup

7.7.2 Image Collection Software

Fig. 7.29 summarizes the software interface for collecting the images on the computer. For a succesful image acquisition from the camera board to the PC, I applied the following steps:
- Writing a MCU software to communicate with the PC
- Embedding the software to the MCU
- Writing a PC application software in C++, which runs on Windows based operating systems and uses WinUSB device functions [Microsoft, 2014] to communicate with the camera board and to collect data
- Connecting the camera board and the PCB through the USB cable
- Installing necessary drivers on the PC, in order to have the computer recognize the camera board when they are connected to each other
- Running the written PC application to collect the data of the USB differential signals in a proper order to create a frame

7.7.3 Collected Images

After applying the steps that are mentioned above, I collected images of test patterns that are printed on a A4 paper. There are many test patterns available online that can be used to quantify the image quality. These test patterns are very useful since they can take the subjectivity out of the equation and provide a quantitative result of the quality of the camera

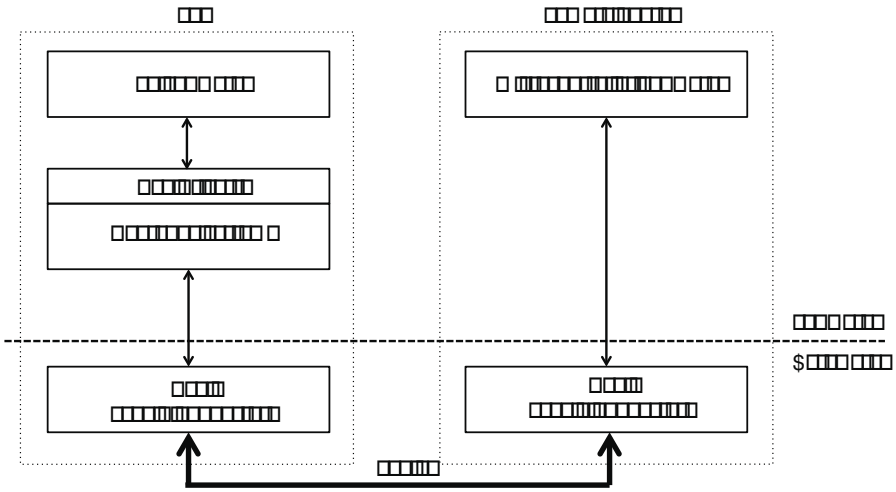


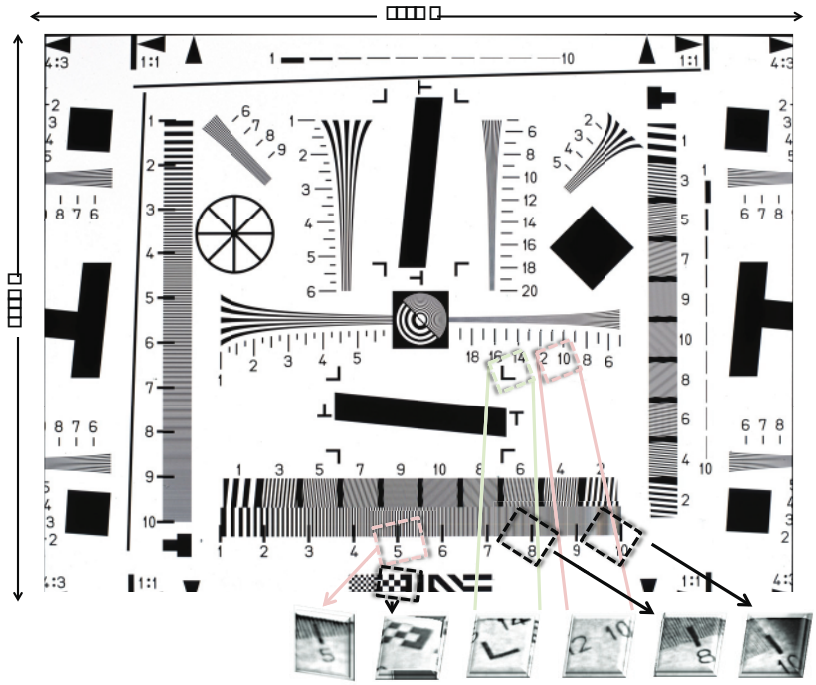
Figure 7.29: Illustration of the Image Collection Software Setup

instead of simply saying that the camera has good quality. It is commonly preferred to use high quality prints of these test patterns and expose them to a strong light from their front surface. However, in this setup, I was obliged to light the test pattern from its back side, which resulted to have background pattern on the collected images. Fig. 7.30 presents the collected images from this camera chip and the test patterns that are used. As already mentioned, the pattern at the background is due to the white paper's inner material, which becomes more visible when the paper is lightened from the back side. Despite these patterns that appear on the collected images, as shown in Fig. 7.30a, the camera chip was capable of differentiating even the closest lines from each other, which is marked with 10 on the pattern. Since the lens that is used is not optimized for such a small array camera chip, it causes the images to appear zoomed in. That is why, I could only image small parts of the test patterns at each image. Fig. 7.30b represents collected images of another test pattern, which is nine times smaller than the previous test pattern. From the images of these test pattern as well, it is seen that the camera could image even the finest details, which are smaller than half mm.

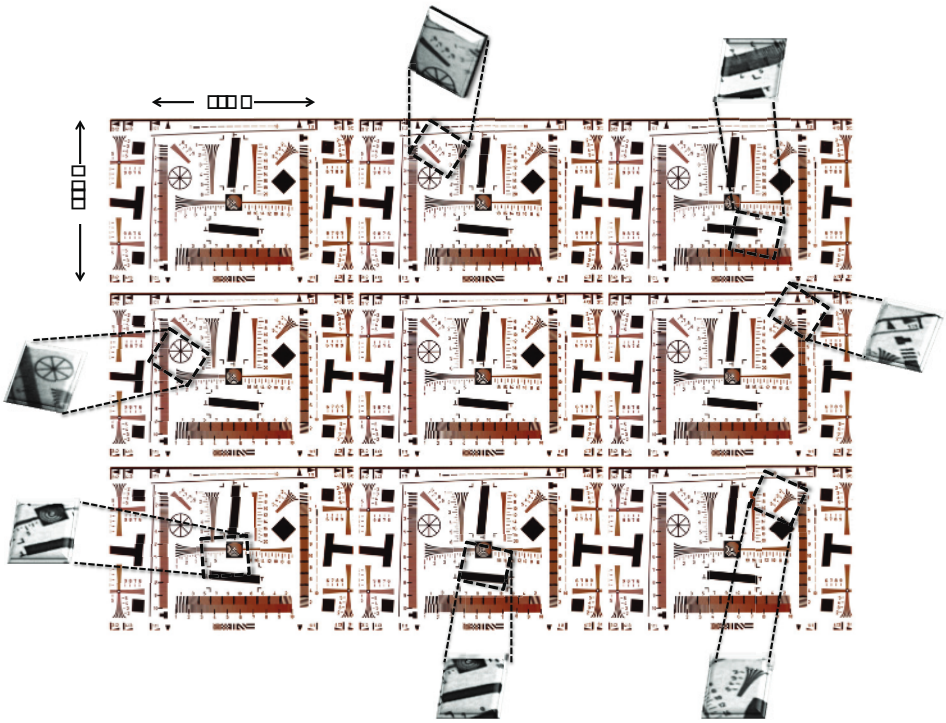
DSNU i.e., dark FPN, and temporal noise are some important parameters that should be analyzed from the collected images as well. To do that, first of all, I collected multiple frames (100 frame) under dark conditions. By applying the Eq. 7.12, I obtained the temporal noise of the camera as minimum 1.11 Digital Numbers (DN) and maximum 15.1146 DN.

$$\text{TemporalNoise(rms)} = \left(\frac{1}{M-1} \cdot \sum_{j}^{M} (S_{i,j} - \overline{S_i})^2 \right)^{1/2} \tag{7.12}$$

where $S_{i,j}$ is the i^{th} pixel value (in DN) of the j^{th} frame, $\overline{S_i}$ is the average of the all collected 100 frames, and M is the number of frames, which is 100 in this case.



(a) Test Pattern 1



(b) Test Pattern 2

Figure 7.30: Collected Images of Different Parts of Test Patterns

There are three types of DSNU: pixel FPN, column FPN, and row FPN. Since this design includes column parallel CDS circuits, it is expected to see highest FPN within pixels in the same row and lowest FPN within pixels in the same column. In order not to take into account the temporal noise when calculating the FPN, the average frame should be used for these calculations. Fig. 7.31 presents the DSNU reduction by subtracting the Master Dark Frame (MDF), i.e., average dark frame, from one of the collected images. Thus, the obtained image only includes the remaining temporal noise under dark. In order to increase the visibility of the FPN and the reduction process, I have enhanced the contrast of these images. According to the average dark frame, the pixel FPN is found as 0.93%, the minimum and maximum column FPN are 0.55% and 0.89% respectively, and the minimum and maximum row FPN are 0.72% and 1.11%. As expected, the highest FPN has been reached in row level due to the mismatches among the column parallel CDS amplifiers. After MDF subtraction, as presented in Fig. 7.31, the resulting pixel FPN has become 0.14%. The input referred noise can also be calculated by using the read noise and the conversion gain of the sensor. Then, the resulting input referred noise is found minimum 12.68e^- and maximum 172.62e^-. This high noise is mainly due to the fact that the sensor output is not digitized on chip but is carried out analog signal and then converted to digital with an off-chip ADC.

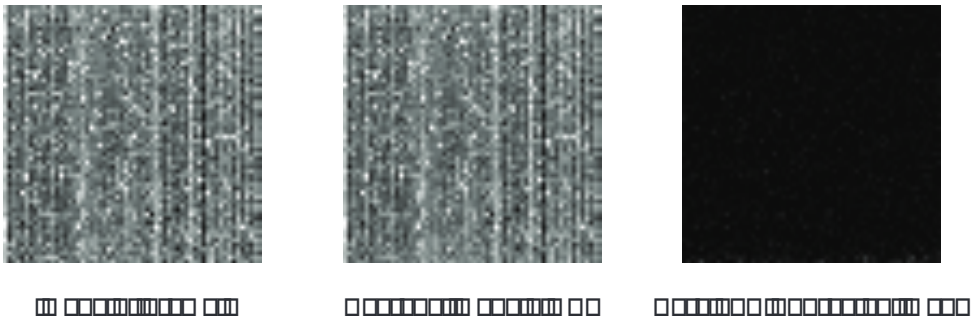


Figure 7.31: FPN Reduction by MDF Subtraction

7.8 Summary

Table 7.1 summarizes the performance parameters of this design based on simulations or collected images.

Table 7.1: Summary of the Prototype Camera Chip Performance

Technology	UMC 0.18μm Standard CMOS
Pixel Size (μm × μm)	9.14 × 14.63
Fill Factor (%)	62
Array Size	64 × 60
Noise Reduction Method	CDS
Output Mode	Serialized Analog
Read-out Mode	Rolling Shutter
Conversion Gain	85.43μV/e^-
Full Well Capacity	11542e^- - 17212$^-$
Chip Area	3240μm × 1525μm
DC Power Consumption	37.512mW
Read Noise Min - Max	1.11 – 15.11(DN)
Input Referred Noise Min - Max	12.68 – 172.62(e^-)
Pixel FPN	0.93%
Column FPN Min - Max	0.55% - 0.89%
Row FPN Min - Max	0.72% - 1.11%

7.9 Conclusion and Novelty

In this chapter, I introduced the details of my first camera chip. I explained the details of a partially pinned photodiode implementation in 4T APS design with standard CMOS technology. I also presented a novel fully differential CDS circuit, which is used in the column parallel noise reduction circuits of this design. With the simulations and measurements above, I showed the behavior of each block separately and together with the other blocks. In addition, with the noise analysis of different circuits, I showed the importance of the effective use of CDS architectures. By implementing the design in standard CMOS technology, I could immensely reduce the fabrication cost of this chip compared to CIS dedicated technologies. This design is a complete camera chip, providing differential serialized analog output. Within this chapter, I also presented the chip output results at different light conditions and showed the collected images from the camera chip in order to quantify the quality of the camera. In the next chapter, I will present our final camera chip, which is a VGA camera chip that delivers two parallel digital outputs.

8 Chip 3: A VGA 4T APS Camera Chip

Since the camera prototype that I have explained in the previous chapter has a very small array size, a larger array format camera chip would be required in order to achieve smoother images in real biomedical samples. This part of the thesis explains how I improve the previous camera chip design by with this novel reprogrammable VGA camera chip integrated with chip level ADC. This chip is our second complete pixel array sensor and third taped-out chip. The design occupies an area of 5mm × 5mm and it is also fabricated in UMC 0.18µm standard CMOS process like the other chips. This camera chip is similar to the previous prototype camera chip except that it uses a mixed-signal design approach, shares the pixel circuit among four pixels and allows 2 channel 8-bit serialized digital output. It also provides a novel programmable interface to adjust the array size with respect to the pixel size depending on the application.

Fig. 8.1 shows the top level schematic of our VGA camera chip. The chip includes a VGA (640 × 480) format 4T APS pixel array that has a total area of $4350 \times 3435 \mu m^2$. Similar to the first array camera chip, the design includes column level current mirrors, CDS circuits and horizontal access circuits at the top and bottom of the pixel array and a vertical access circuit. The pixel implementation in this camera chip benefits from pixel sharing technique. In addition, this design consists of two parallel 8-bit Successive Approximation Register (SAR) type ADCs at the top and bottom of the pixel array. Furthermore, the design gives the flexibility to choose analog or digital outputs by use of transmission gates controlled by OUTPUT SEL signal. If the OUTPUT SEL signal is high, the analog readout operation is selected and two parallel differential outputs are provided, conversely if the OUTPUT SEL signal is low, digital readout operation is selected and two parallel digital outputs are provided.

Moreover, I used a mixed-signal design approach when implementing this VGA camera chip. I designed the vertical and horizontal access circuits in semi-custom by using Cadence Design Compiler and Encounter programs. I designed the rest of the chip in full-custom. In order to reach a compact layout, I stacked three CDS blocks at the top and the bottom of the pixel array. With this implementation, I matched the CDS blocks and the pixel array's horizontal dimensions. The 8.2 shows the layout of this camera chip.

In the following sections, in order to avoid repetition, I will only introduce the blocks that are different with respect to the previous camera chip, i.e., the pixel circuit and the SAR ADC.

8.1 Top Level Design

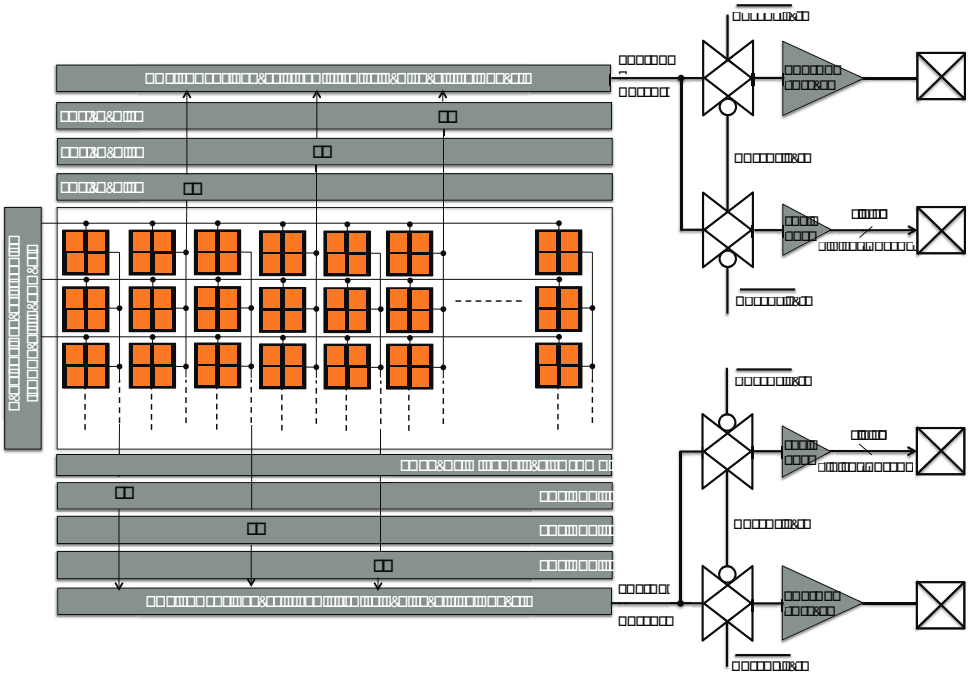


Figure 8.1: Top Level Schematic of the VGA Camera Chip

8.2 Pixel Design and Pixel Sharing Technique

8.2.1 Programmable Pixel Design and Pixel Sharing Technique

In order to implement a VGA sensor with small silicon area, i.e., low cost, in this design, one pixel circuit that consists of M_{RS}, M_{SF}, and M_{SEL} transistors is shared by four pixels, where each photodiode has its own M_{TG} transistor. Thus, in this design there is 1.75 transistor per pixel instead of 4 transistors as opposed to the traditional implementation of the 4T APS CMOS image sensors and to our first array camera chip.

In the literature, we can find different ways of implementing pixel sharing technique. The most common implementation is having a unique photo-diode and M_{TG} for each pixel and connecting all the FD nodes to the common pixel circuit. With this method, each pixel has only 1.75 transistor per pixel instead of 4 transistor. However, this method requires four different control lines for four M_{TG} transistors, which reduces the fill-factor of the design by requiring extra connections and wires. Thus, in our VGA camera chip, we used a pixel sharing technique that is different than the traditional implementation. Our approach also reaches 1.75 transistor

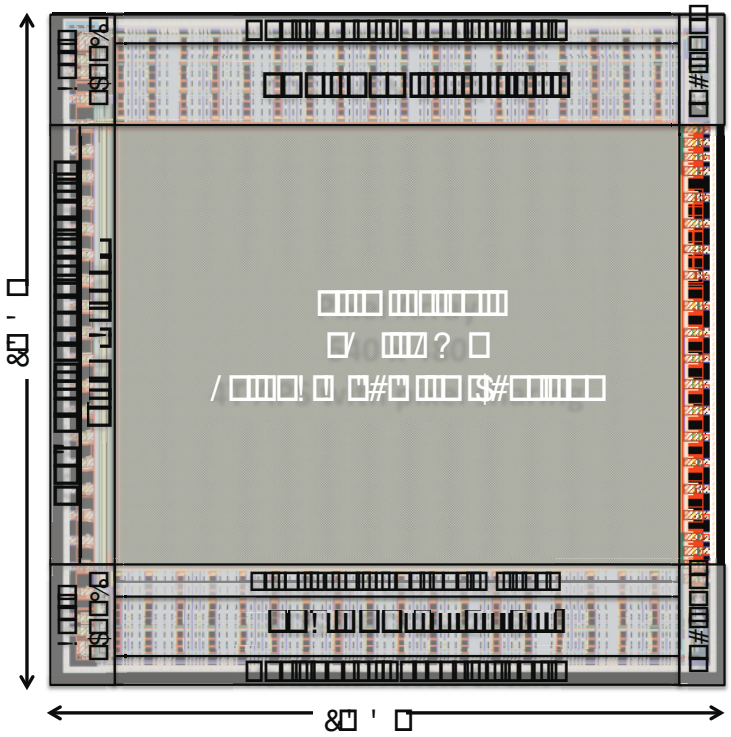


Figure 8.2: Top Level Layout of the VGA Camera Chip

per pixel similar to the traditional implementation but instead of requiring 4 control lines for each gate of the M_{TG} transistors, it only requires two control lines per row [Mori et al., 2004]. To do that, each group of four pixels is either controlled by Φ_{TG_0} and Φ_{TG_1} or Φ_{TG_2} and Φ_{TG_3}. Thus, in one group of four pixels, only the two of the photodiodes are connected to the pixel circuit and the other two photodiodes use the pixel circuit of the next group of pixels. With this implementation, I make sure that only one pixel is selected at a time, yet I have only two control signals per pixel. Thus, I reach a higher fill-factor than the traditional pixel sharing implementations. The fill factor of this design is %79, where it was %62 for our first array camera chip.

The schematic and the layout of this pixel is shown in Fig. 8.3 and Fig. 8.4 respectively. The total size of one group of four pixels is 12.64µm × 12.64µm while the size of each photo-diode is 5.6µm × 5.6µm .

In Chapter 3, we have defined spatial resolution and the relation between the diffraction limit and the pixel pitch. In Table 3.1, we summarize the relation between the pixel pitch and the diffraction limit for different objectives and NAs. According to this table, the smallest pixel pitch is required (3.35µm) only when lowest magnification objectives (2X or 4X) are used. As opposed, for higher magnification objectives, pixel pitches above 6.71µm would even be enough to reach the diffraction limit. For low light imaging applications, low magnification objectives should not be preferred, since they reach lower photon collection efficiency than

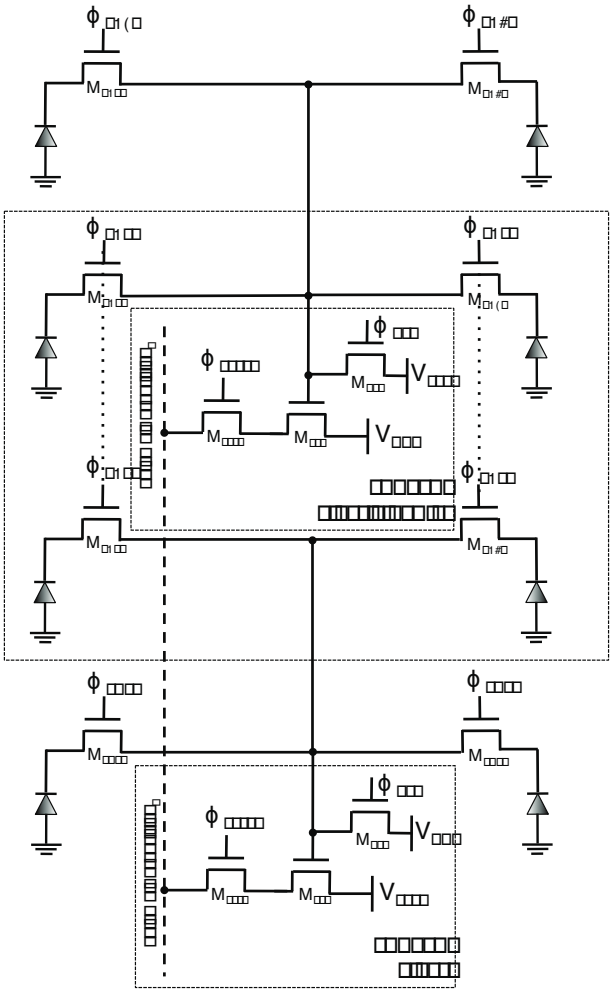


Figure 8.3: Pixel Schematic of the VGA Camera Chip

the higher magnification objectives as shown in the table. Moreover, the spatial resolution that can be reached with low magnification objectives (2X or 4X) is only 3.35μm, while imaging cell details would require much lower resolution than this. Thus, for low light biomedical imaging applications, 20X and higher magnification objectives should be chosen. This makes us to conclude that if we have the flexibility to change the pixel pitch of a design, we may reach better collection efficiency by using larger pixels when higher magnification objectives are used. Hence, our VGA camera chip gives us the flexibility to program the pixel in different mode of operations and to optimize the pixel size according to the selected objective.

The method of programming the pixels for reaching different pixel pitches is illustrated in Fig. 8.5. In the standard configuration, the TG gates are controlled with four different TG pulses, i.e, Φ_{TG_0}, Φ_{TG_1}, Φ_{TG_2}, and Φ_{TG_3}. In this case, the resulting pixel pitch would be the smallest (6.32μm) and the output image format would be VGA (Fig.8.5a). If a magnification objective equal or larger than 40X is selected, then the sensor can be programmed to have larger pixels.

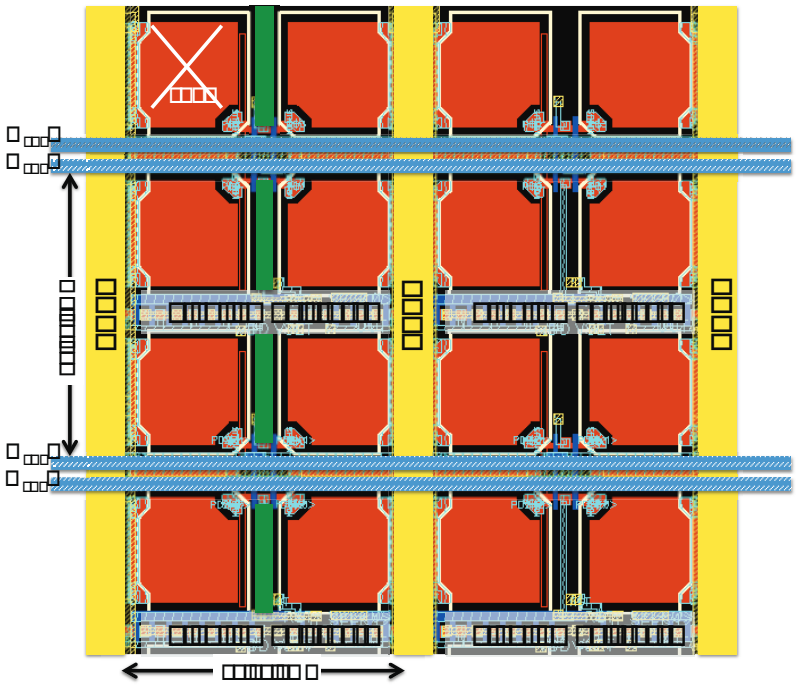


Figure 8.4: Pixel Layout of the VGA Camera Chip

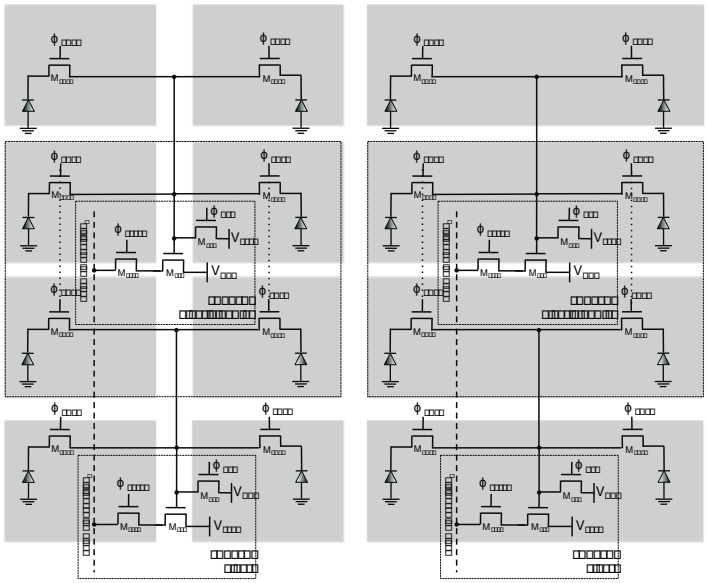
To do that, the two of the TG gates are controlled with the same control signal as in Fig.8.5b. Thus, the resulting image output would become Half VGA (HVGA) and the pixel pitch of the design becomes 6.32µm vertically and 12.64µm horizontally. The design can be programmed to obtain even larger pixels (pixel pitch of 12.64µm). In this case, all the TG gate signals should be controlled with the same control signal and the design would work as if there is no pixel sharing.

This optimization is very useful especially in very low light imaging applications. With this method, depending on the selected objective, different pixel sizes can be obtained. As a result, the collection efficiency and the total charge transferred to the FD node can be increased for the same amount of light.

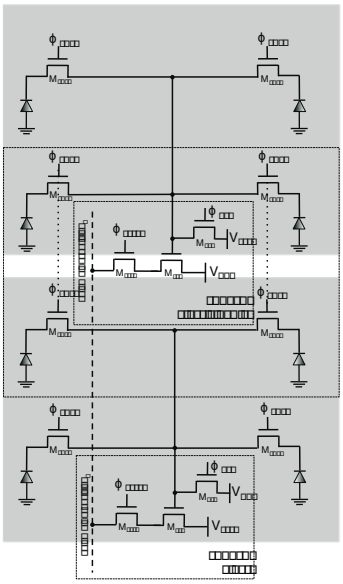
The timing diagram of the this design in standard configuration is shown in Fig. 8.6.

8.3 Capacitive SAR ADC

Analog to Digital Converters (ADCs) are devices that convert the continuous signals to digital numbers. Since the analog information of the light needs to be converted to digital signal to construct the image, they are inevitable parts of digital cameras. In the literature, it is possible to find CMOS image sensors integrated with column parallel ADCs [Zhou et al., 1997] as well as chip level single ADCs [Hamami et al., 2004]. In addition, there are many different approaches for the type of ADCs. The Successive Approximation Register (SAR) and single slope type ADCs



(a) VGA Format Image Output (b) HVGA Format Image Output



(c) QVGA Format Image Output

Figure 8.5: Three Different Programming Options of the Pixel

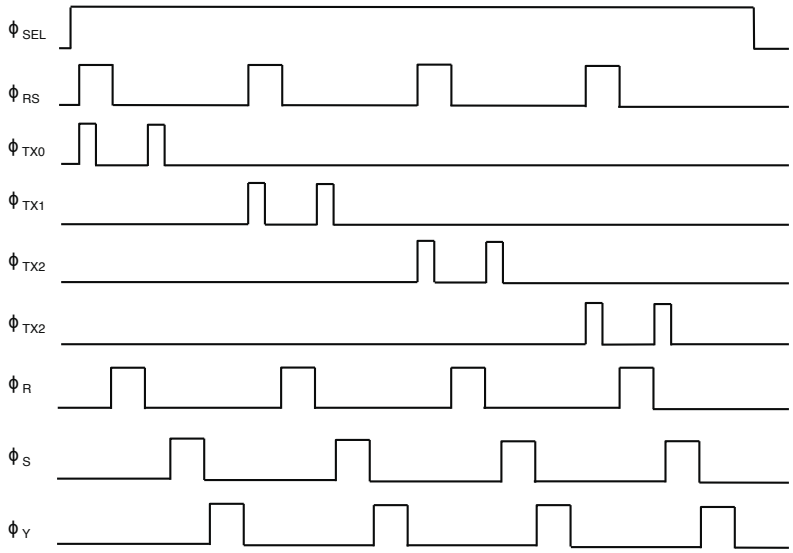


Figure 8.6: Timing Diagram of the VGA Camera Chip in Standard Configuration

are the most commonly used ADC types for CMOS image sensors since their area overhead is low and can reach high resolution with reasonable speed. As mentioned earlier, most of the biological applications have slow response time and require long exposure times. Thus, ADCs with 200kS/s to 1MS/s speed rates are enough for these types of applications. The primary concerns in biomedical applications are the resolution and the area. In order not to introduce distortion or artifacts into the image, the ADCs must have at least 8-b resolution with low Integral NonLinearity (INL) and Differential NonLinearity (DNL) [Zhou et al., 1997]. For the VGA camera chip, I have used Microelectronic Systems Laboratory (LSM) SAR ADC Intellectual Property (IP), which has 8 bit resolution and reaches maximum 2MHz conversion rate. The measurement results of this ADC IP have validated its function under 220kHz coversion rate with 7.3 Effective Number of Bit (ENOB) and INL and DNL below 0.8LSB [Majidzadeh Bafar, 2012].

Successive Approximation Register type Analog to Digital Converters (ADCs) require several comparison cycles to complete one conversion. It is based on binary search through all possible quantization levels and at each quantization level, it outputs a decision bit. The resolution of the SAR ADCs are determined according to the number of clock cycles and with a different quantization level at each clock cycle. A conventional SAR ADC is shown in Fig. 8.7 which includes a track and hold circuit, a comparator, a digital control circuit, an N-bit register and an N-bit Digital to Analog Converter (DAC) unit.

Due to the nature of this technique, its operation speed is limited but since the same blocks are used for representation of each digital bit, this type of ADCs does not require a large area when compared with pipeline ADCs or Flash ADCs. Majority of the ADCs in the market today are based on SAR ADCs since they provide medium to high resolutions (8 to 18bits) with low area and reasonable speed (up to 50 MS/s).

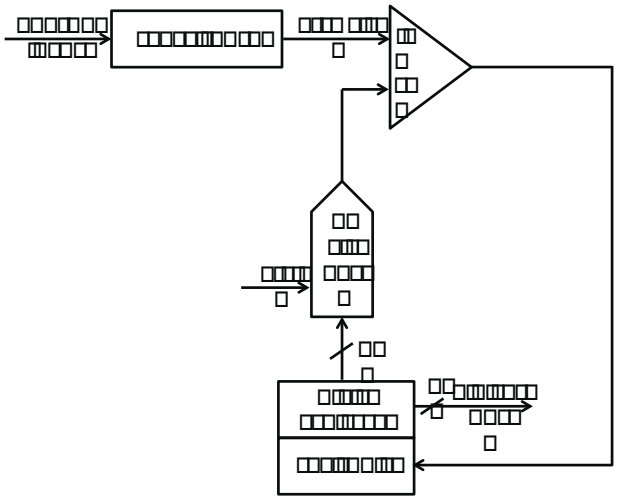


Figure 8.7: Illustration of SAR ADC

The working principle of a conventional differential capacitive 8-bit SAR based ADC that includes a capacitive DAC with an inherent track and hold is shown in Fig. 8.8. All capacitors have binary weighted values, e.g. C, 2C, 4C, 8C. The last capacitor is a dummy capacitor with the same size as the one before it. With the dummy capacitor, the total capacitance of the n+1 capacitors becomes 2 times of the MSB capacitance value. The ADC takes the differential input as it is required by the CDS stages, which provide differential outputs. The positive and negative input nodes of the comparator is connected to two different capacitive blocks controlled with switches. Each capacitor is connected to V_{CM}, V_{REF} or $V_{IN+/-}$ input signals by using the switches controlled by the SAR logic block. The conversion process is performed in three steps: the sample mode, the hold mode, and the actual conversion mode.

The process starts by the sampling of the input signals. To do that, the comparator's positive and negative inputs are both connected to virtual ground, i.e., V_{CM} node and the other nodes of the capacitors are all connected to V_{IN+} or V_{IN-} through the control switches. This behavior is shown for a 4-bit ADC in Fig. 8.9a. With this operation, a charge proportional to each capacitor and a total charge of $8 \times C_{MSB} V_{IN+}$ or $8 \times C_{MSB} V_{IN-}$ are trapped. For simplicity purposes, the V_{CM} node is considered as ground for charge calculations.

After the sampling operation, the hold operation starts at which the V_{CM} connection switch at the common node becomes OFF and the capacitors are connected to V_{CM} from their opposite side. With this operation, $-V_{IN+}$ and $-V_{IN-}$ voltages are applied on the positive and negative input terminals of the comparator. Fig. 8.9b presents the hold operation of this SAR ADC.

After showing the built-in sample and hold operation of the ADC, now we present the actual conversion operation. In the first conversion step (see Fig. 8.10), the largest capacitor of the top DAC block is connected to the reference voltage V_{REF} through the S_{3p} switch. All the other switches connect the capacitors to V_{CM} node. The bottom DAC blocks behaves the opposite way around and the largest capacitor is connected to the V_{CM} while the other capacitors are

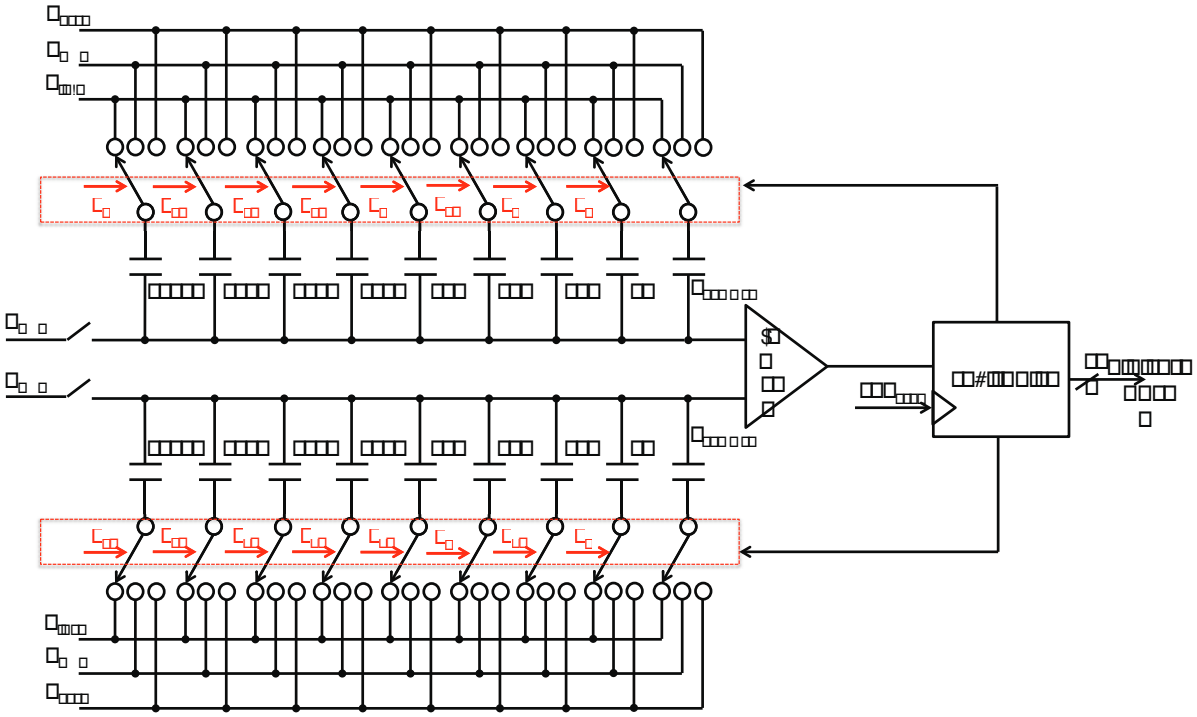


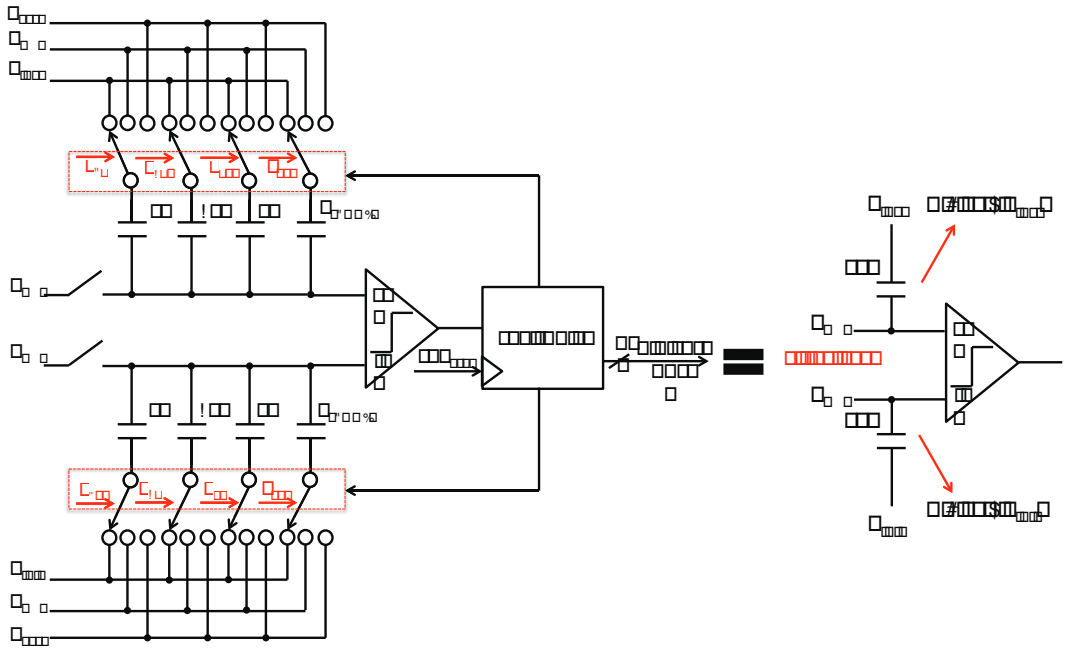
Figure 8.8: Top Level Implementation of the Capacitive SAR ADC

connected to the V_{REF} voltage through the S_{0n}, S_{1n}, and S_{2n} switches. According to the result of this conversion, SAR logic circuit decides for the next configuration and the switches of the DAC block is configured accordingly. This operation continues for 8 clock cycles where at each clock cycle one bit of the 8-bit digital output is extracted starting from the LSB. I illustrate the actual conversion operation according to the decision of each clock cycle within Fig. 8.11. After conceptually explaining the operation of capacitive SAR ADC, in the next section, I will present the simulation results.

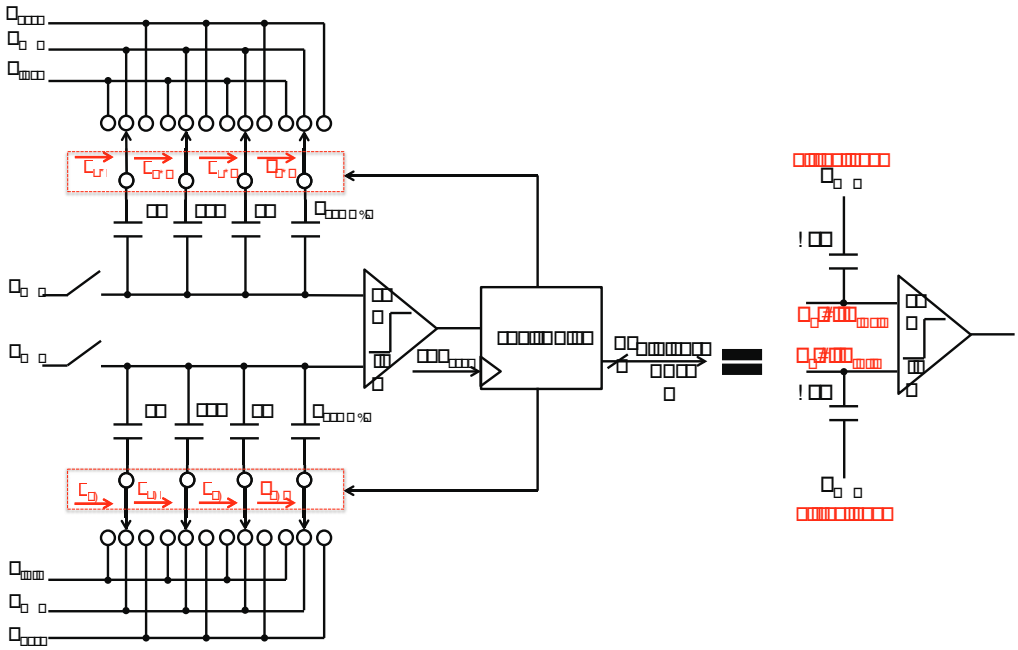
8.4 Results

8.4.1 Performance Parameters

As mentioned earlier, there is a trade-off between the conversion gain and the FWC of the sensor. Due to the increase of the FD node capacitance (5.93fF), this design results in lower conversion gain but higher FWC than the previous camera chip. The performance parameters of this design is summarized in the Table 8.1.



(a) Sample



(b) Hold

Figure 8.9: SAR ADC Sample and Hold Operation

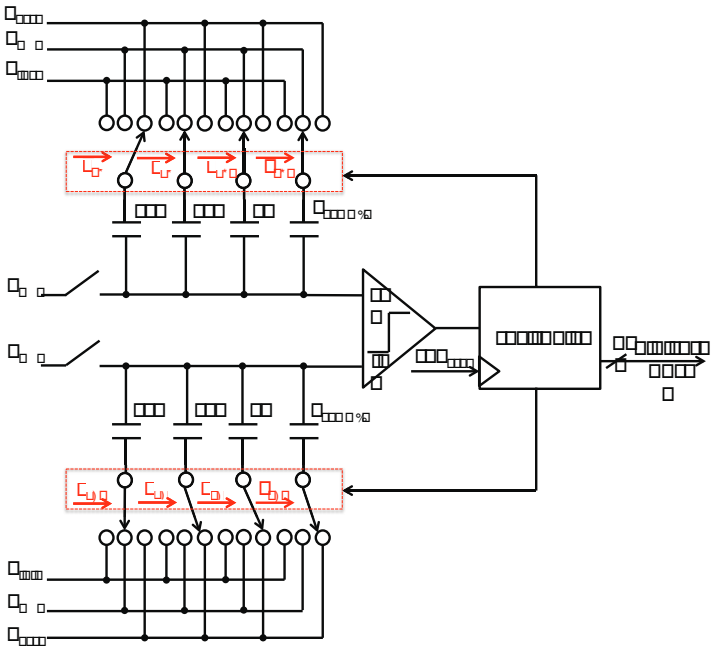


Figure 8.10: SAR ADC 1st Conversion Step

Table 8.1: Summary of the VGA Camera Chip Performance

Technology	UMC 0.18µm Standard CMOS
Pixel Size - QVGA (µm × µm)	12.64 × 12.64
Pixel Size - HVGA (µm × µm)	12.64 × 6.32
Pixel Size - VGA (µm × µm)	6.32 × 6.32
Fill Factor (%)	79
Array Size	640 × 480
Noise Reduction Method	CDS
Output Mode	Two Parallel Digital or Differential Serialized Analog
Read-out Mode	Rolling Shutter
FD node capacitance	5.93fF
Conversion Gain	27µV/e^-
Full Well Capacity	66629e^-
Chip Area	5mm × 5mm
DC Power Consumption	

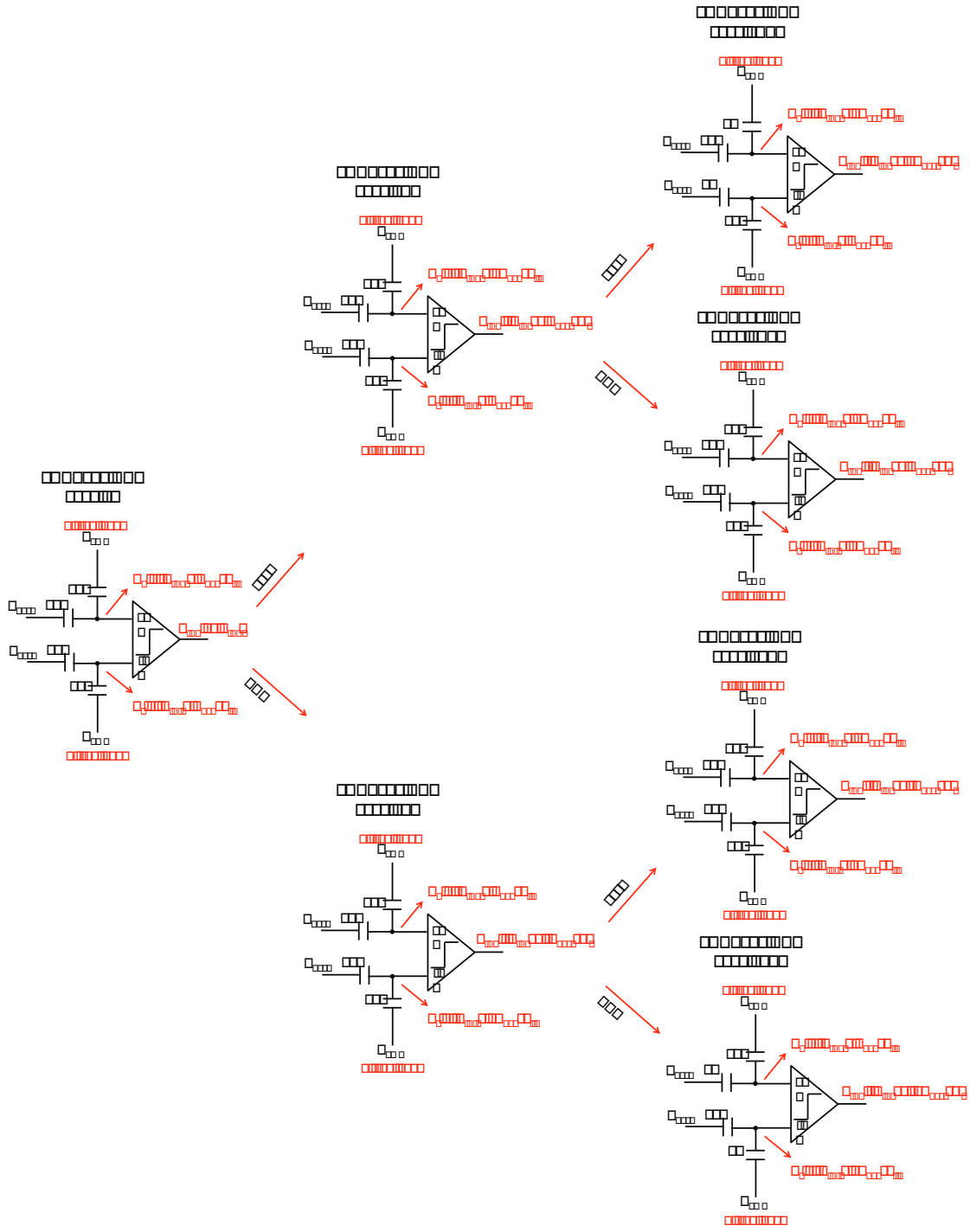


Figure 8.11: Summary of Conversion Steps in SAR ADC According to the Decision of Each Clk Cycle

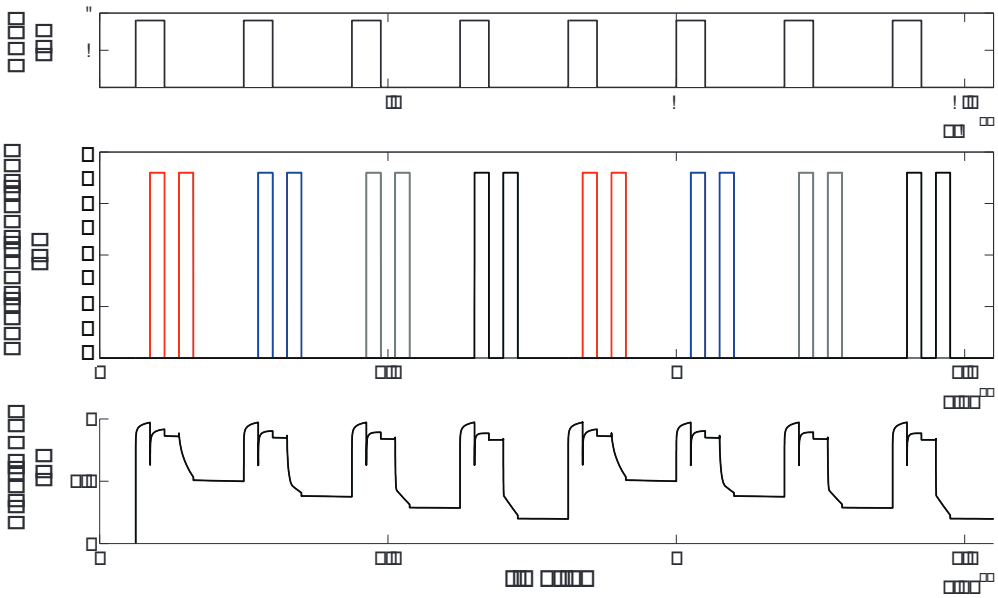


Figure 8.12: Transient Simulation of the VGA Camera Pixel

8.4.2 Pixel Simulation

In Fig. 8.12, I present the transient simulation result of one pixel group that consists of four pixels sharing the same pixel circuit. For this simulation, I provided different photo current for each photodiode. Thus, at the end of each ϕ_{TG} clock cycle, the pixel output voltage reaches a different value. According to this result, the voltage drop after reset operation at the pixel outputs are 0.36V, 0.49V, 0.58V, and 0.67V for photocurrents (I_{ph}) of 5nA, 10nA, 15nA, and 20nA with integration time of 2µs.

8.4.3 ADC Simulation

The ADC simulation in Fig. 8.13 confirms the functionality of this ADC IP, when the ADC conversion rate is at 55kHz with an ADC clock period of 2µs.

8.4.4 Top Level Simulation

The top level simulations confirm the functionality of this chip when the analog output operation is selected through the SEL OUT TYPE switch. As mentioned earlier, this switch is used as a control switch for the transmission gates in order to select analog or digital output option of the chip. Moreover, similar to the previous design, the outputs are serialized by use of the shift registers at the horizontal access circuits at the top and bottom of the pixel array, which are triggered with the SR IN signals as shown in the figures. Finally, the TOP (OUT+ - OUT-) and BOTTOM (OUT+ - OUT-) signals represent the serialized analog outputs as in two

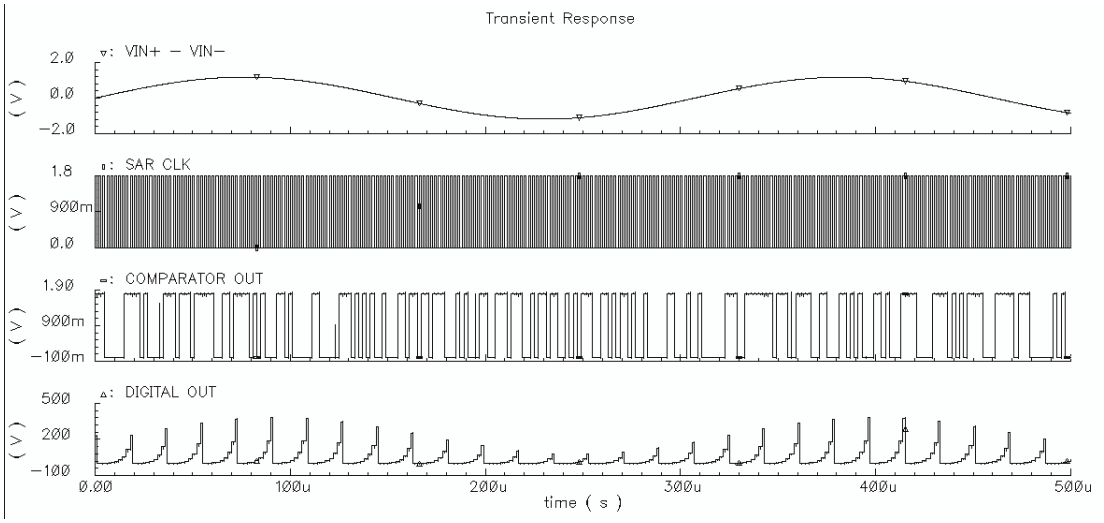


Figure 8.13: Transient Simulation of the Capacitive SAR ADC

parallel forms.

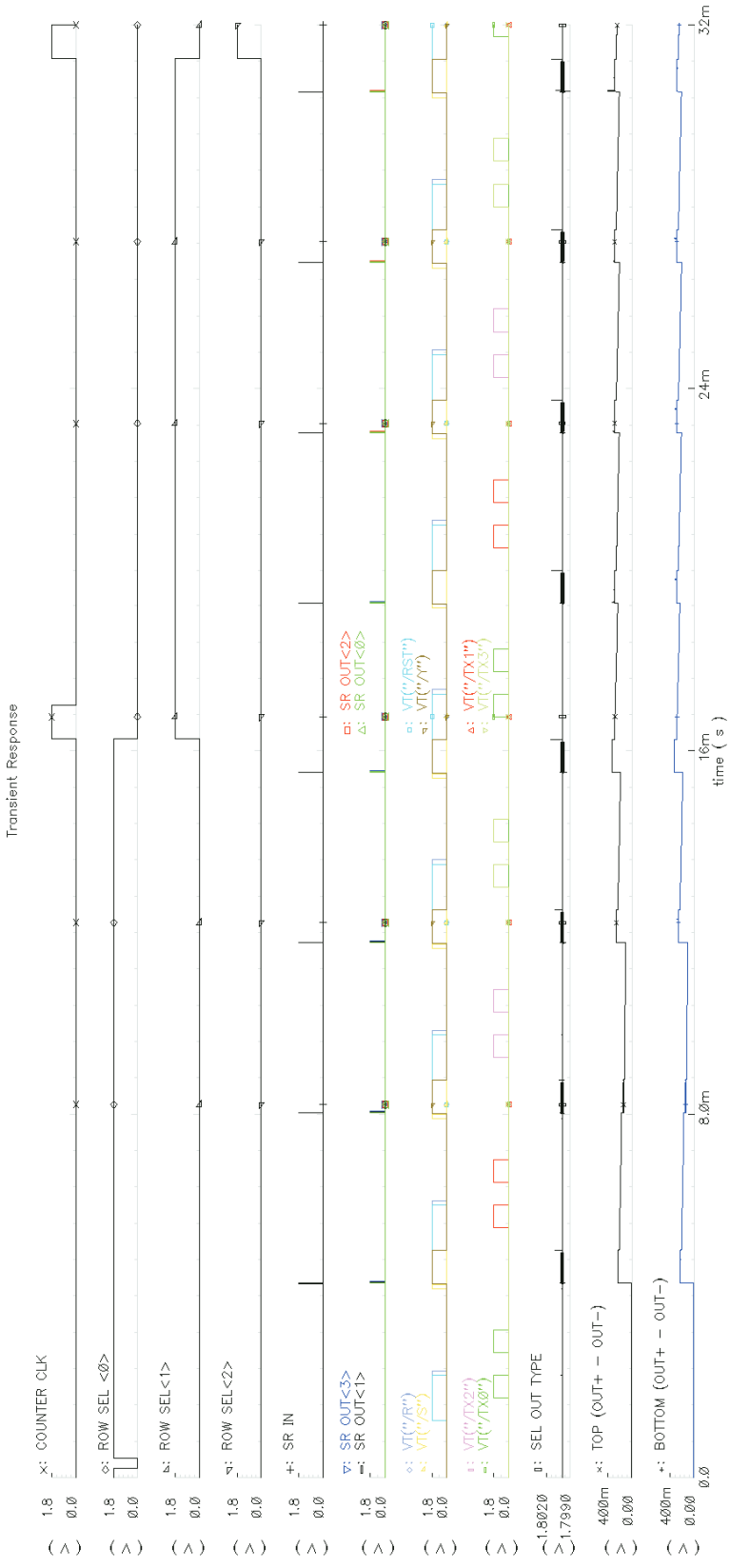


Figure 8.14: Top Level Simulation of the 3rd Camera Chip

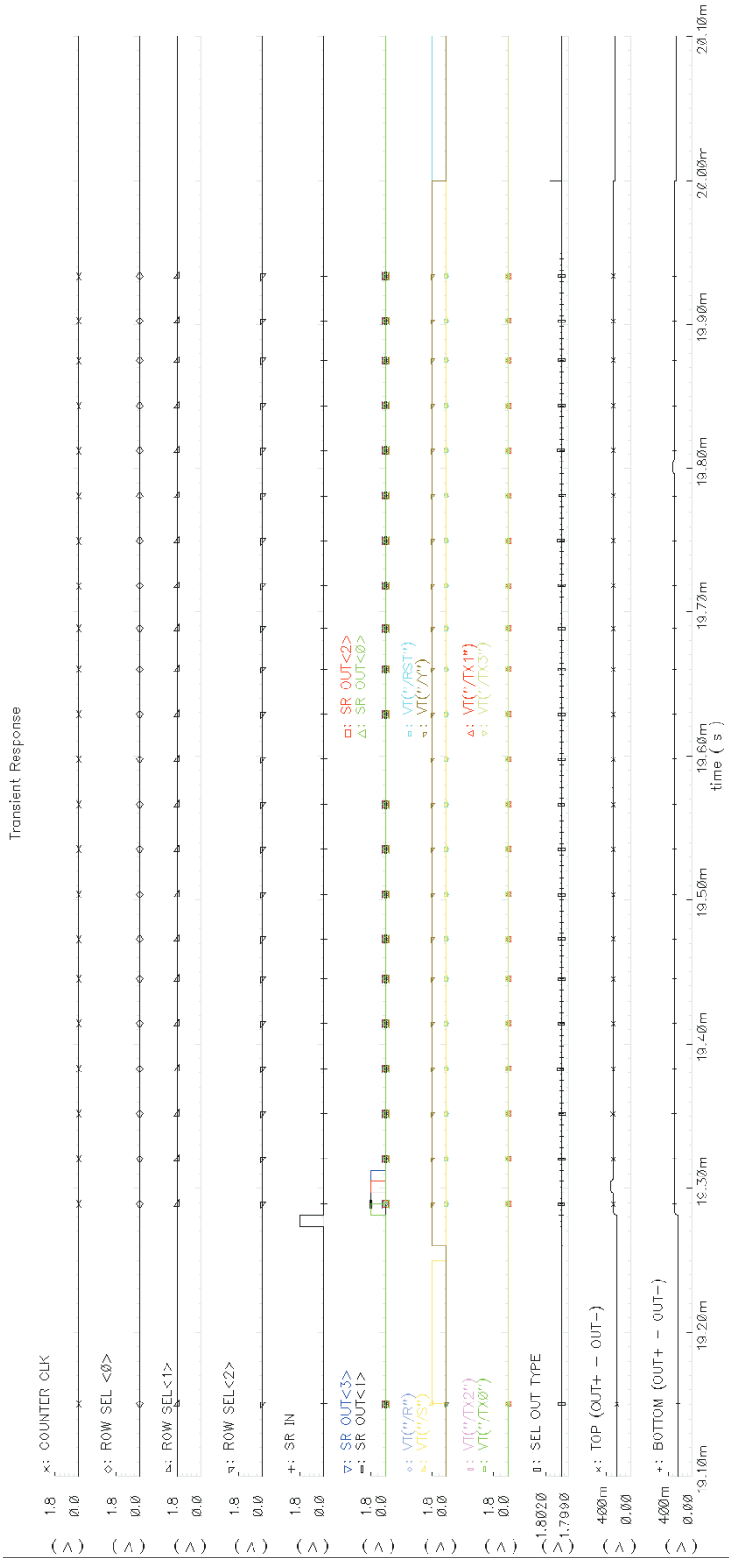


Figure 8.15: Top Level Simulation of the 3rd Camera Chip with More Details

8.4.5 Comparison

Table presents a comparison of our small camera prototype, reprogrammable VGA camera chip and similar format CMOS image sensors from the literature and market. According to this table, our reprogrammable VGA camera, CHIP v3, provides highest fill-factor and full-well capacity. In addition, the small camera prototype, CHIP v2, presents comparable DR performance with a very popular sensor from the market [Aptina, 2014c], which is also the one that used in Chapter 4. Moreover, the area that our CHIP v3 occupies is much smaller than the sensors in this table, which provide similar sensor outputs (640x480). Most importantly, none of these sensors are re-programmable as our CHIP v2.

Table 8.2: Results Comparison Table

	CHIP v2	CHIP v3	MT9V032 [Aptina, 2014c]	OV9620 [OVT, 2002]	YONEMOTO [Yonemoto et al., 2000]	YANG [Yang et al., 1999]
Sensor Array (HxV)	64x60	640x480 320x240 160x120	752x480	640x480	640x480	640x512
Pixel Pitch (µm × µm)	9.14x14.63	12.64x12.64 6.32x12.64 6.32x6.32	6x6	5.2x5.2	7.4x7.4	10.5x10.5
Chip Area (mm × mm)	3.24x1.5	5x5	4.51x2.33 (imaging area)	6.66x5.32	5.84x5.01	6.7x5.3
Fill Factor (%)	62	79	NA	NA	NA	29
QE(max)(%)	55.3	NA	49	NA	NA	NA
$N_sat(e^-)$	17212	66629	NA	NA	NA	NA
NF(e^-)	12.68	NA	NA	NA	NA	NA
DR(dB)	62.6	NA	62.9	60	53	NA
DN(bits)	12 (off-chip)	8 (on-chip)	10	10	NA	12

8.5 Conclusion and Novelty

In this chapter, I explained the design details of the VGA camera chip, which uses pixel sharing technique that reaches 1.75 transistor per pixel instead of 4 transistor as in traditional implementations and different from the traditional implementations, requires only two TG control lines per pixel instead of 4. Within this chapter, I also presented a novel approach that gives the design a flexibility in changing the array resolution with respect to the pixel size. With this novel method, the photon collection of the sensor could be increased and optimized according to the application. Due to the larger FD node capacitance, this design suffers from reduced conversion gain but reaches almost four times higher N_{sat} than the previous camera chip. Moreover, with the pixel sharing technique, this design results in 13% higher fill factor than the previous camera chip.

9 Proposed Novel DPS Designs for Biomedical Applications

The DPS designs reduce the analog design limitations and benefit from technology scaling more efficiently than APS designs. These advantages can be very useful for portable low-cost devices since they lead to further reduction in the power consumption and the cost of the chip by reducing the total chip area. Especially the DPS designs that integrate change detection feature may serve well in biomedical applications where the target molecules have very slow response time. With this feature, an automatic generation of images when only there is change in the target molecule can be done. This would eliminate the requirement for the scientists to examine the samples for full time in front of the microscope. Thus, within the frame of this thesis, I propose novel DPS designs for biomedical applications.

9.1 An Event-Detection Pixel Sensor with Single Output for Each Pixel

In Fig. 5.6, I have shown a DPS design, which provides high speed readout operaiton. The first concern of this design is of course the low-fill factor mainly due to the 8-bit pixel level memory. The use of pixel level memory is of great importance when the target is high speed imaging applications. However, for biomedical applications, since the target is low read-out speed with high quality, it is important to improve the fill-factor rather than increasing the speed. Thus, in order to improve the fill-factor, my first attempt has been to replace the pixel level 8-bit memory with a 1-bit memory [Köklü et al., 2013c]. In this design, since 1-bit memory is not used to register the value of the pixel but it is used to check if there is an event in the pixel, the pixel size does not depend on the digital resolution in as in Fig. 5.6. I proposed pixel circuit is presented in Fig. 9.1 and the top-level schematic is shown in Fig. 9.2, which replaces the N-bit pixel level memory with a single bit memory to store the previous state of the pixel.

This design includes a pixel level event generation mechanism. A ramp voltage generated by a 10-bit counter and a Digital to Analog Converter (DAC) is compared with the pixel integrated voltage at each clock cycle at the same time allowing a fixed exposure time interval. The timing diagram of this design is shown in Fig. 9.3. Each column includes 120 pixels, a priority encoder,

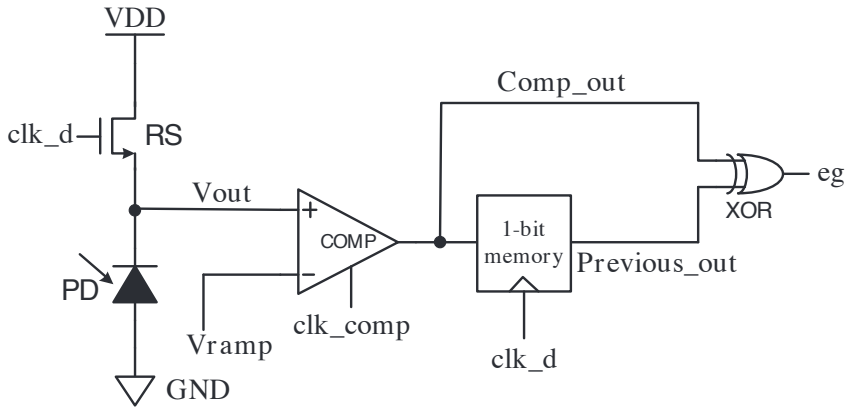


Figure 9.1: Event-Detection Pixel [Köklü et al., 2013c]

a decrement counter and a DAC Digital to Analog Converter. The pixel architecture includes a photodiode, a reset transistor (RS), a latched-comparator and a novel photo voltage change monitoring system by means of a 1 bit register and an XOR gate as seen in Fig. 9.1. A ramp voltage is generated by a 10-bit decrement counter and a DAC for each column independently. The design can also be realized by a common counter and DAC block for all columns instead of per column counter-DAC blocks.

The technique is based on binary search where the digital control logic (counter) decrements bits at each clock cycle. After each decrement, the input voltage of the pixels (which is the integrated pixel voltage in this case) is compared with the reference voltage generated by the Counter-DAC block. When the input voltage is higher than the generated ramp voltage, the event detector in the pixel is triggered to 1 by means of a comparator, 1-bit register and XOR gate and the event generation (eg) signal becomes 1. In the next clock cycles, the pixel output (eg) will return to 0 since the value in the pixel will always stay higher than the ramp voltage after the first event generation. The timing diagram showing this event-generation mechanism is represented in Fig.9.3.

The working principle of each independent column in case of single (Fig. 9.4a) and multiple (Fig. 9.4b) event conditions is explained in more detail in Fig. 9.4.

The single event case is trivial, where pointer 1 represents the generated event from one of the pixels in a column, pointer 2 represents the counter value at the time of the event or the value of the pixel with the event and the arrow 3 points the priority encoder output that represents the address of the active pixel.

For cases where multiple pixels are active at the same time, the priority encoder implementation is used to give priority in a column to one pixel at a time. In this case, first, the location of the pixel with highest priority is registered and all the other active pixels are queued until they receive the priority. The priority can be shifted from the least significant to most significant pixel or vice versa or other orders can be used. In this design, I implemented the priority shift-

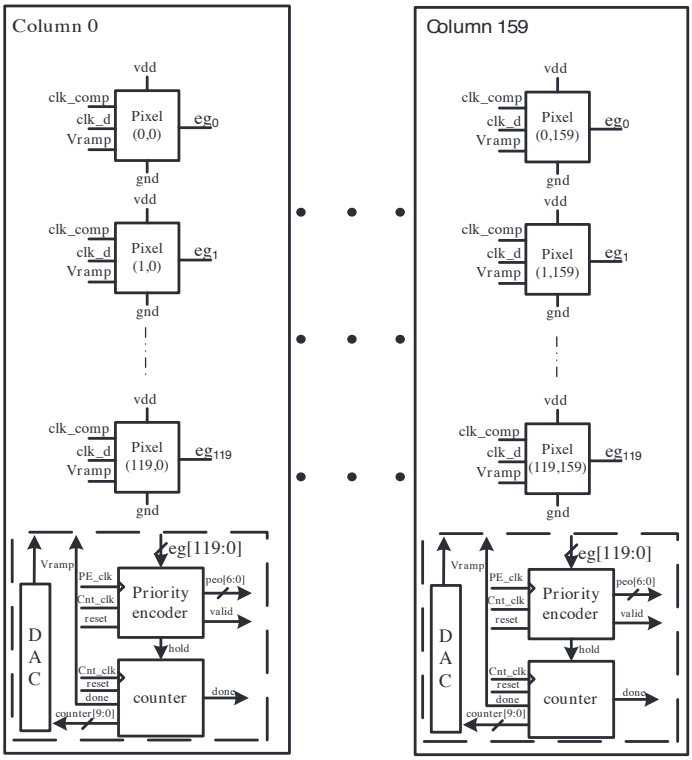


Figure 9.2: Event-Detection Top Level Schematic [Köklü et al., 2013c]

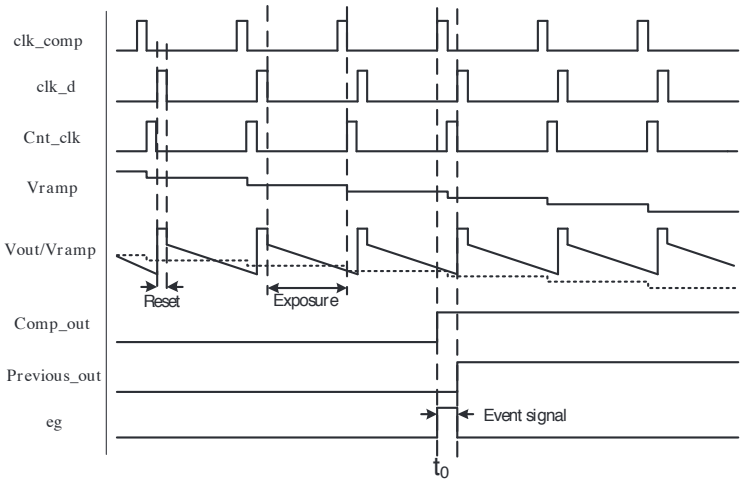


Figure 9.3: Timing Diagram of a Single Pixel [Köklü et al., 2013c]

ing from the least to the most significant pixel. As explained earlier, during priority shifting, the counter is in Hold mode as shown by pointer 2 and the ramp voltage value is no longer changed until the priority shifts to the lowest priority pixel. It is also seen that during the Hold mode, even if the counter's clock has risen (pointer 4), until the next clock cycle of the counter

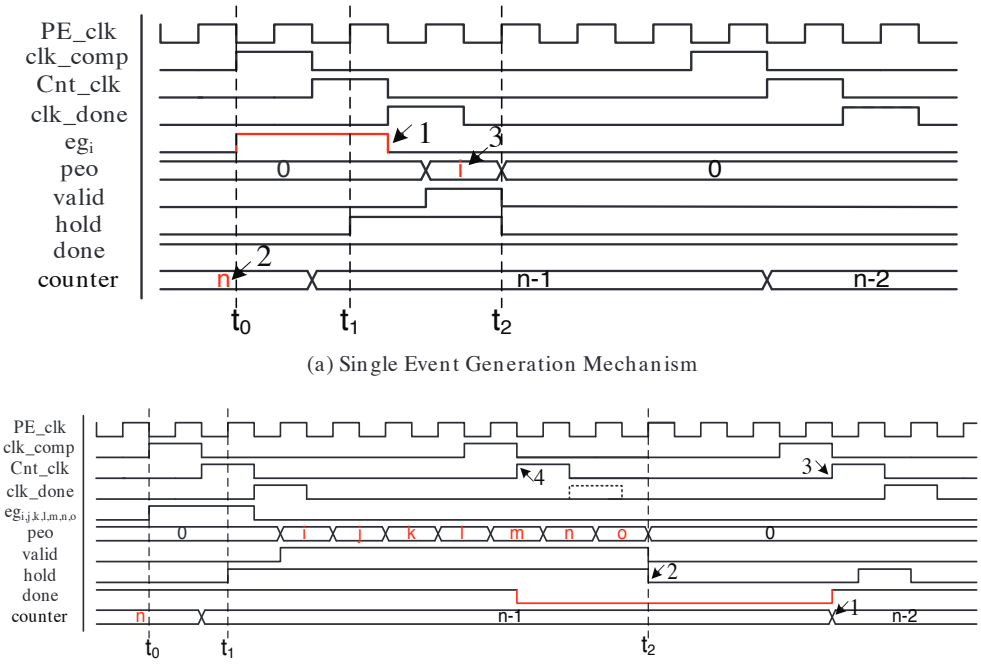


Figure 9.4: Event Generation and Priority Shifting Principle [Köklü et al., 2013c]

(pointer 3), the counter keeps its previous value (pointer 1).

The idea of a priority encoder is similar to AER Address Event Registration protocol but the difference is that the pixels do not require acknowledge or request hand-shaking signals since each pixel uses a separate output line. After passing through the priority encoder, the location information of the pixels are represented by 7 bit data for 120 row lines. The read-out of each column output is considered to be serialized by multiplexing the column outputs with an 8-bit Multiplexer. The final output of the overall system should be considered to include the serialized priority encoder outputs together with the encoder's Hold and Valid and the counter's Done signal output. These signals will be used to regenerate the counter value at the time of each event for the corresponding active pixels when constructing the images. The clock of the counter, priority encoder and the main clock of the system is also expected to be known during this read-out.

The proposed design consumes a total pixel array area of 1505.62µm × 4566µm for a pixel array size of 160(H) × 120(V) and the overall pixel array reaches a fill factor of %34 which is more than two times higher than the design in [Kleinfelder et al., 2001].

Similar to other digital pixel sensor designs, this design benefits from the inherited advantages of DPS architectures e.g. wide dynamic range and gets rids of the limitations of analog design and extra (ADC) unit while requiring less area and higher fill-factor than the related state of the art designs [Kleinfelder et al., 2001] and [Guo et al., 2007]. However, this design is not intended

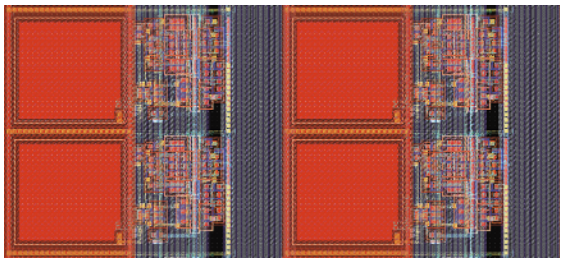
for use in very high-speed applications since it is not required for most of the biomedical applications so it is not integrated with pixel-level memories. Instead, every pixel is compared with the current value of the counter at the same time, the ones that show activity with that value queue their output by using priority encoders per column. Since this implementation requires the event generation output of each pixel to be held for a longer time than the one in Fig. 5.6, it results in lower speed.

The main drawback of this design is that every pixel has its own output bus lines connected to each column level encoders. With this method, I have avoided the use of extra request/acknowledge signals. In [Guo et al., 2007], due to the large area of pixel control unit for communication with the Address-Event Protocol (AER) for request/acknowledge signals, the pixel has reached again a large non-photosensitive area. This causes our event-detection design to be advantageous in terms of area and fill-factor only for low array sizes (lower or equal to Q-QVGA). In the current design, each pixel bus line goes through the other pixel circuits such as comparator, XOR gate and the memory. By this way, the pixel output buses do not require extra space. The layout of a 2×2 pixel array of this design is shown in Fig. 9.5a and the top level layout is shown in Fig. 9.5b. However, for higher resolution designs, the pixel output bus lines would require more space than the area of the pixel circuits which is the limiting factor of this design.

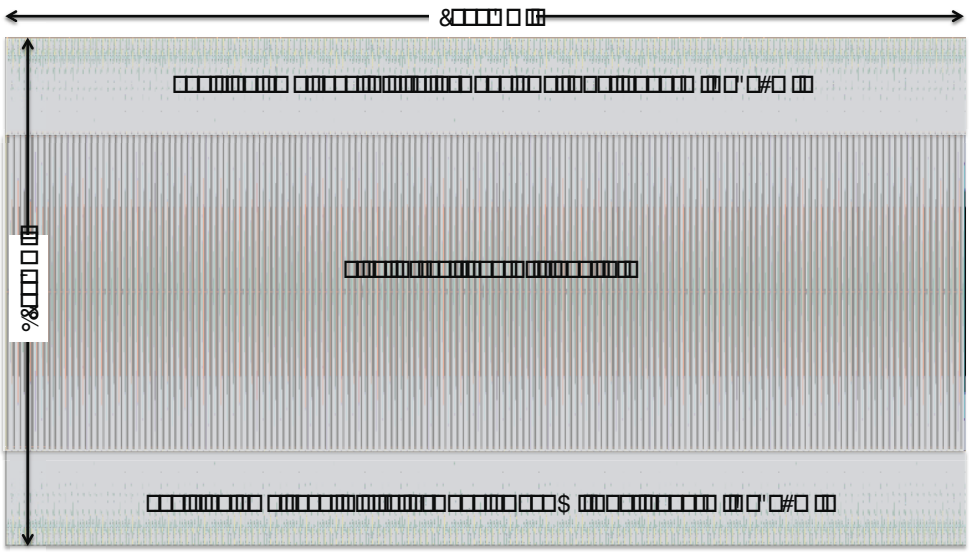
In addition, for the 1-bit register cell of each pixel, 5-T SRAM is preferred due to its lower area as seen in Fig. 9.6a and its timing diagram in Fig. 9.6b. The DRAM Dynamic RAM as in Fig. 5.6 is not considered as an option for this design although it can be implemented by 3 transistors only, since DRAMs tends to discharge and loose their value during long exposure time. For this design, since each pixel requires to keep it is value until the priority is given to it, I preferred a static memory instead of a dynamic one. Thus, this sensor is appropriate for long-exposure times, which is of great importance for low-light biomedical applications.

This design has been implemented by using UMC 0.18µm standard CMOS process. With this proposed design, each pixel continuously monitors its photo-voltage for events and the location of the corresponding pixel with the event is registered. The address of the pixel with the event is encoded by means of a priority encoder. The sensitivity (minimum detectable light) and the dynamic range of the image sensor are determined by the comparator and counter resolution, which are both 10-bits in this implementation. However, depending on the application the counter and the DAC can be designed with higher resolution without bringing a large area penalty since these blocks are already present per column or per chip.

During this design, analog, digital and mixed signal simulators and design environments are used. I designed the photodiode, comparator, 5T-SRAM, the logic gates and the DAC blocks in full-custom and simulated them by using Cadence Analog Environment Spectre Simulator. I implemented the RTL level design of the counter and priority encoder parts in verilog and synthesized with Design Compiler Tool. The synthesized design is placed and routed by using the Encounter Tool. For overall system simulations, first I used Cadence Analog

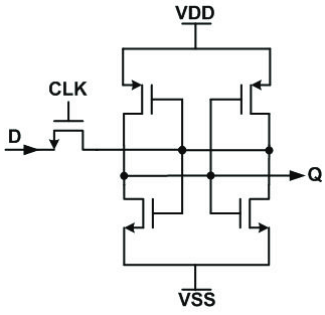


(a) Pixel Layout

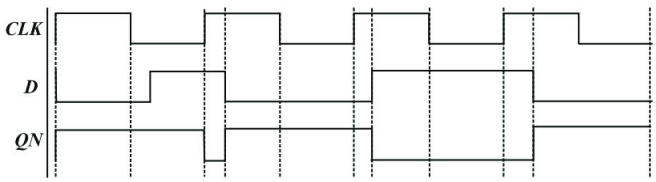


(b) Top Level Layout

Figure 9.5: Event Detection Design Layouts [Köklü et al., 2013c]



(a) Schematic View of the 5-T SRAM



(b) Timing Diagram of the 5-T SRAM

Figure 9.6: 5-Transistor SRAM Cell [Köklü et al., 2013c]

Environment with mixed mode simulators (SpectreVerilog Simulator) and after importing the placed and routed digital designs to Cadence, I used Cadence Spectre Simulator for post synthesis simulations.

As mentioned earlier, this design is limited in terms of the total array resolution due to the single output lines of each pixel. Thus, this design can only be advantageous for small pixel arrays. In order to solve this problem, a hand-shaking protocol should be integrated in the pixel to decrease the number of outputs per column. However, this implementation will obviously increase the pixel area. In the next section, our next DPS pixel design with hand-shaking protocol will be presented.

9.2 An Event-Detection DPS with AER Protocol

This design aims to overcome the limitation of the previously proposed design with minimum area overhead. By implementing a hand-shaking protocol, it allows every pixel on the same column to share a common output. The technique is similar to the previous design and is based on binary search where the digital control logic (counter) decrements bits at each clock cycle. After each decrement, the pixel integrated voltage is compared with a ramp voltage.

The pixel includes a reset transistor, a comparator, and a 1 bit memory similar to the previous design. In addition to those, there are extra transistors for column and row request and acknowledge signals as shown in Fig. 9.7. The row request signal is connected to the output of the comparator by use of a PMOS transistor named as M_1 and an inverter. In order to keep the row request signal low when the pixel is not excited/ triggered, an NMOS weak pull-down transistor named as M_2 is used. Similarly, there is another NMOS weak pull-down transistor named as M_5 to keep column request low in the same manner. The M_3 and M_4 PMOS transistors are used to pull up the column request line to V_{DD}, which are active when their inputs are "0" i.e. when the pixel is triggered.

The top level schematic of the design is shown in Fig. 9.8. As seen in this figure, the design includes a global counter, a Digital to Analog Converter (DAC), row and column arbiters, row and column encoders, and OR gates at the column and row arbiters for global reset.

The timing diagram of the design when single pixel is active is shown in Fig. 9.10. First, the design is in reset mode, with the Global Reset signal being high. This condition provides both row and column acknowledges to each and every pixel. Thus, with the Global Reset, each pixel transfers the initial comparator output of "0" to the output of the D-latch and to the input of the M_4 transistor while the input of the M_1 and M_3 transistor is "1". This guarantees that each pixel starts a new frame with both column and row requests at "0". This condition is illustrated with Fig. 9.9a.

When the Global Reset is no longer active, first the ClkA is set to high. With this clock, M_{RS} transistor is switched on and the photodiode is reset to VDD – Vth or Vset - Vth depending

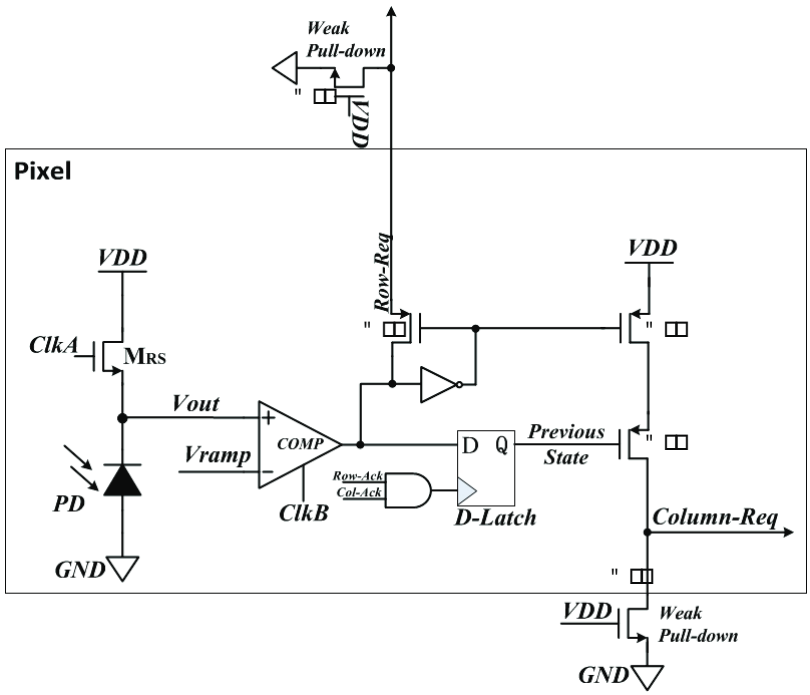


Figure 9.7: An Event-Detection Pixel with Hand-Shaking Protocol

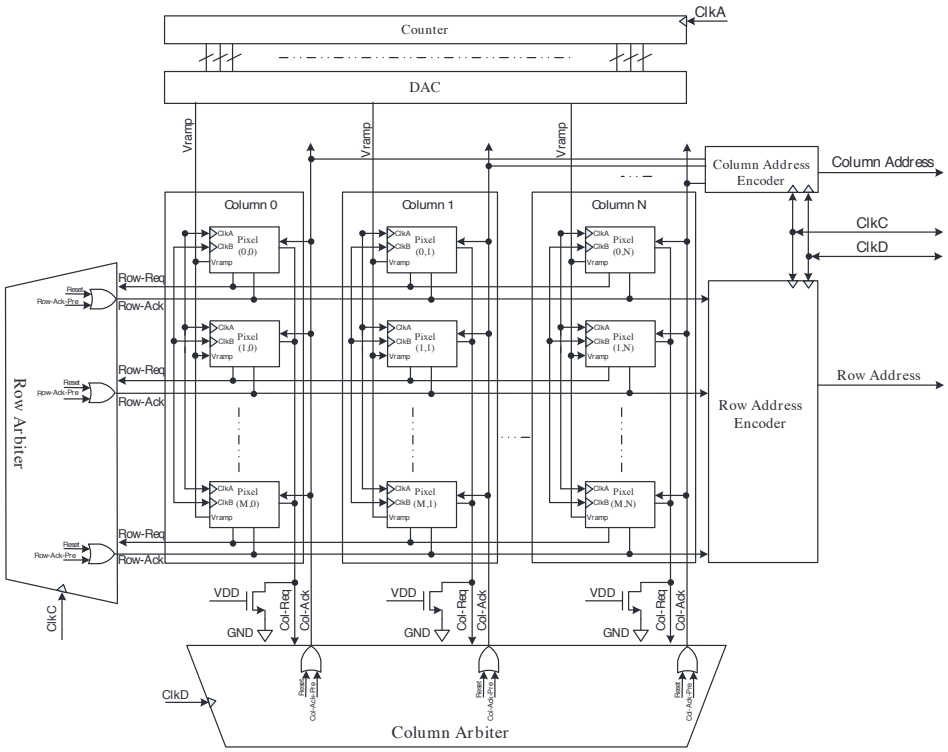
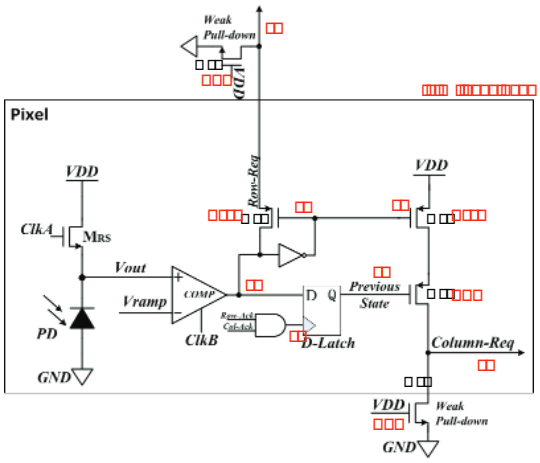
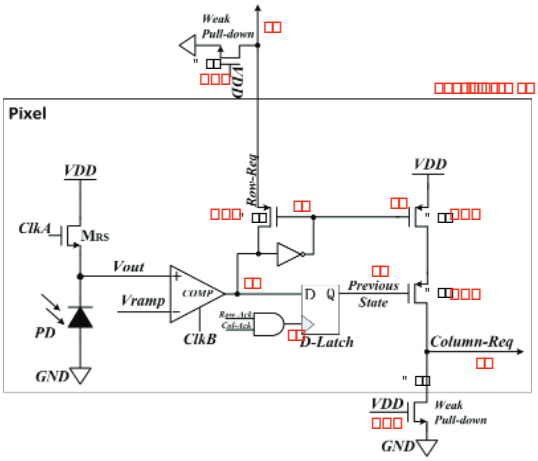


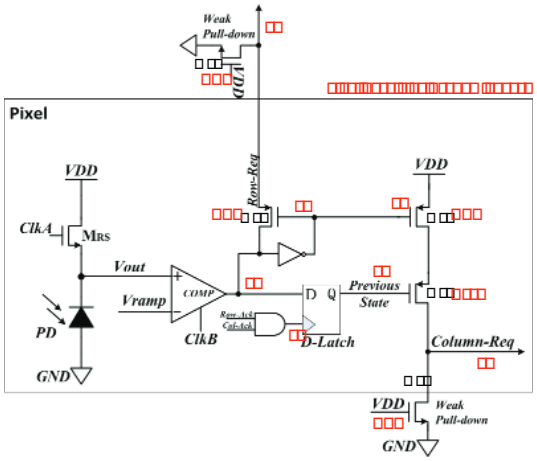
Figure 9.8: An Event-Detection DPS with Hand-Shaking Protocol



(a) Pixel under Global Reset



(b) Pixel with Activity



(c) Pixel Receving Acknowledges

Figure 9.9: An Event-Detection Pixel Working Modes

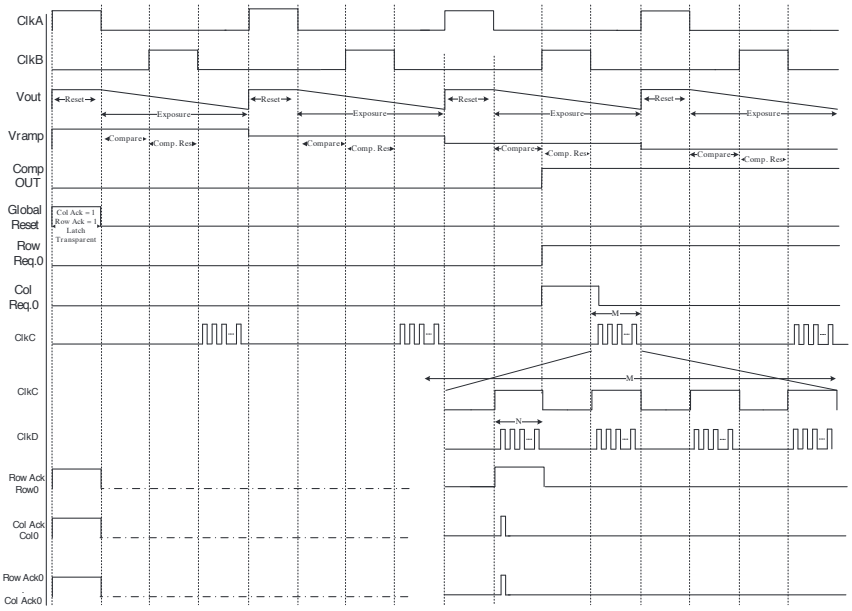


Figure 9.10: The Timing Diagram of the Single Event-Detection

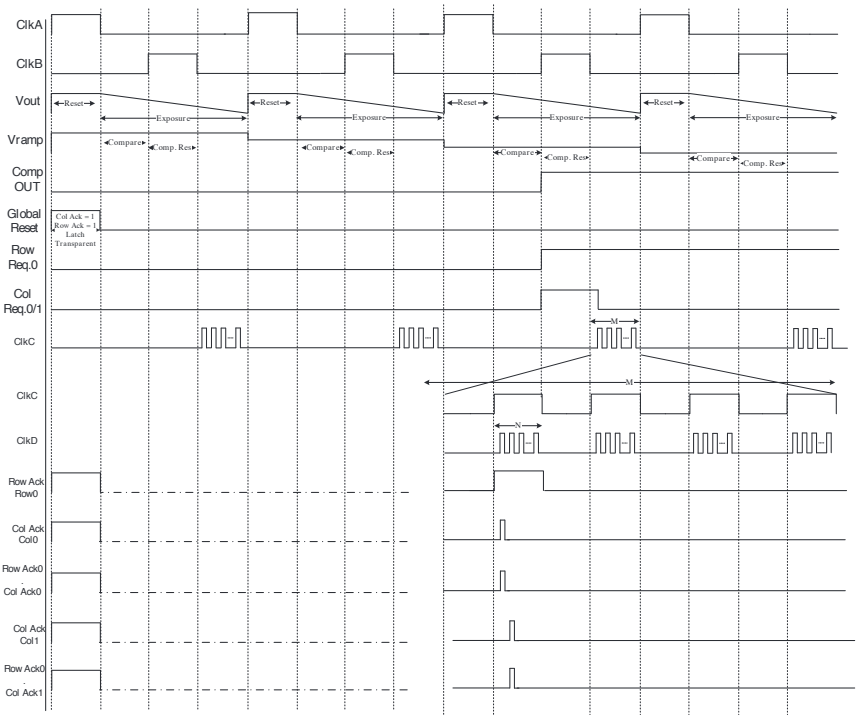


Figure 9.11: The Timing Diagram of the Multiple Event-Detection

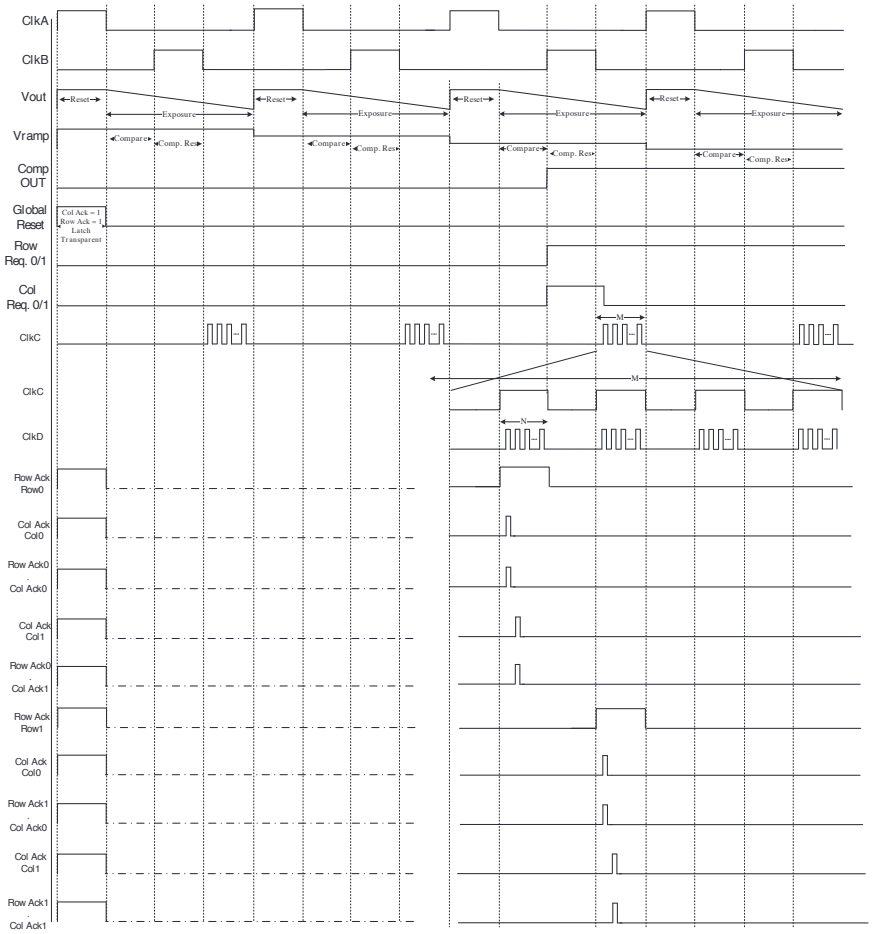


Figure 9.12: The Timing Diagram of the Multiple Event-Detection Case 2

on the source voltage of the M_{RS} transistor. Later, when ClkA becomes low, the photodiode is no longer in reset mode and the photodiode voltage value starts to discharge with a slope determined by the light intensity exposed on the sensor. In the next phase, when ClkB becomes high, a comparison between the current value of the ramp voltage and the integrated photodiode voltage is made. Since the ramp voltage decreases at each clock cycle, at some point it becomes smaller than the pixel integrated voltage and the comparator results with a "1", triggering both row and column requests. When the pixel receives both row and column acknowledges, the corresponding value in the counter should be registered as the value of that pixel by use of the row and column encoders as shown in Fig 9.8. This behavior is illustrated with the Fig. 9.9b and the timing diagrams can be found in Fig. 9.10.

The arbiter cells give acknowledge only once to each pixel and they use faster clocks (ClkC and ClkD) than the ClkA and ClkB in order to switch the priority from one pixel to another when multiple pixels are active at the same time. In Fig. 9.11, the response of the sensor in case of multiple pixels are active is represented. In this figure, it is shown that when both Row0

- Column0 and Row0 - Column1 pixels are active, the row arbiter gives the acknowledge to the 0th row and the column arbiter first gives acknowledge to the 0th column and in the next clock cycle of ClkD, it shifts it to Column 1.

The resulting waveform of a case when there are two pixels active at two different rows at the same time is shown in Fig. 9.12. In this case, during the 1st clock cycle of ClkC, row acknowledge is given to Row0 and Column0 and Column1 consequently with the ClkD. During the next clock cycle of ClkC, the row acknowledge is shifted to Row1 and again consequently to Column0 and Column1 with ClkD.

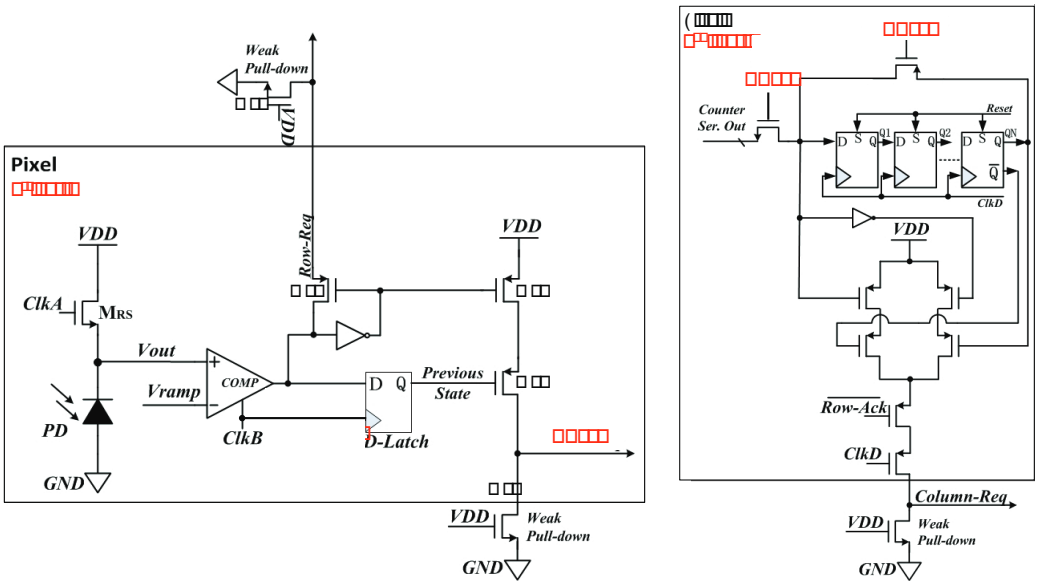
Although, this design solves the issues of the previous DPS design with a hand-shaking protocol, it does not bring change detection feature. For this purpose, a DPS design with change detection feature is proposed in the following section.

9.3 AChange-Detection DPS with AER Protocol

DPS cameras easily offer additional features such as change detection and reduction in data redundancy ([Culurciello et al., 2003], [Mallik et al., 2005], [Chi et al., 2006], [Posch et al., 2010], [Delbruck et al., 2010]). Since the target molecules in biomedical applications usually response or change very slowly, it requires the scientists to observe the experiments for a long time which can be minutes, hours, days or in some cases weeks. For such cases, I propose a DPS design with an additional functionality of change detection which would help to automatically generate an image when there is a change in the target. In this design, I target frame-to-frame change detection which means that after generating the 1st image, the camera looks for possible change in the pixels compared to the previous frame and the new image would include only the pixels' values that have changed. If none of the pixels' values have changed after the generation of the 1st image, then no new image is generated.

In Fig. 5.9, the change detection has been done through an additional pixel and it was not integrated with the exposure measurement pixel. This reduces the fill factor and may also cause inconsistent results since the photo-device for exposure measurements and change detection are two different devices at two different positions in a pixel and they may response differently. Thus, I propose a DPS design with change detection that is integrated within a single pixel using a single photo-device. In Fig. 9.13, the pixel circuit of our change-detection design is shown.

Similar to the event-detection design, this architecture is also based on binary search where the digital control logic decrements bits at each clock cycle so the ramp voltage. The first part of the pixel is shown in Fig. 9.13a and it is the same as the event-detection design in Fig. 9.7 except that the clock of the D-latch is controlled by ClkB which is the clock of the comparator. This part of the pixel generates an output only when the comparator output's previous value is "0" and the current value is "1". In all other cases, the output of this part stays at "0". The second part of the pixel is shown in Fig. 9.13b and it is used to detect change in the pixel from



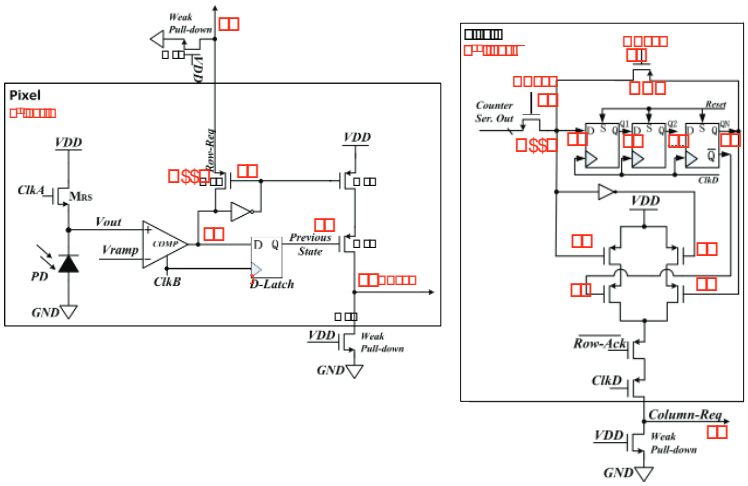
(a) Event Generation Part (b) Change Detection Part

Figure 9.13: Change Detection Pixel in Two Stages

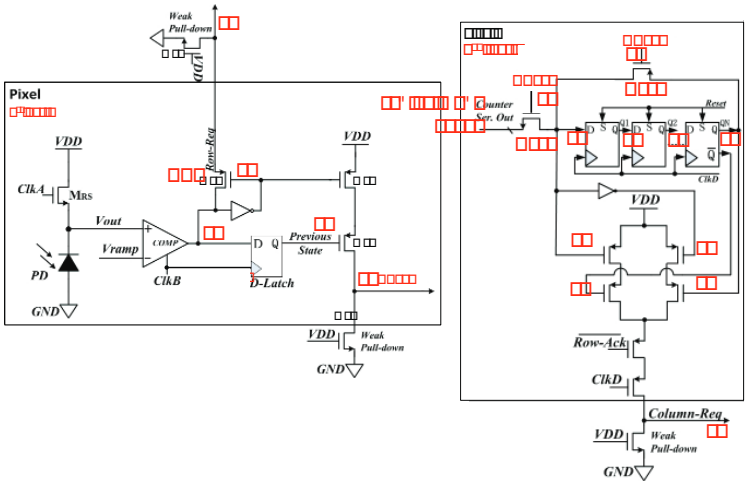
one frame to another. It includes a shift register unit with N number of D Flip-Flops depending on the resolution of the counter and the flip flops in the shift register are controlled by the ClkD which is N times faster than the pixel reset clock ClkA and the comparator clock ClkB. The input of the shift register is connected to the serialized counter output through an NMOS switch that is controlled by the output of the first part of the pixel. Thus, the serialized counter value is connected to the shift register input or the value in the shift register unit is updated only when the previous value of the counter is 0 and the current value is 1. In all the other cases, the shift register keeps its previous value. To make the shift register keep its value until the end of the image generation, a PMOS switch is used which shorts the input and the output of the shift register when the first part of the pixel output is "0".

Three different cases representing different behaviors of this pixel is illustrated with Fig. 9.14. Fig. 9.14a represents global reset condition. When the global reset signal is “1”, all the storage elements in the shift register units are set to 1, the comparator output is "0" and both row and column requests are pulled-down to "0". When, the global reset signal is “0”, at each clock cycle, the ramp voltage generated with a DAC-counter block is compared with the pixel integrated voltage. When pixel voltage becomes higher than the ramp voltage, the corresponding serialized counter value is transferred to the input of the shift-registers starting from the MSB to LSB. When the clock of the shift register (ClkD) becomes active, bit-wise comparison is made between the pixel value at the current frame and the previous frame.

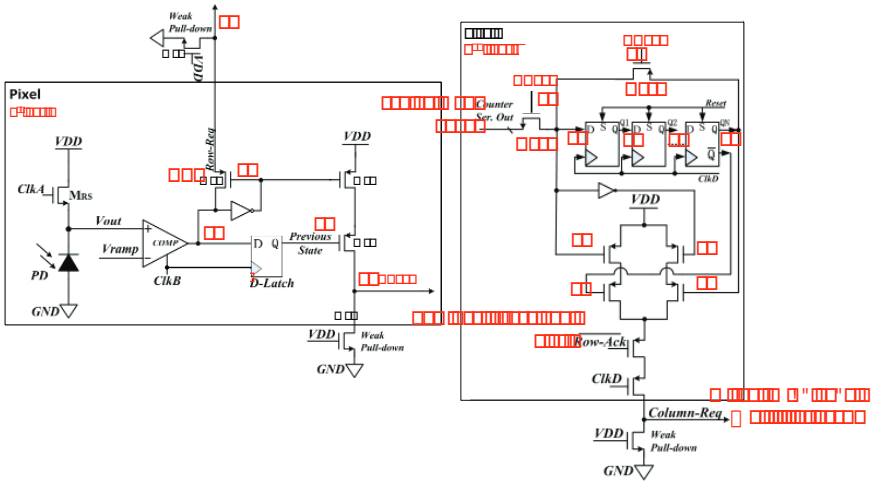
Fig. 9.14b represents the behavior of the pixel at the 1st clock cycle of ClkD. As seen tn this illustration, there is an activity at the pixel, so the comparator output becomes "1" and the counter serial output is 1101 starting from the LSB to MSB. Since the comparator’s previous



(a) Pixel under Global Reset



(b) Pixel with Activity - 1st cycle of ClkD



(c) Pixel with Activity - 2nd cycle of ClkD

Figure 9.14: Change Detection Pixel with Global Reset and with Activity

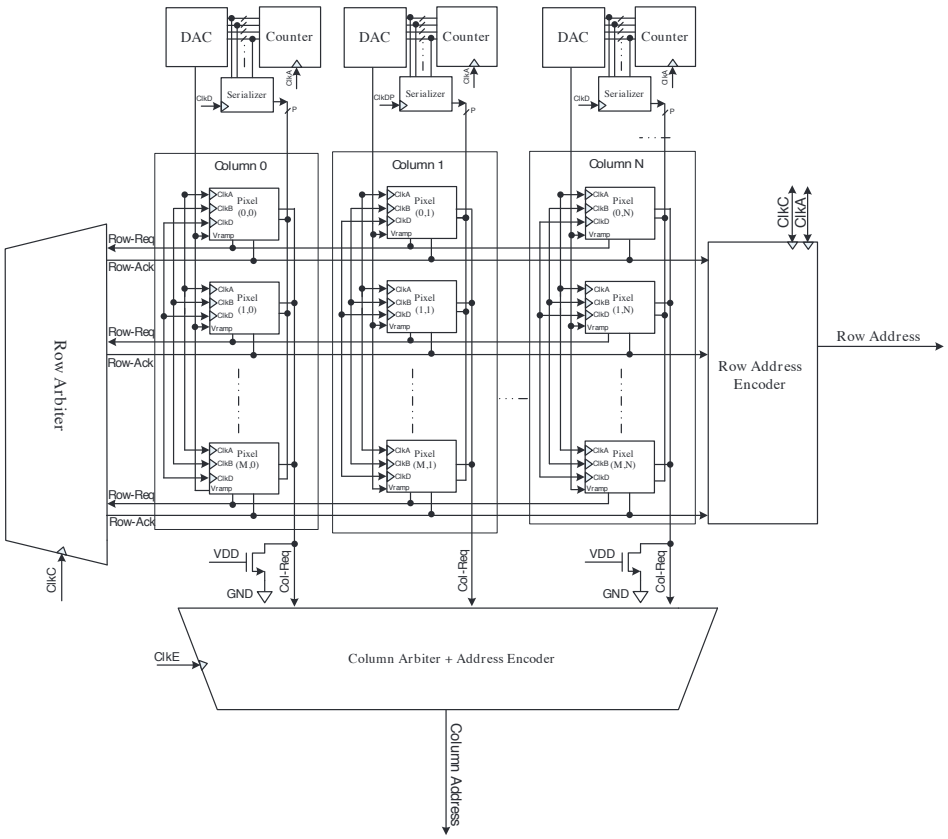


Figure 9.15: The Top Level Schematic of the Change Detection DPS Design

value has been "0" in global reset and the current value is "1", the first part of the pixel generates a "1", which connects the serialized counter output to the input of the shift register. Since both the MSB of the counter output and the output of the shift register (Q_N) are "1", the change in the pixel cannot be detected at the first clock cycle of ClkD. In the next clock cycle, as represented in Fig. 9.14c, the values in the shift register are shifted. The value at the output of the shift register is still "1" but this time, the new value at the input of the shift register is "0". This condition switches on two serially connected PMOS transistors in the column request network and when there is row acknowledge, at the falling edge of the ClkD, the column request is generated.

The top level schematic of this design is shown in Fig. 9.15. Since the timing diagram of this design is similar to the previous event-driven designs, the timing diagram is not repeated here.

9.4 Conclusion and Novelty

In this chapter, after investigating the DPS designs from the literature, I offered novel designs inspired by the ones in the literature. Two different event-driven pixels with less number of

transistors than that is currently offered in the literature are proposed. One of these designs has separate output for each pixel and the other uses common output for pixels in the same column. Second, I offered a change detection DPS sensor. Due to the slow response time of biological samples, I offered the change-detection sensor as a solution to automatically generate an image when there is a change in the target molecule without the need for a scientist to observe the sample and wait for a change to happen.

Although the APS designs provide higher fill-factor and photon collection efficiency, the DPS design can still be considered for biomedical applications when integrated with BSI technology. With this technology, the DPS designs no longer suffer from low fill-factor, meanwhile provide design flexibility and bring extra features.

10 Thesis Overview

Within the scope of this thesis, I first showed the reliability of the standard CMOS cameras for low-light biomedical applications by using an optical microscope, imaging real cell samples, and empowering those images with image processing algorithms. By showing the successful localization of target molecules and reaching high correlation data between collected images from the two cameras, I provided a proof-of-concept for scientists and recommended them to evaluate CMOS cameras for their applications before making a default selection of high-cost CCD cameras. Later, I showed the details of designs and fabricated chips to improve the quality of current standard CMOS cameras. I provided characterization data for the first time in the literature for designers using a 0.18 μm standard CMOS technology, which can be also consistent for other technologies using LOCOS. Thanks to the nature of 4T APS pixel architecture, I reached high conversion gain and low noise performance. Since the most important limiting factor in standard CMOS cameras especially for biomedical applications is their noise floor, I put special attention on the implementation of true CDS operation within this thesis. For that purpose, I provided two novel CDS designs, where one includes internal offset compensation. These noise reduction circuits not only allowed fully differential outputs with easy switching operations but also omitted the requirement for extra pseudo differential to fully differential conversion steps within the sensor. Further enhancements in these circuits may include design of offset and gain compensation with low area overhead.

The camera prototype that I have presented within this thesis reached good quality images, although the lens has not been optimized for such small arrays. The camera could differentiate lines that are even sub-millimeter distant from each other. I further enhanced this camera chip with a novel re-programmable VGA camera chip. With this new chip, I reached a larger array format in digital output, higher fill factor, and flexibility in improving the photon collection efficiency for low-light imaging conditions without requiring extra circuits.

Finally, I also provided possible ideas and road-maps for future developments in DPS designs for biomedical applications.

11 Conclusion and Future Perspective

After the invention of the camera on a chip concept with CMOS image sensors, it was expected by many people that CCDs will disappear sooner or later and loose their market share completely. In 1993, E. Fossum has carried out the question in the same context: “Active pixel sensors: are CCDs dinosaurs?”. However, 20 years after this question has been brought up, CCDs still preserve an important role in the market especially for high-quality and biomedical imaging applications. That is also why, the research interest towards better CMOS image sensors is still alive.

Especially with the cost, lower consumption, and high integration advantages of CMOS image sensors, today, we use digital cameras in every aspect of life. The first thing that may come into our minds when we consider CMOS cameras is obviously their use for personal entertainment. However, these cameras also massively contribute in security and health care systems. With the introduction of low-cost single chip cameras, it is now possible to imagine/use devices, PoCs and LoCs, for early detection and diagnostics of many diseases even by ourselves at home. These devices will increase the life span and the quality of life and will soon become inevitable for our lives. Moreover, with further advancements in the quality of these devices, while keeping their costs low, it is possible to increase the accessibility to high quality health care detection systems in under-developed or developing countries. Hence, it is important to focus on new CMOS camera design, implementation, and optimization solutions without causing an increase in their cost.

One important handicap for scientists, who work in biomedical field, is the slow response time of the target samples. This would require the scientists or the researchers to observe the samples for a long time, yet have the risk to miss the changes in the target. Cameras integrated with change detection options or automated post processing units within the cameras may serve very well for biomedical applications by automatically generating images with change information only. This technique when used in the hospitals can also save time for doctors and the patients. Thus, the automatic generation option for new generation cameras not only paves the way for faster analysis but also reduces the data redundancy and provides data compression. Although, the automatic generation of images can be made by

post processing units by using APS designs, the DPS designs allow much faster and efficient implementations. Thus, in the future, more interest towards DPS designs can be expected with additional chip-level features that will ease our lives.

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