Reconfigurable Nanowire Electronics – Device Principles and Prospects

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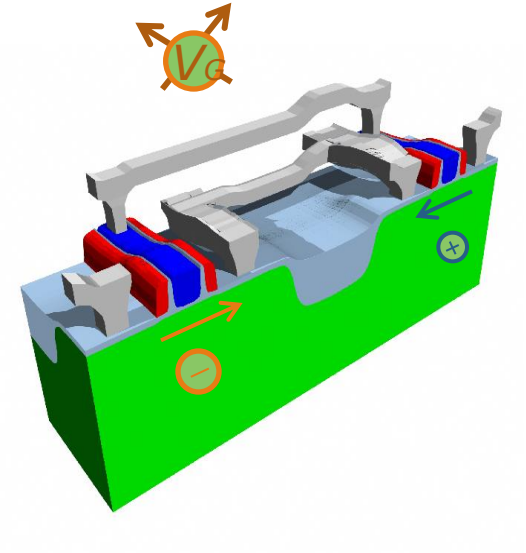
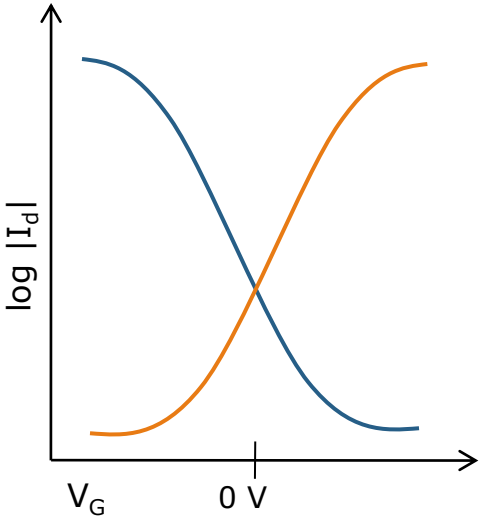
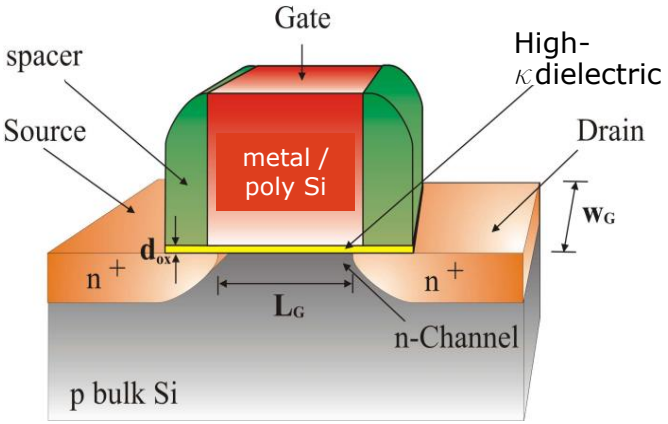
Basics and limitations of present CMOS technology

- ~ 88 % of IC market ($320 bn: 2013) covered by ***CMOS***
- **n-** / **p-** FETs alternated to constrain energy consumption to the switching event
- **n-** and **p-** FETs differ in technology (doping, dev. dimensions, strain, gate)
- Limited to static and single switch - function



Inverter, modified from
S. Selberherr TU Wien



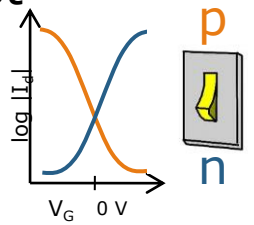


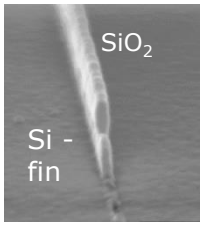
Simplified MOSFET

The quest for the "universal" transistor

Wish list for a universal nano-device for logic operations:

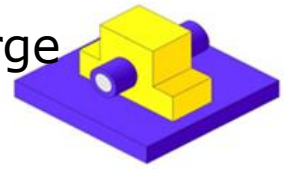
- Provide both n- and p- FET characteristics upon request
  - **->** Electrically configurable characteristics
  - **->** No pre-program routine
- Cost-effective and reliable fabrication
  - **->** Compatible with silicon technology
  - **->** Suppression of doping variability
- Sufficiently high performance
  - **->** Enhanced electrostatics: multi-gated nanowire geometry
  - **->** Circuit maturity: drive next stage´s charge

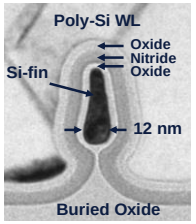




Infineon FinFET

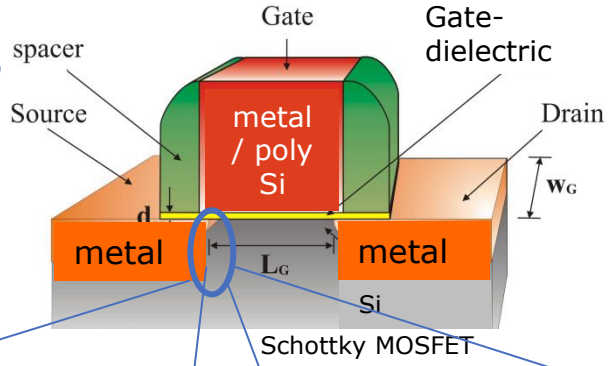
Intel FinFET





Infineon Trigate multibit flash

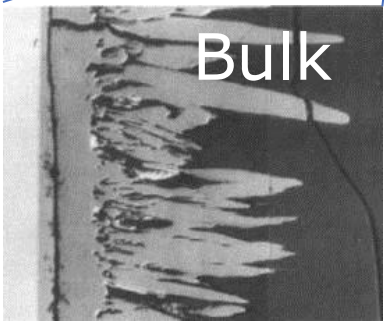
Approach & challenges with Schottky FETs

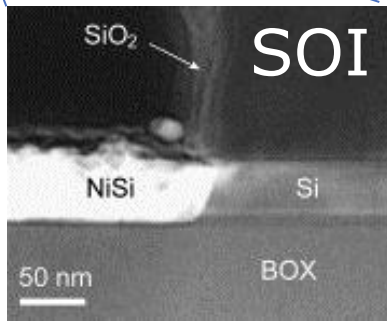


- Intrinsic Si with near midgap metal electrodes.
- Filter out segments of ambipolar IV charact.

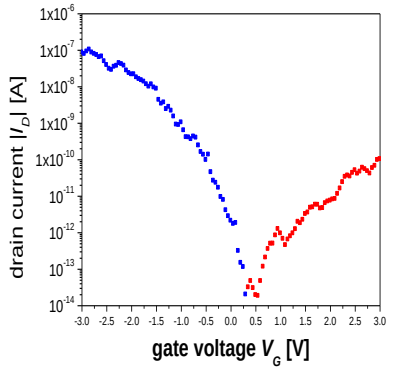
Issues with SBFETs to be solved :

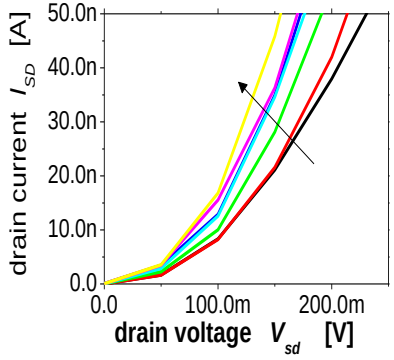
- High variability (varying junction areas)
- Low drive currents (tunnel barrier in on-state)
- Degraded off – state > *ambipolarity removed*
- Exponential turn-on in output characteristics (presence of energy barriers)





S Feste (2009)





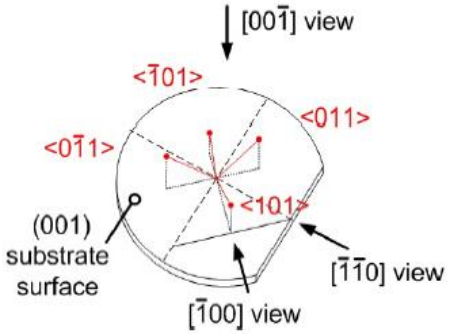
Intrinsic Si-nanowires as vehicles

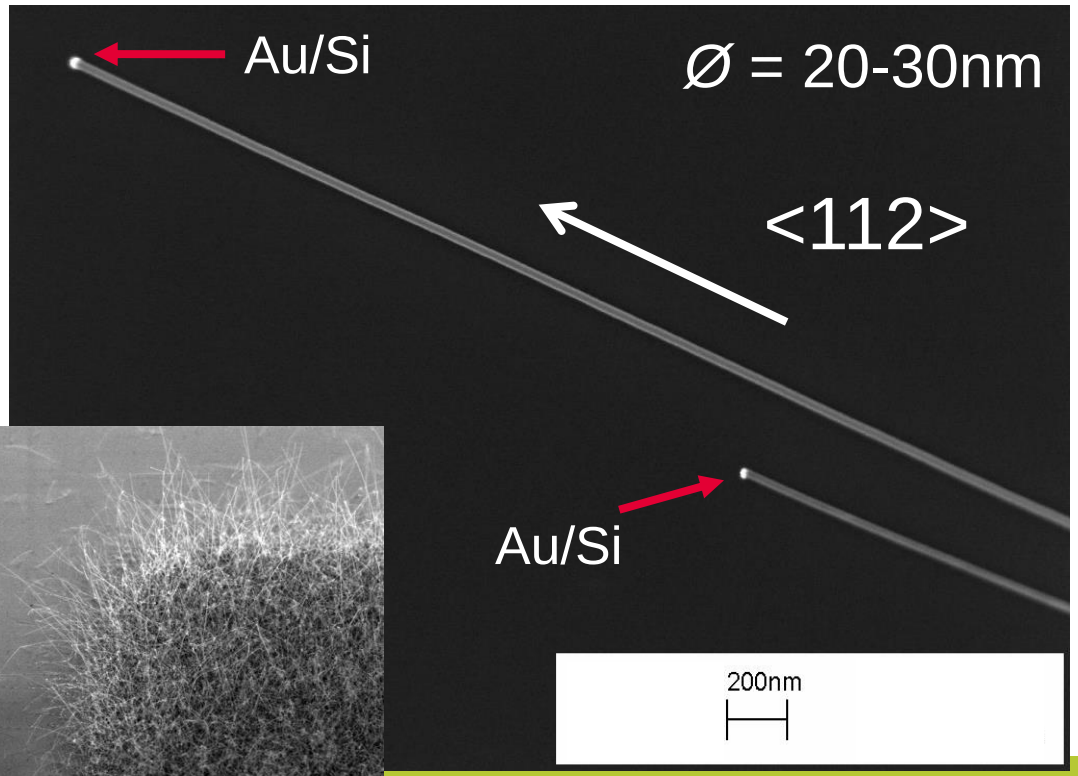
VLS / VSS growth

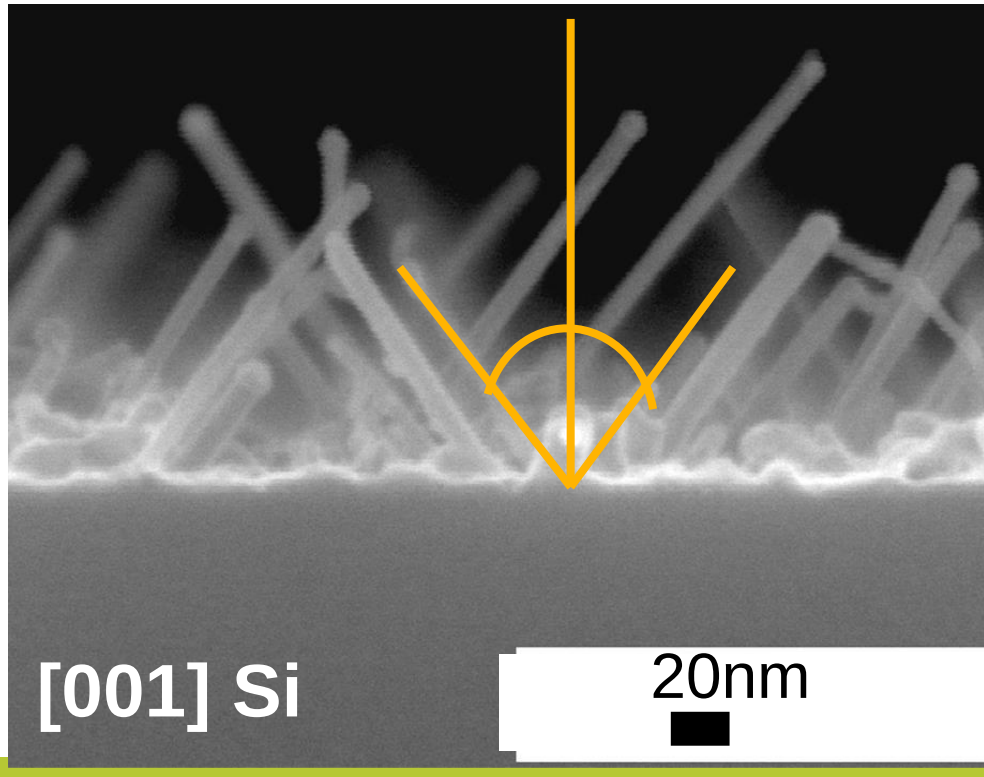
Controllable diameters, starting from Ø ~ 3nm

Diameter dependent lattice direction

thinner NWs <- <110>; <112>; <111> -> thicker NWs







W.M. Weber, et al. IWEPNM 2006 *PSSb 243, (2006)*

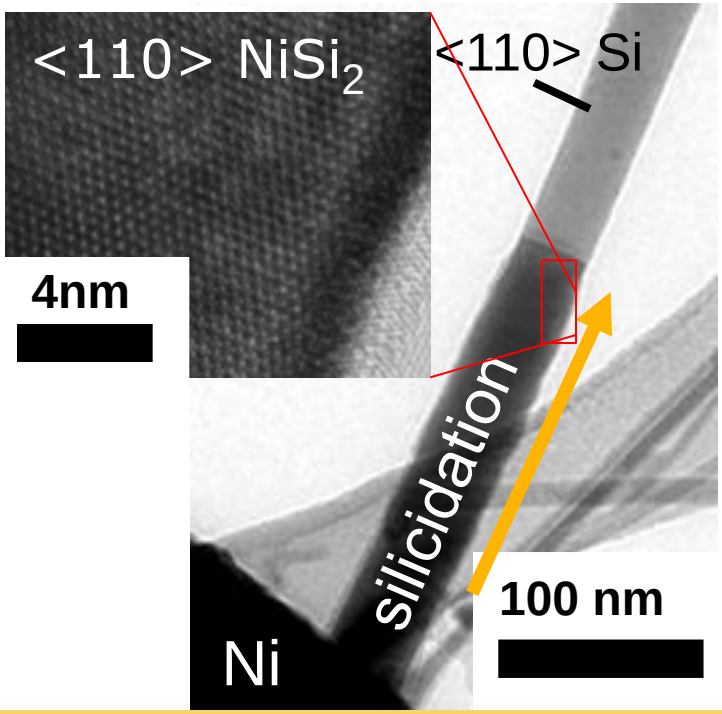
Ni - Si nanowire solid state reaction kinetics

- Phase formation dependent on crystal orientation:

<110> -> Direct cubic $NiSi_2$ lattice matched nucleation

- 0.4 % lattice mismatch to Si <111>

<112> -> Sequence: Ni_2Si / NiSi / $NiSi_2$

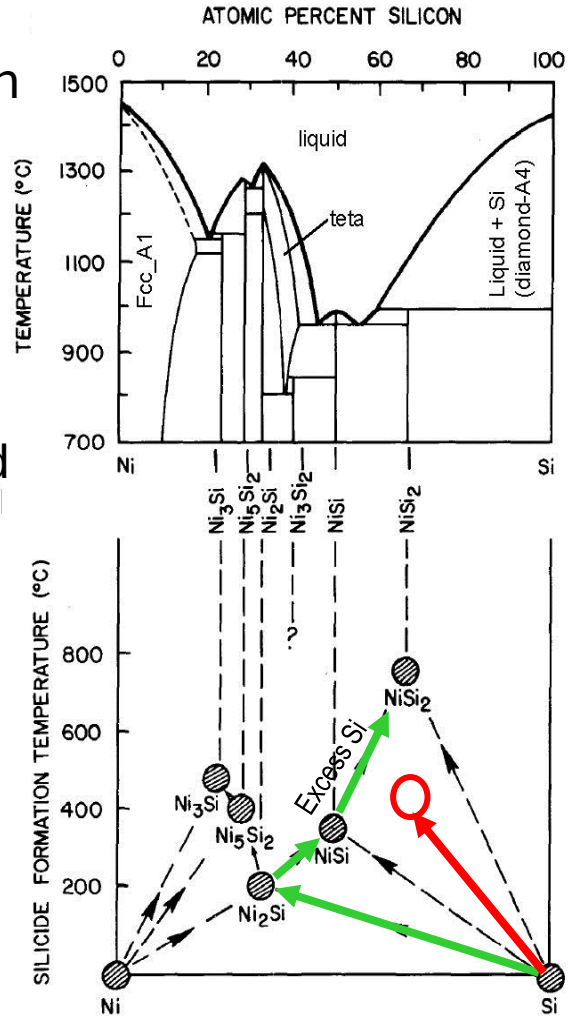


Long range, diffusion limited

$$d \sim \sqrt{t}$$

Short range, interface-reaction limited

$$d \sim t$$



W.M. Weber et al. *Nano Lett.* **6**, 2660 (2006)

Sharp and flat interfaces-> known junction area -> low variability

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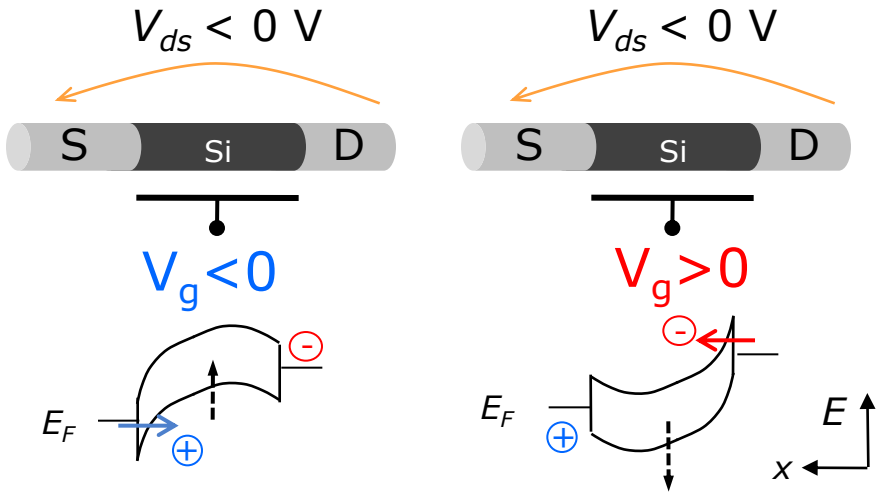
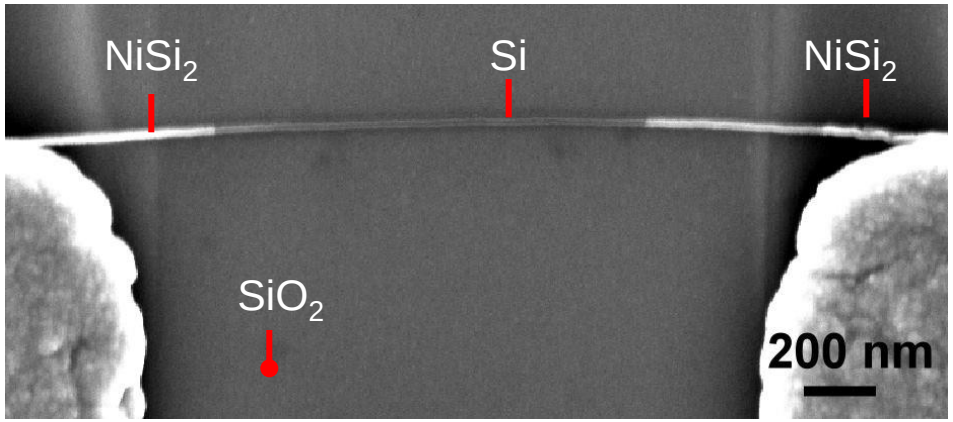
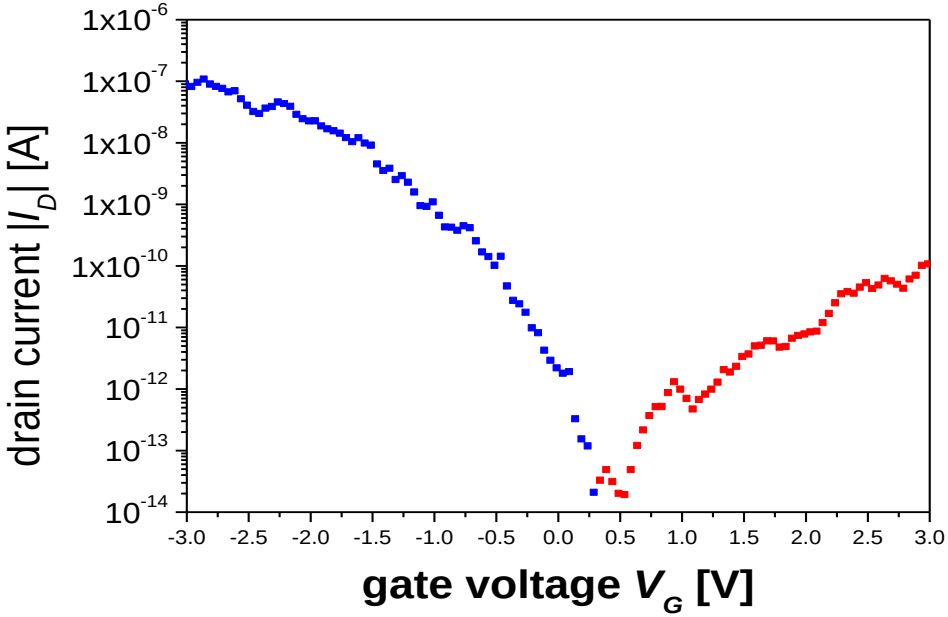
Working principle Schottky FETs

- i-Si: depletion / accumulation
- Field induced band bending at junctions
- Injection of both electrons and holes
  -> ambipolar behavior



SEM top view of a Si-NW -FET





Reference: bulk $NiSi_2$/Si

$e\Phi_{B\ \text{holes}}$ = 0.39-0.48 eV

$e\Phi_{B\ \text{electrons}}$ = 0.66-0.75 eV

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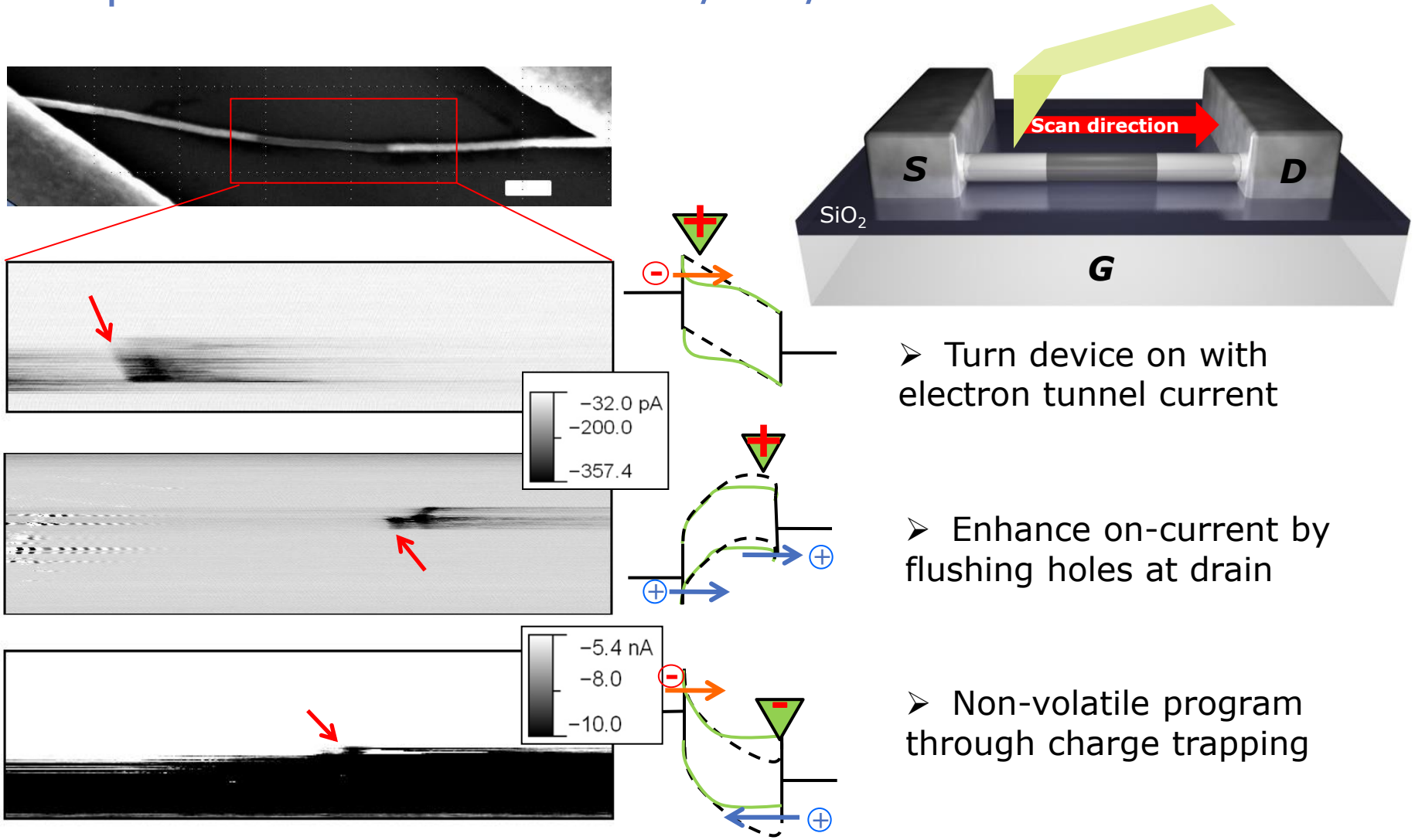
Transport alteration in metal / Si / metal nanowires

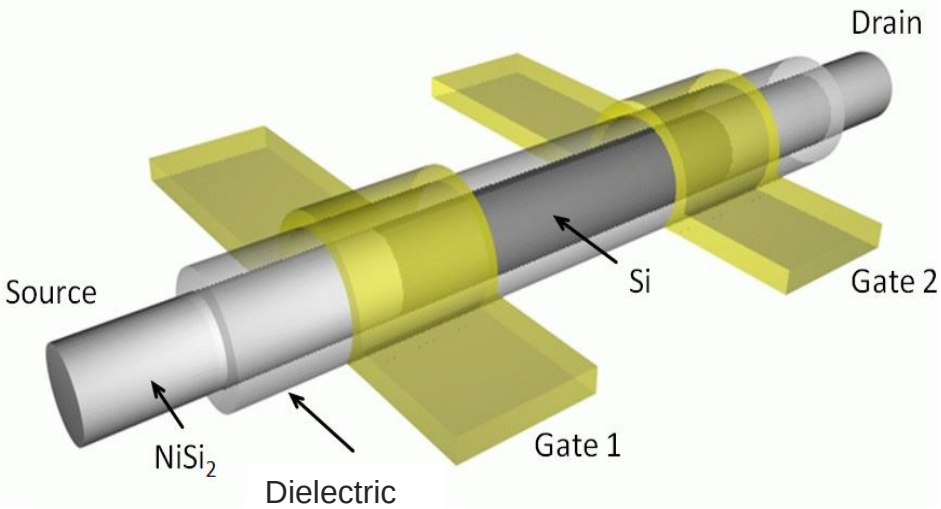


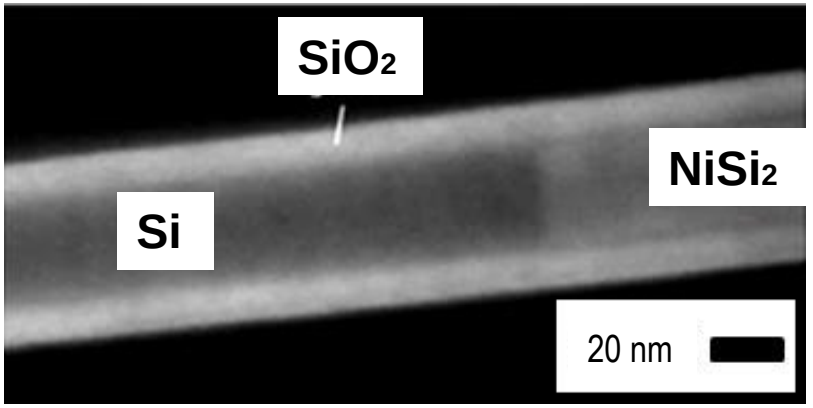
- Turn device on with electron tunnel current
- Enhance on-current by flushing holes at drain
- Non-volatile program through charge trapping

- In contrast to a MOSFET a point potential selectively controls electron / hole transport

D. Martin, W. Weber et al. *Phys. Rev. Lett.* **107**, 216807 (2011)

RFET: Reconfigurable Si nanowire FET

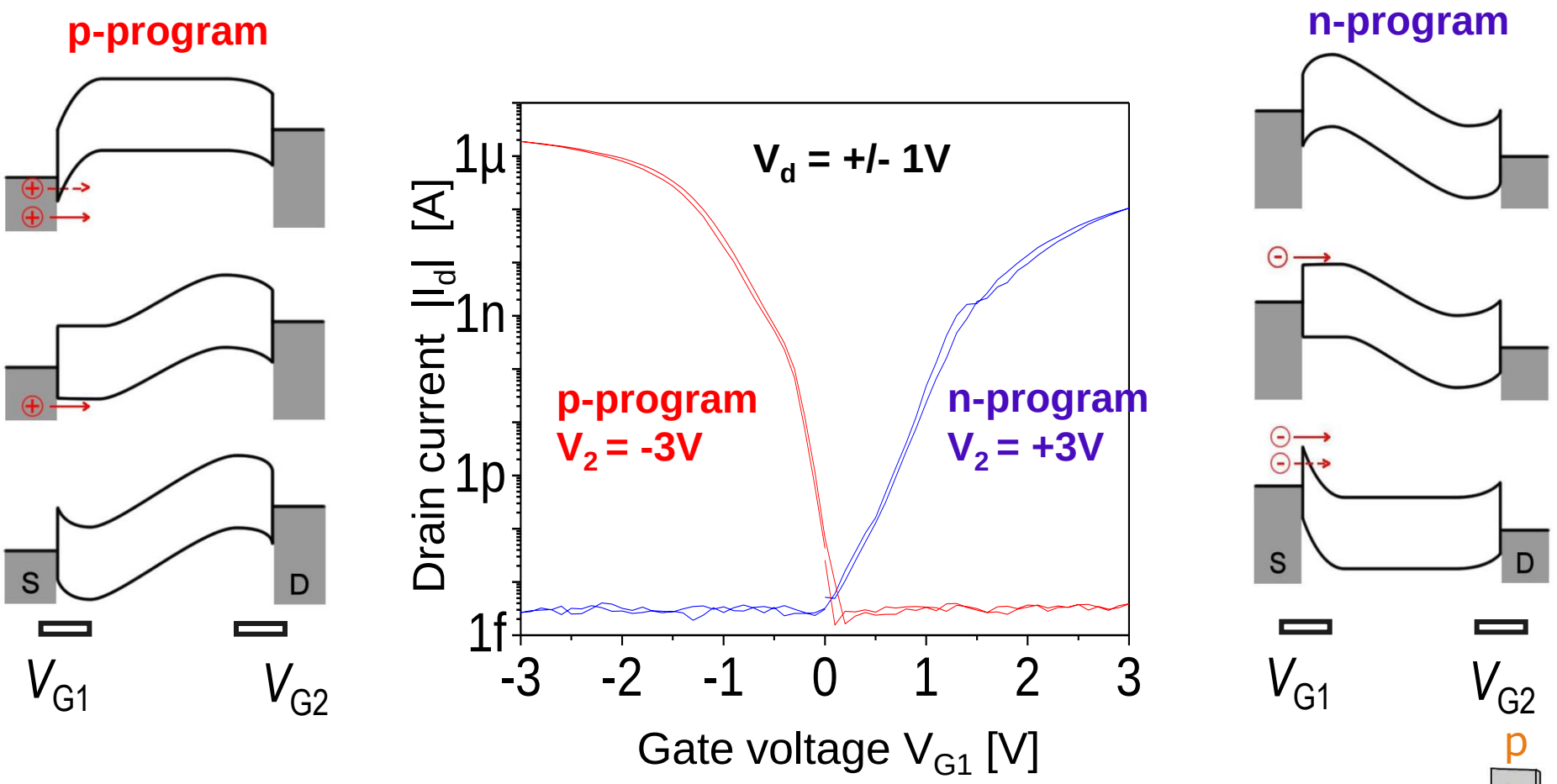




- Longitudinal nanowire heterostructure: $NiSi_2$ / intrinsic Si / $NiSi_2$
- Thermal silicon dioxide shell -> No need for extra spacer
- Individual gating of each Schottky junction -> valves for electrons / holes

A. Heinzig, W. Weber et. al Nano Lett 12, 119 (2012)
Weber, W.M. et al. *IEEE Proc. Nanotech Conf. 2008*, p. 580 (2008)

Reconfigurable Si nanowire FETs

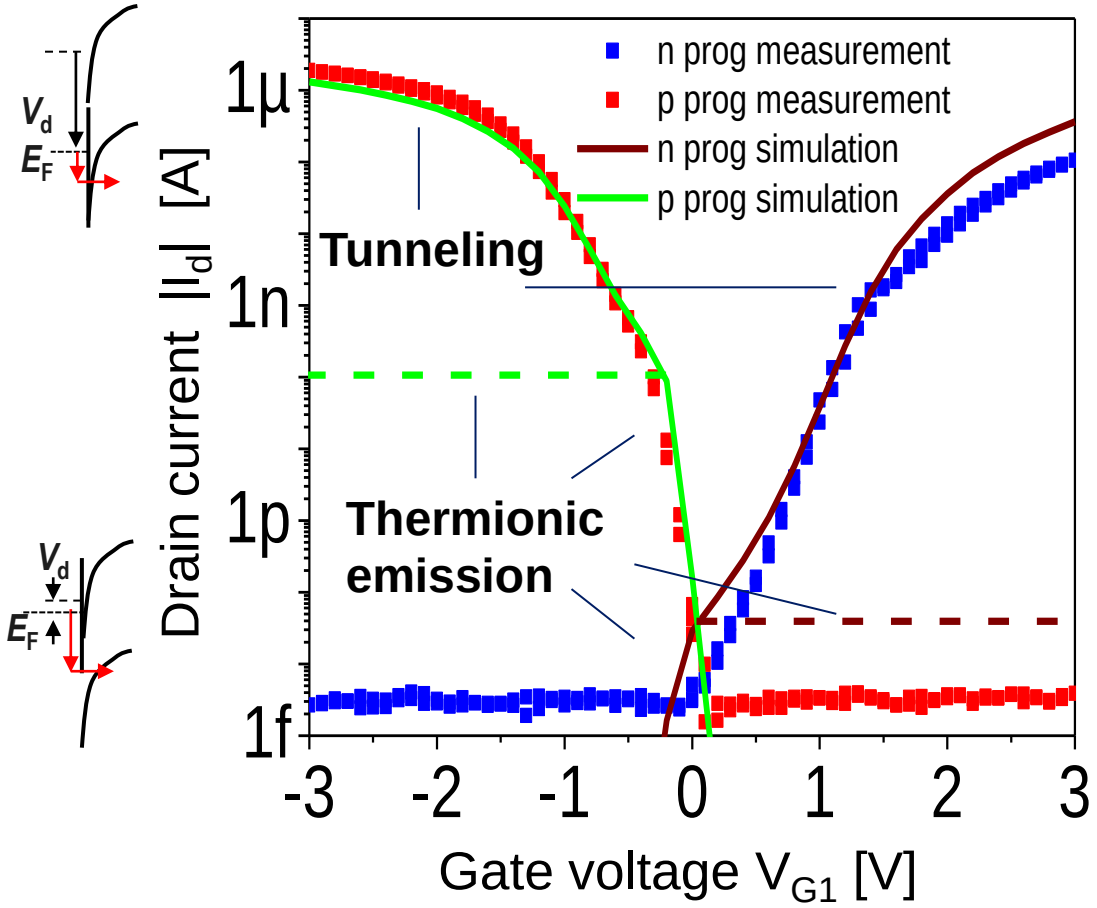


- Same FETs provide p- and n- type transport: leaner complexity
- Higher device functionality -> reprogrammable logic

Ion / Ioff > 5 x 10^7 ; *J*on = 6 x 10^5 A/cm^2 @ Vd=1V ; g_m = 130 µS/µm

A. Heinzig, W. Weber et. al Nano Lett 12, 119 (2012)

Reconfigurable Si nanowire FETs: transport



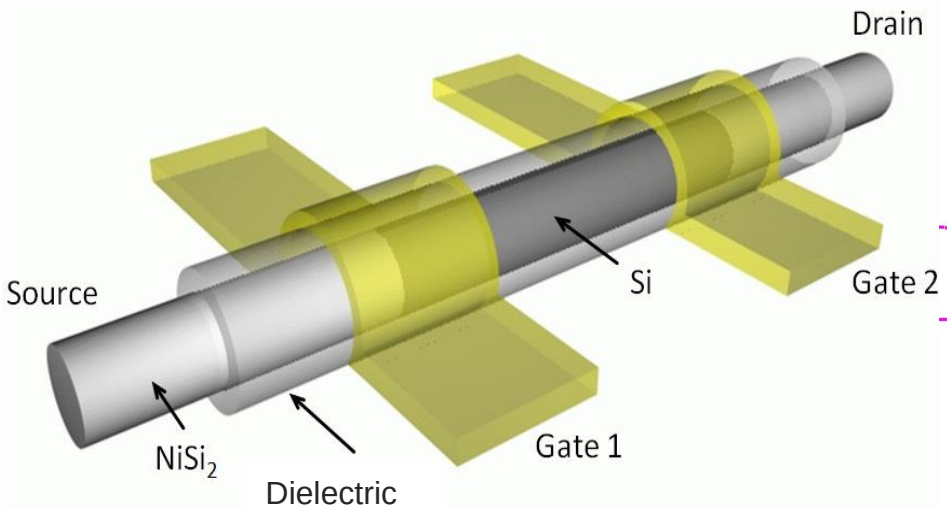
3D TCAD calc.(Sentaurus dev)

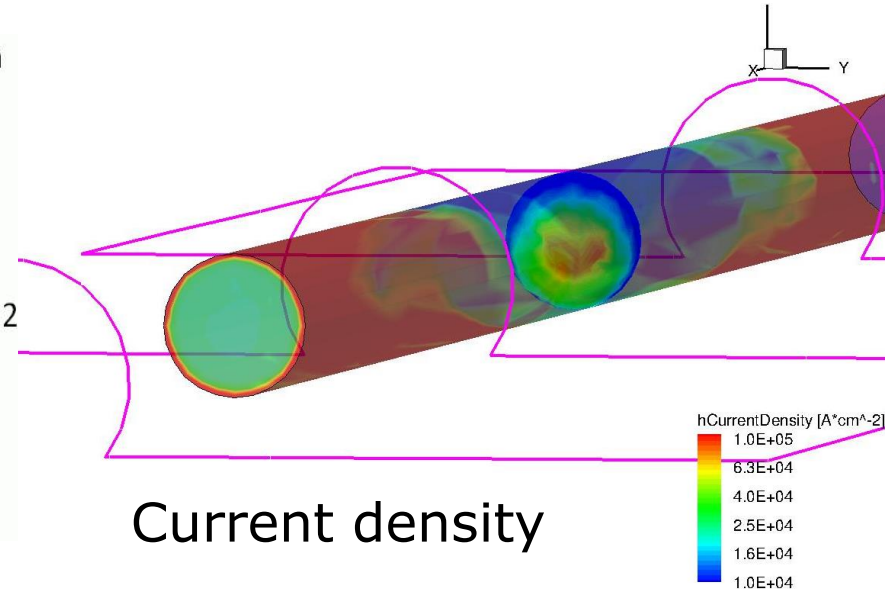
Drift diff. + WKB (tunneling)

- Sub- Vth region divided into tunneling and thermionic emission
- Drive current dominated by tunneling
- N-FET degraded by unequal SBH

Transport path: *sand glass form*

- Gated region at the nanowire surface / interface to dielectric
- Ungated region in the nanowire´s core
- Less scattering expected in active region

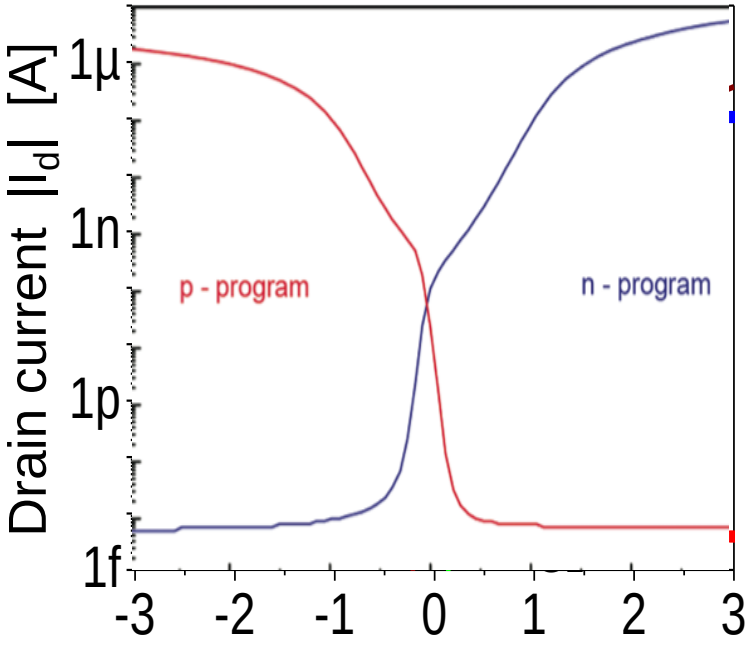




Current density

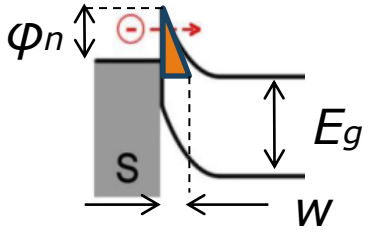
➢ Ultra low gate capacitances $C = 3*10^{-17}F$ / $Cg \sim 10^{-4}$ fF/µm

Prospects for enhanced symmetry & performance



- Trivial adjustment of barrier height φ_n *vs.* φ_p
- Alter tunneling transmission

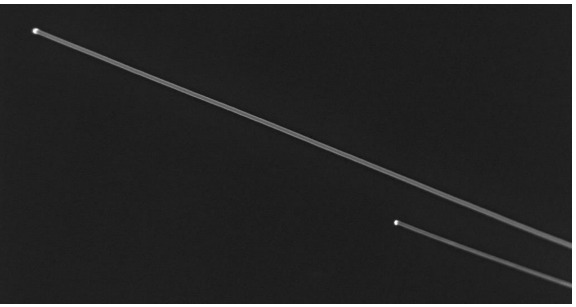
$$T_{n,p}(WKB) \propto e^{\frac{-4w\sqrt{2m^*_{n,p}}\phi_{n,p}^{3/2}}{3q\hbar V}}$$

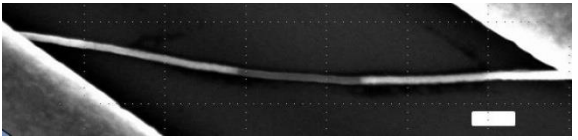


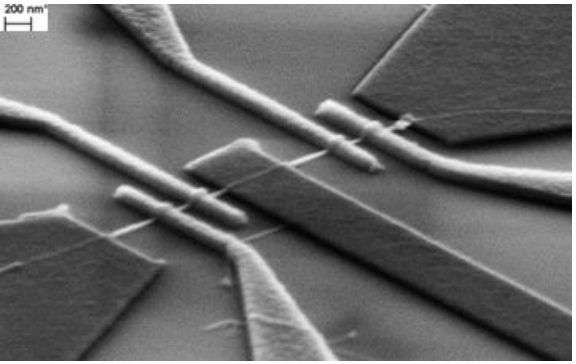
- Alter barrier width *w* (electrost. *geom*, d_{Si}, d_{ox}, κ)
- Replace channel material m^*, $\varphi_{p,n}$, E_g

- Ge with NiGe contacts, boost I_{on} without degrading I_{off}

Summary







Formation of metal / silicon nanowire heterostructures

- Formation of single crystal $NiSi_2$
- Sharp silicide to Si interface

Transport properties

- *carrier type* injected controlled by point potential

Reconfigurable electronics

- *p*- and *n*- type behavior on the same devices
- No doping required

Issues with SBFETs adressed:

- ✓ High variability (varying junction areas)
- ✓ Low drive currents (tunnel barrier in on-state)
- ✓ Degraded off – state > *ambipolarity removed*
- ✓ Exponential turn-on in output characteristics

DFG Deutsche Forschungsgemeinschaft
Project ReproNano &
Cluster of Excellence : cfAED

sachsen.de
SAB: basic funding