Layout Technique for Double-Gate Silicon Nanowire FET with an Efficient Sea-of-Tiles Architecture

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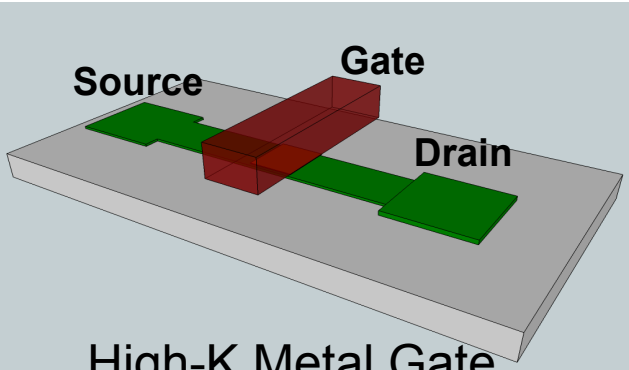
ÉCOLE POLYTECHNIQUE
FÉDÉRALE DE LAUSANNE

INTEGRATED SYSTEMS LABORATORY LSI

Functionally Enhanced Device

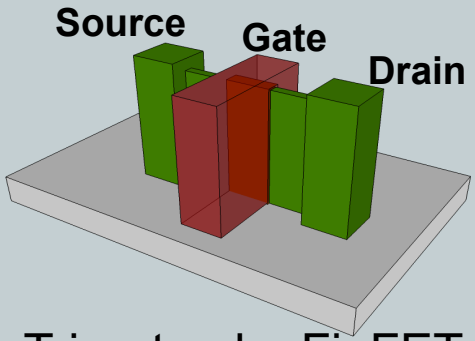
Miniaturisation: More Moore

32nm



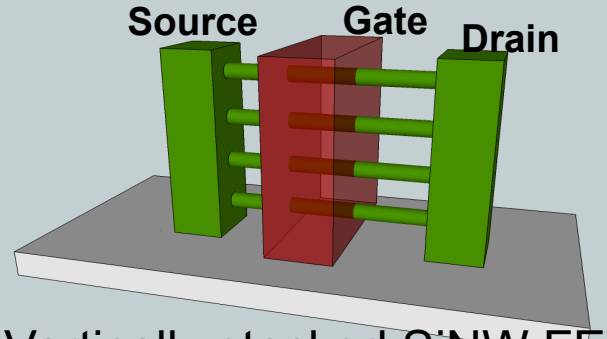
High-K Metal Gate

16nm

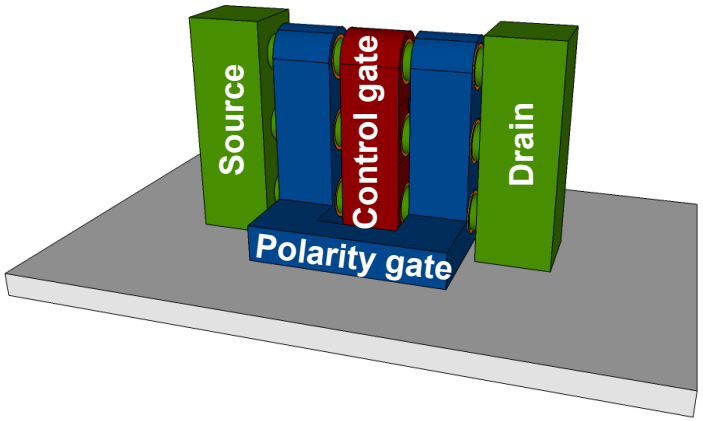


Tri-gate aka FinFET

10nm

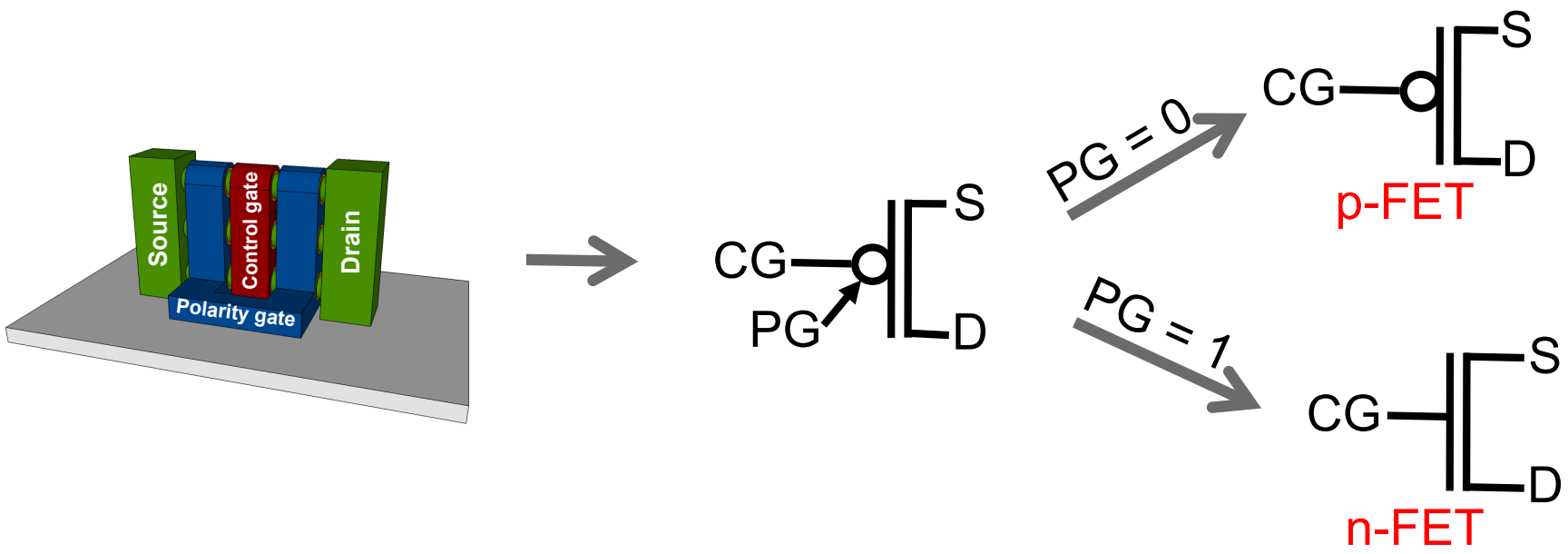


Vertically stacked SiNW FET



Enhanced Functionality

Double-gate Silicon Nanowire FET

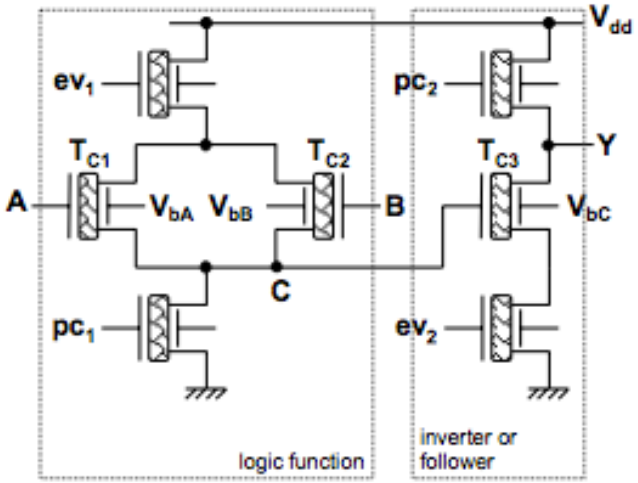


- Dynamic control on the polarity of the device
- Promising feature for future reconfigurable circuits
- Ambipolar logic circuits

Ambipolar Logic Circuits

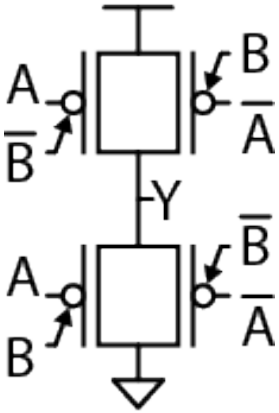
- Circuits based on double gate ambipolar transistors with controllable polarity (CNFET, SiNW FET, Graphene, …)
- Optimal for XOR and XNOR dominated circuits

CNT-DR8F



O'Connor, ICECS 07

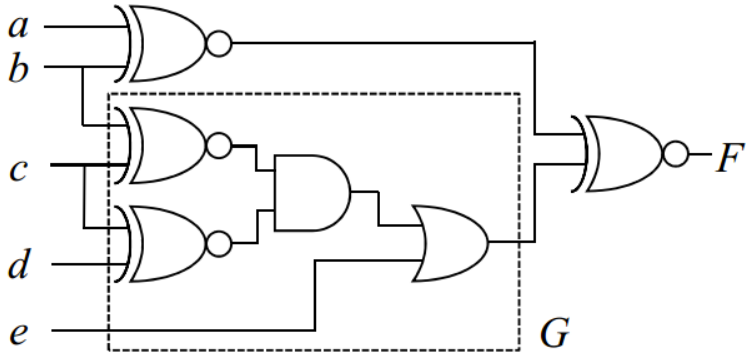
XOR2



Only 4 transistors

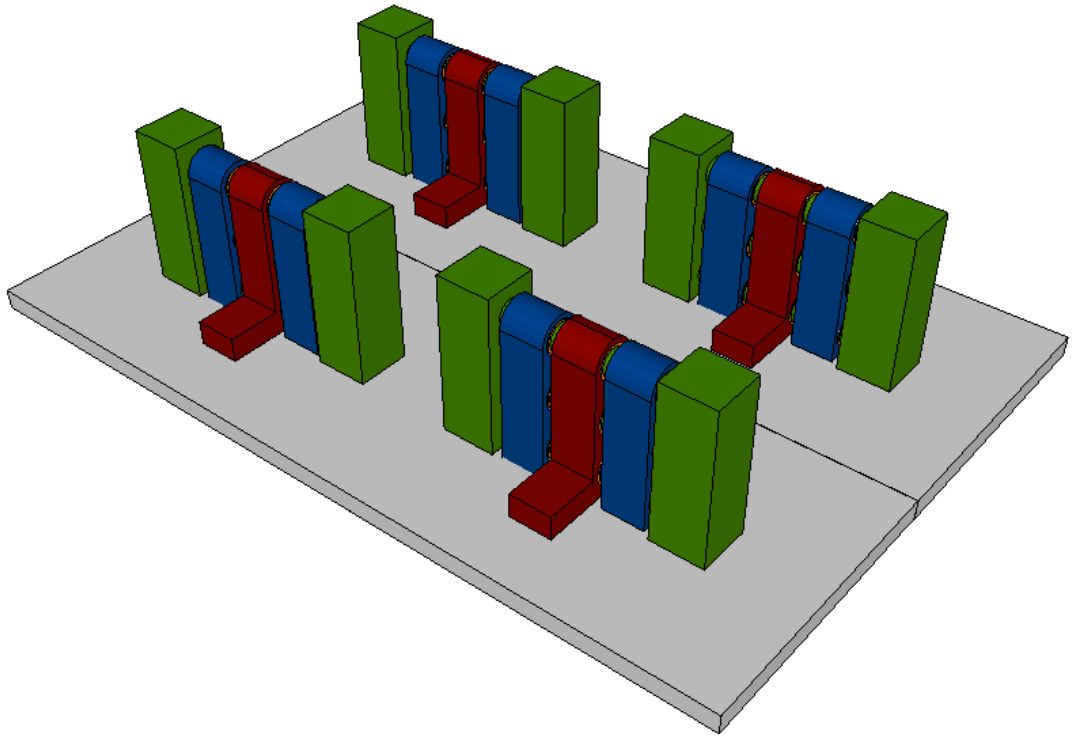
M-H. Ben Jamaa, PhD Thesis

ULM (5,3)



K. Mohanram, DAC 12

Motivation

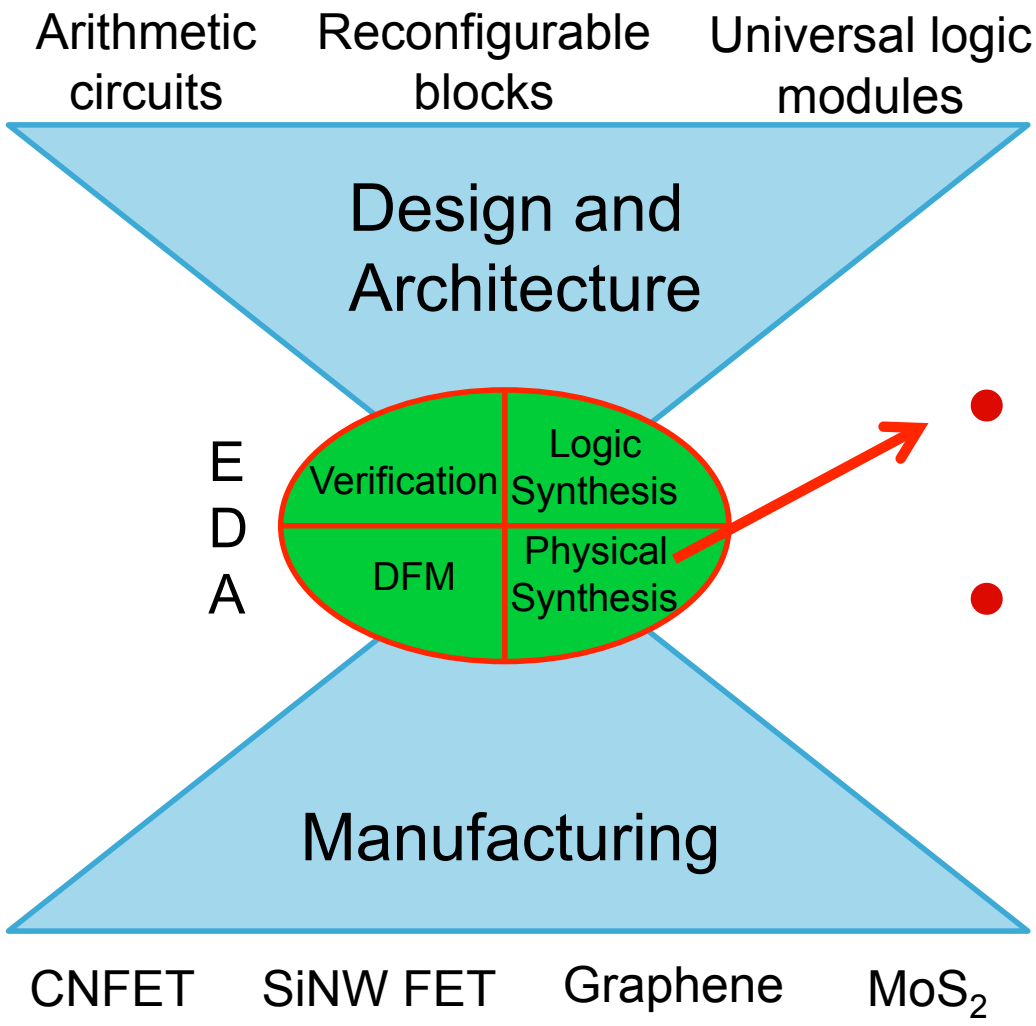


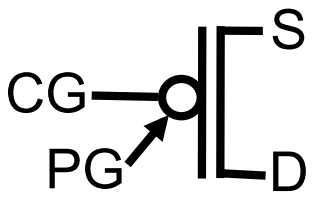
XOR2 ??

Fewer transistors for XOR operation

Every transistor has two gates to route

Physical Design Challenges





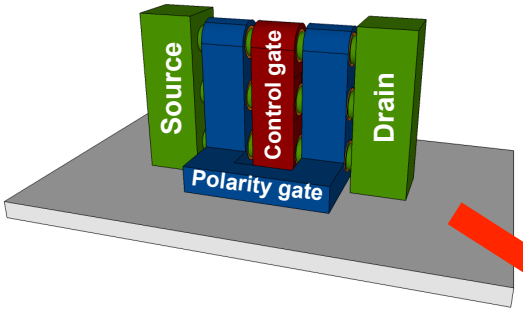
- Can we use existing layout techniques?
- Logic bricks for improved Yield

Outline

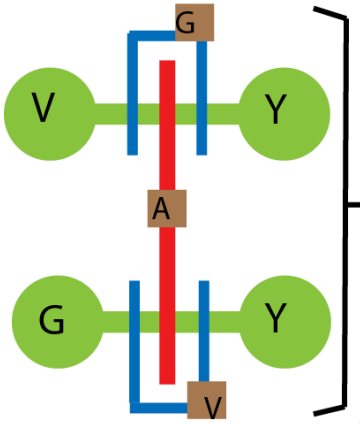
- Introduction
- Layout Technique for DG-SiNW FET
  - Motivation
  - Layout algorithm for XOR embedded Boolean functions
- Sea-of-Tiles
- Simulation Results
- Conclusion

Symbolic layouts : Dumbell-stick diagrams

- Need for new symbolic layouts for ambipolar circuits

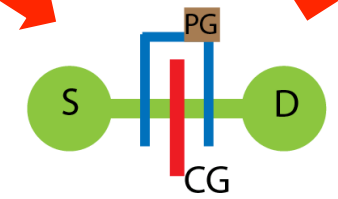


Transistor pairing



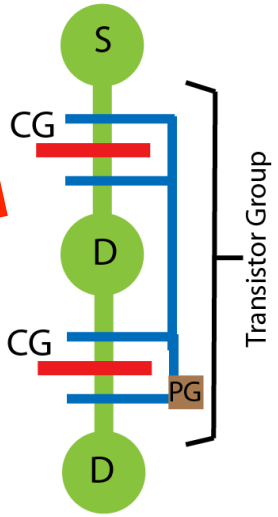
Transistor pair

Control gates connected together



Dumbell-stick

Transistor grouping



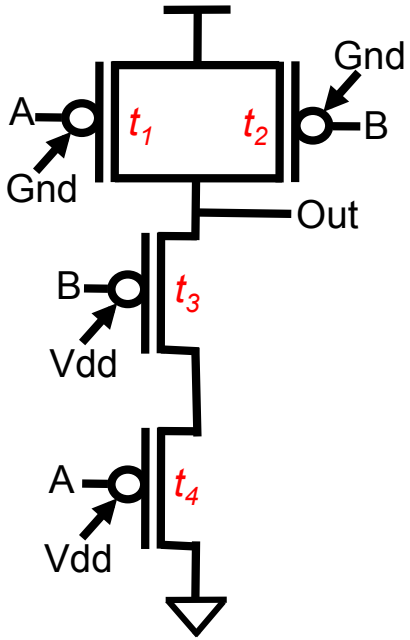
Transistor Group

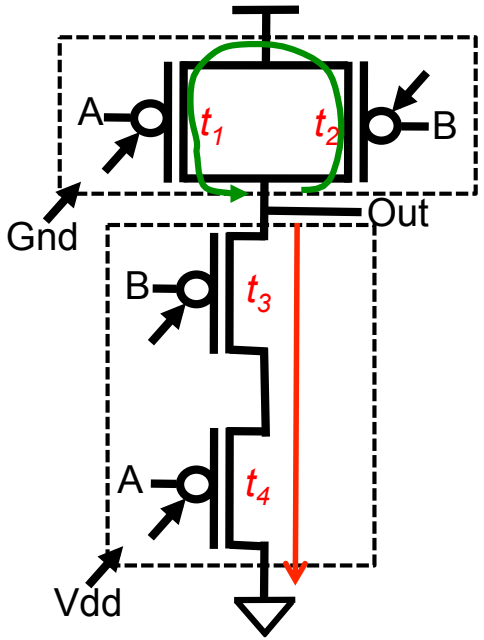
Polarity gates connected together

Layout technique for *Unate* logic functions

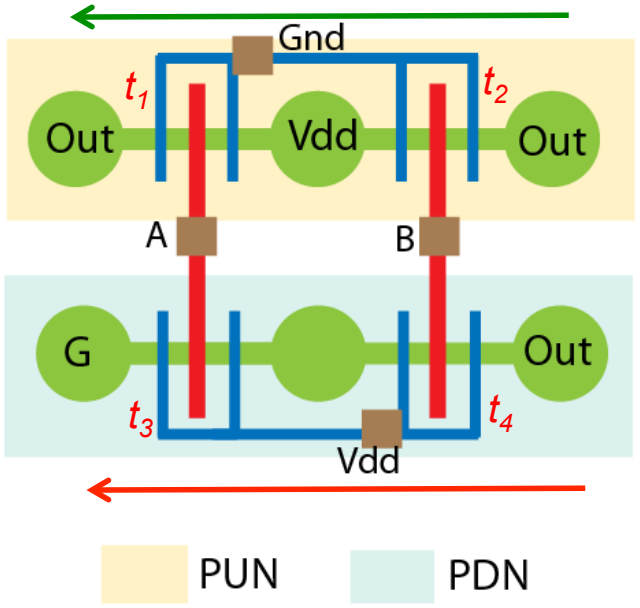
- Negative Unate functions: NAND, NOR, AOI, OAI
- Polarity gates are biased to either *Vdd* or *Gnd*

2-input NAND gate



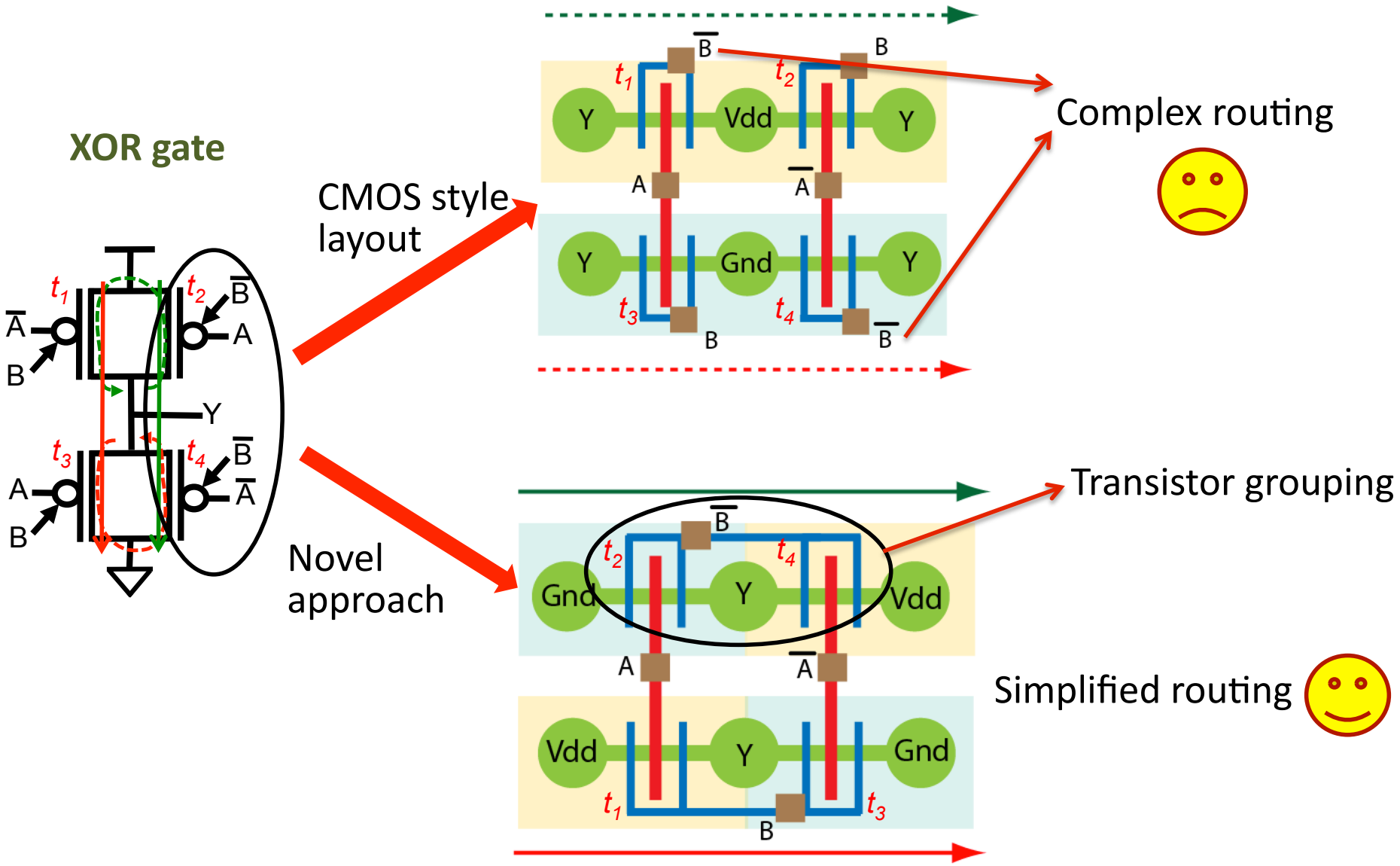


Only one polarity gate for PUN and PDN



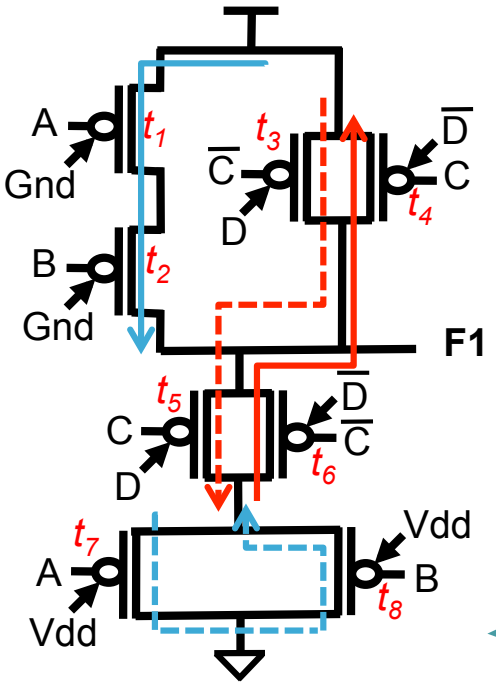
Dumbell-stick diagram

Layout technique for *Binate* logic functions



Complex gates with embedded XOR/XNOR

$$F1 = \overline{(A+B)(C \oplus D)}$$



a) Transistor grouping

b) Transistor pairing

c) Transistor ordering

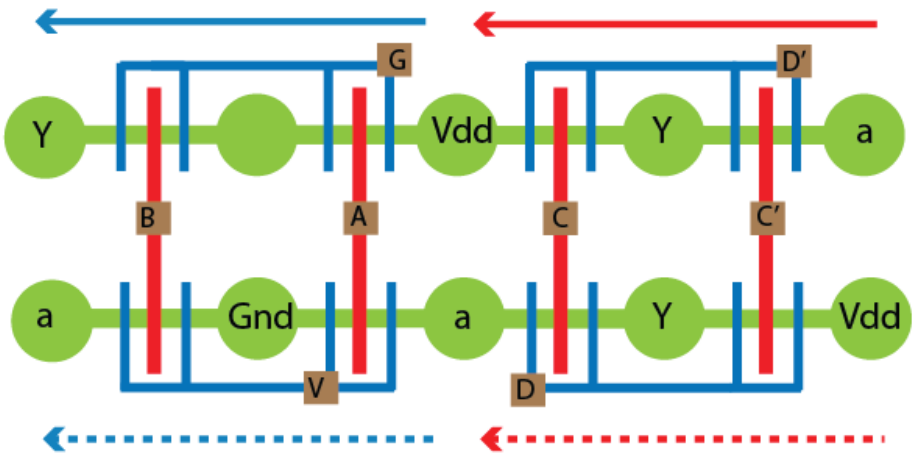
d) Transistor chaining

group D : {t_3, t_5}

group $\overline{D}$: {t_4, t_6}

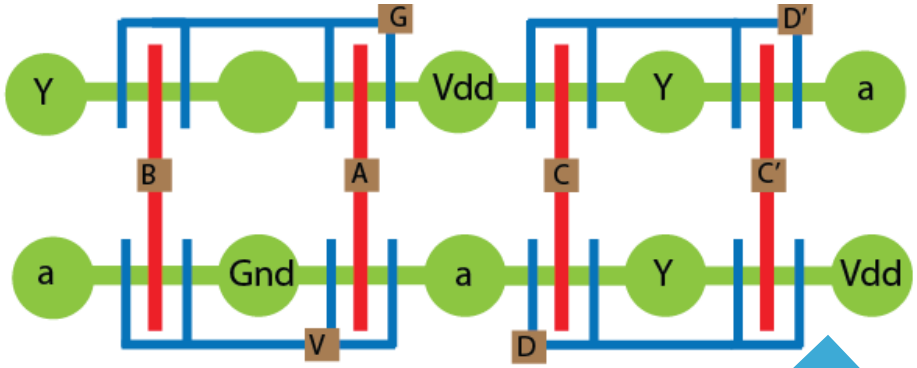
group Vdd : {t_7, t_8}

group Gnd : {t_1, t_2}



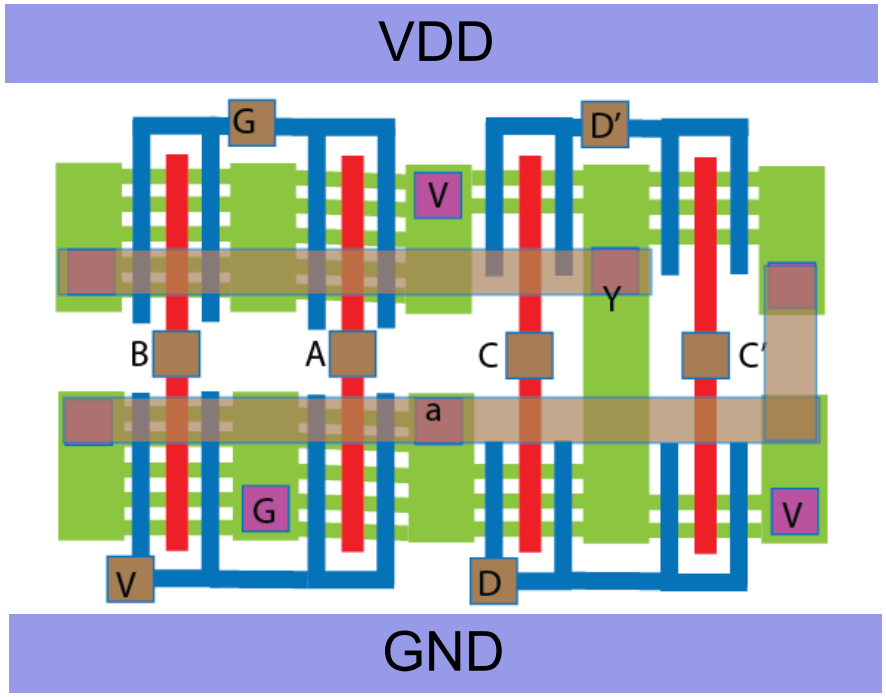
Dumbell-stick diagram

Layout Extraction



Dumbell-stick diagram

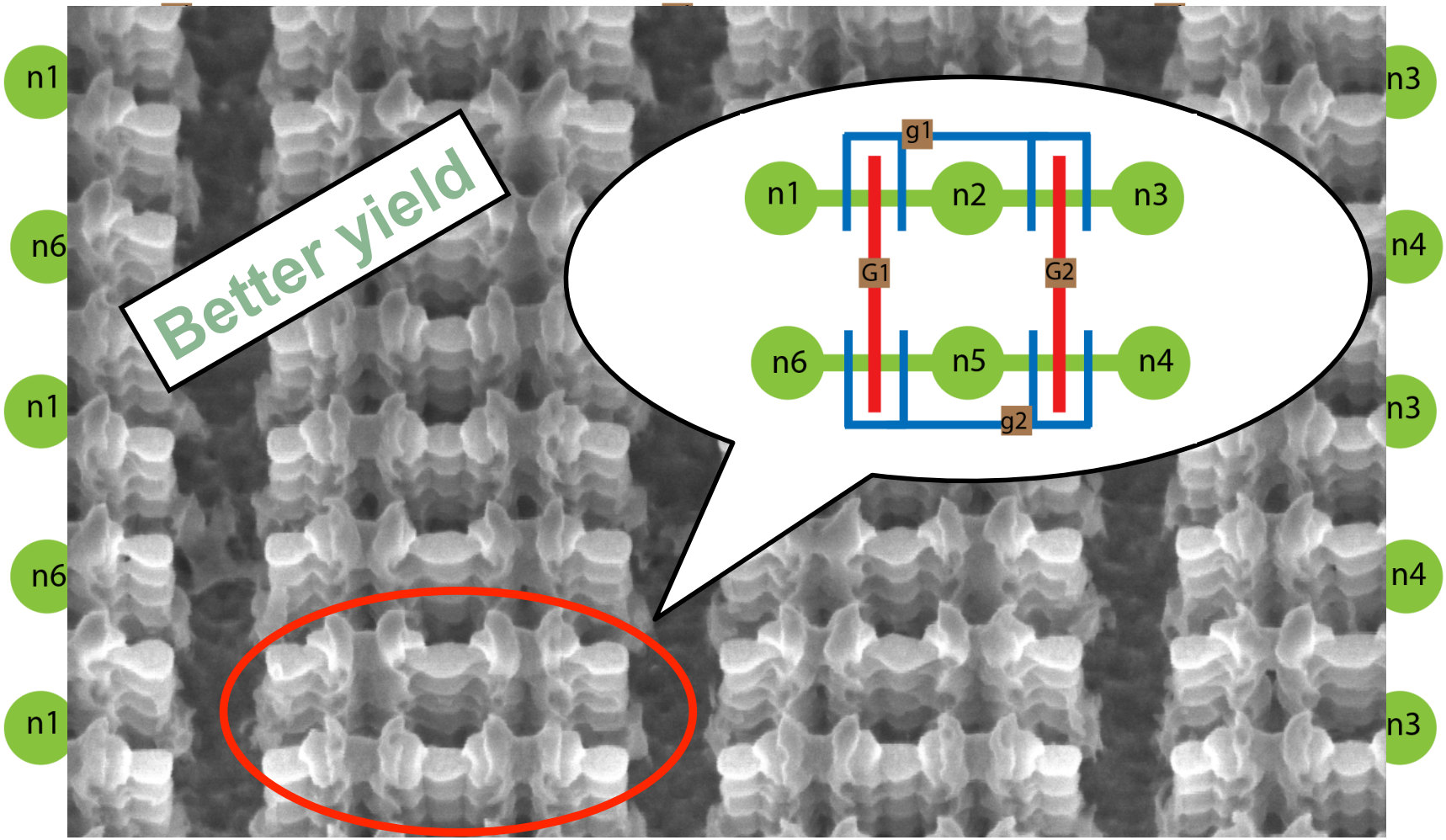
Transistor sizing + Layout generation



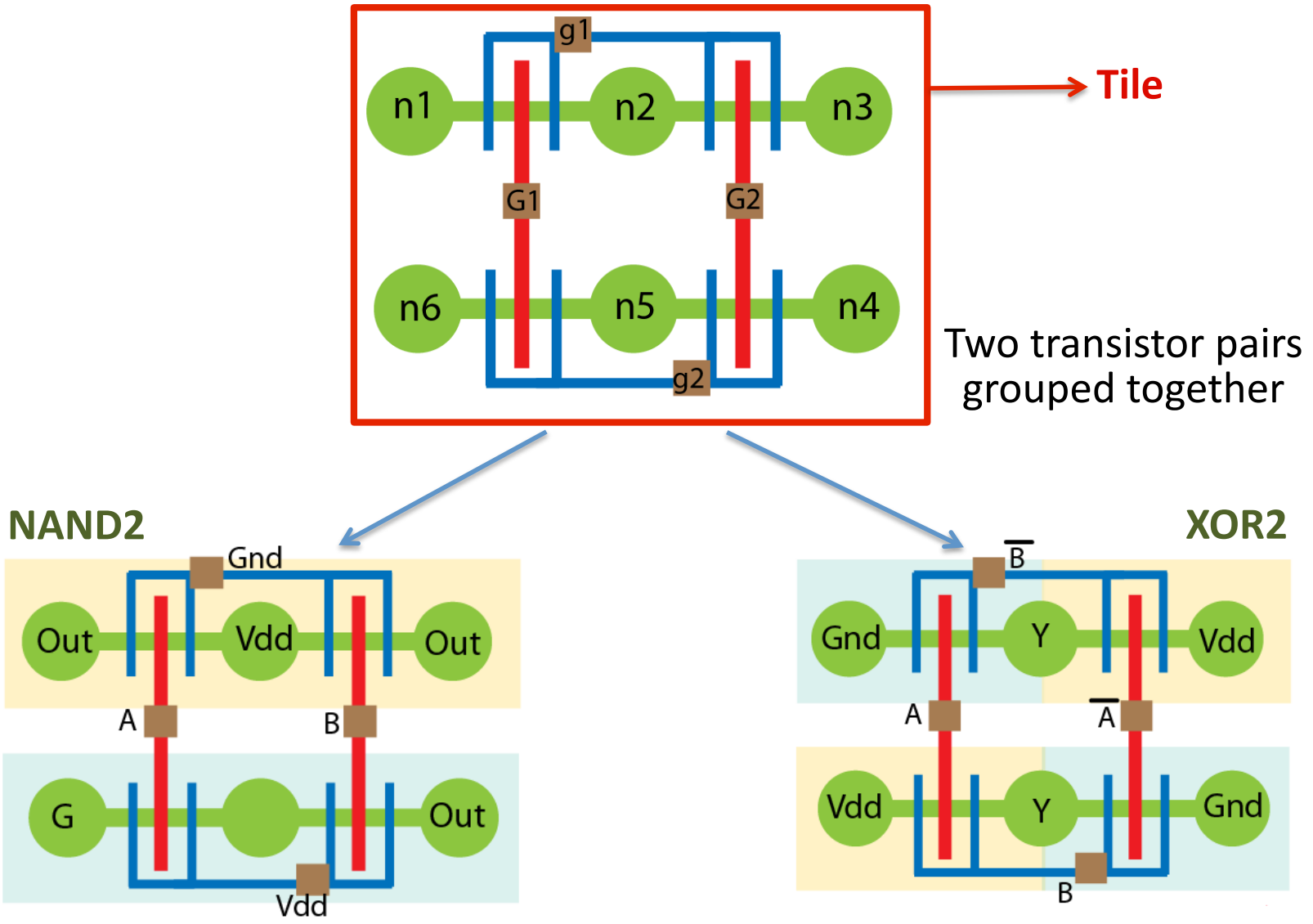
Outline

- Introduction
- Layout Technique for DG-SiNW FET
- Sea-of-Tiles
  - Tiles as basic blocks
  - Optimal Tile
  - Power distribution for SoT
- Simulation Results
- Conclusion

Sea-of-Tiles (SoT)

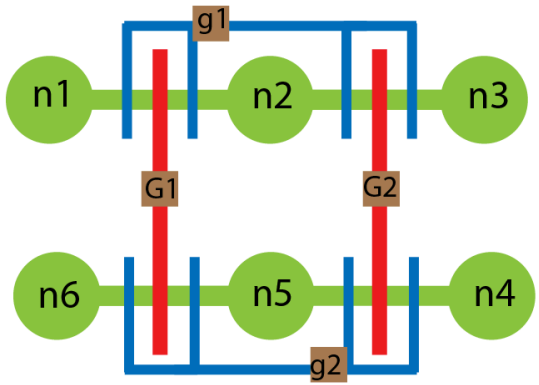


Layout regularity with *Tiles*



Sea-of-Tiles (SoT)

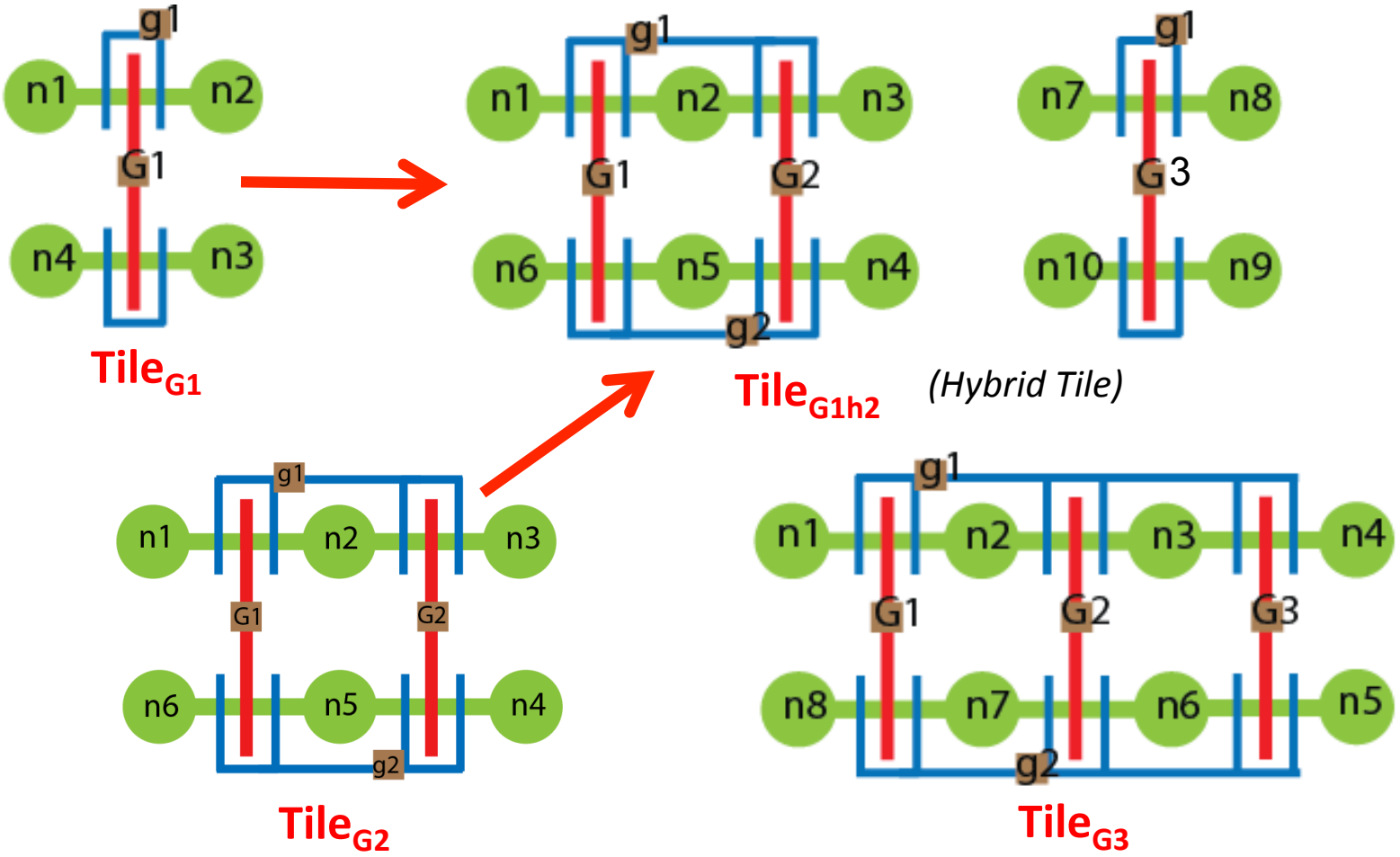
- Gate to Tile mapping



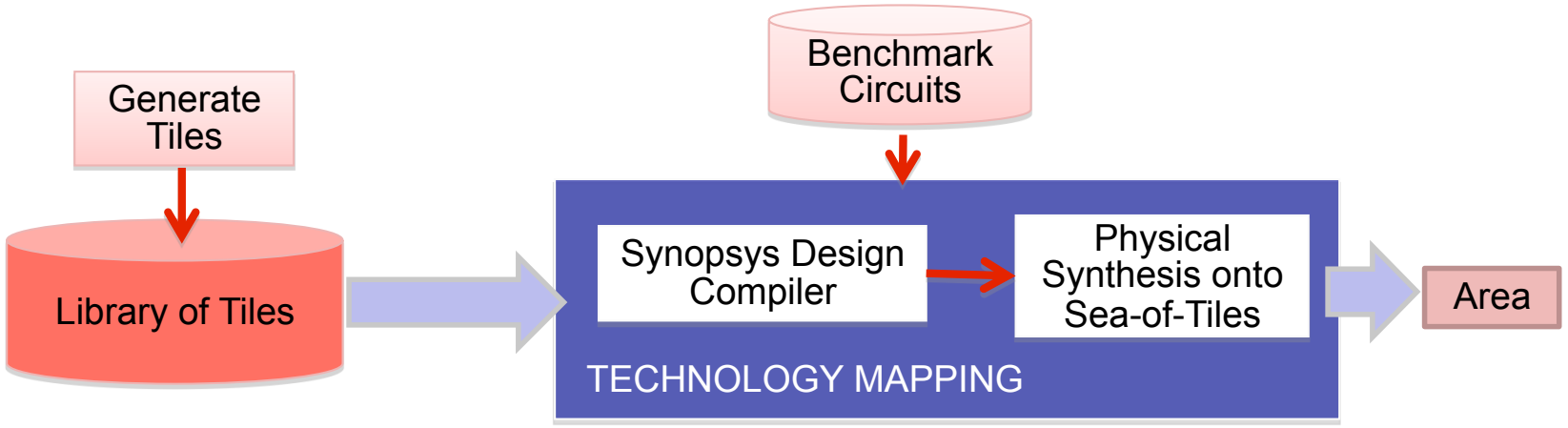
Gates	n1	n2	n3	n4	n5	n6	G1	G2	g1	g2
Xor2	Gnd	Out	Vdd	Gnd	Out	Vdd	A	A’	B’	B
Xnor2	Gnd	Out	Vdd	Gnd	Out	Vdd	A	A’	B	B’
Nand2	Out	Vdd	Out	Out	-	Gnd	A	B	Gnd	Vdd
Nor2	Vdd	-	Out	Out	Gnd	Out	A	B	Gnd	Vdd
Inv2X	Vdd	Out	Vdd	Gnd	Out	Gnd	A	A	Gnd	Vdd
Buf	O1	Vdd	O2	O2	Gnd	O1	A	O1	Gnd	Vdd

Various logic *Tiles* as basic building blocks

- What is the Optimal Tile?



Design flow for determining the Optimal Tile



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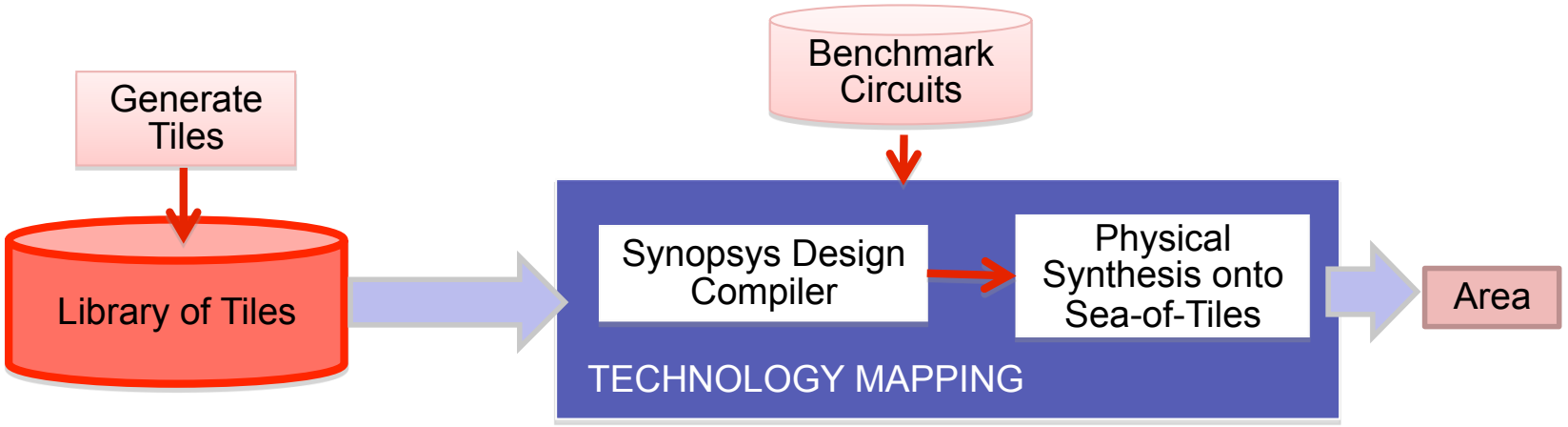
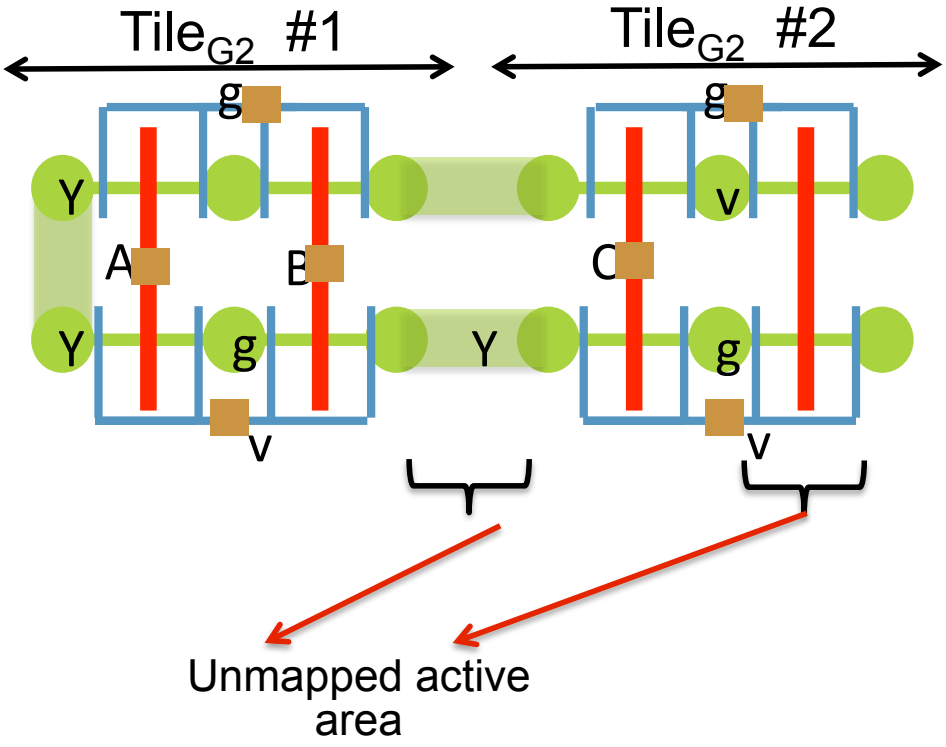
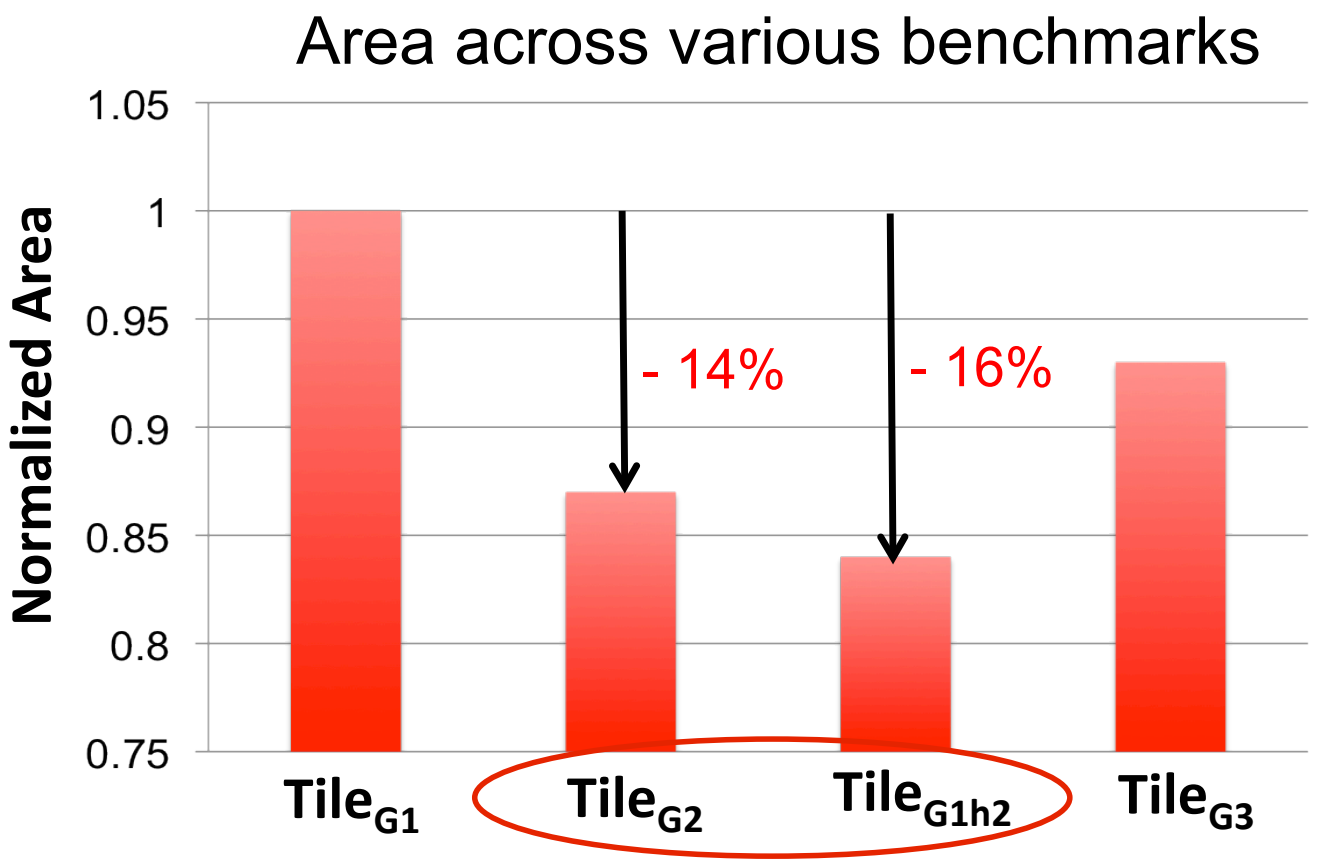


Gates	$Tile_{G1}$		$Tile_{G2}$		$Tile_{G1h2}$		$Tile_{G3}$	
	#N	#UF	#N	#UF	#N	#UF	#N	#UF
AND2	3	0.6	2	0.6	1	0.75	1	1
AND3	4	0.57	2	0.8	1.38	0.67	2	0.57
AOI21	3	0.6	2	0.6	1	0.75	1	1
AOI221	5	0.56	3	0.625	1.62	0.71	2	0.71
AOI222	6	0.54	3	0.75	2	0.67	2	0.86
AOI22	4	0.57	2	0.8	1.38	0.67	2	0.57
AOI321	6	0.54	3	0.75	2	0.67	2	0.86
BUF	2	0.66	1	1	0.62	1	1	0.67
INV	1	0.66	1	1	0.38	1	1	0.67
NAND2	2	0.66	1	1	0.62	1	1	0.67
NAND3	3	0.6	2	0.6	1	0.75	1	1
NAND4	4	0.57	2	0.8	1.38	0.67	2	0.57
NOR2	2	0.66	1	1	0.62	1	1	0.67
NOR3	3	0.6	2	0.6	1	0.75	1	1
NOR4	4	0.57	2	0.8	1.38	0.67	2	0.57
OAI21	3	0.6	2	0.6	1	0.75	1	1
OAI22	4	0.57	2	0.8	1.38	0.67	2	0.57
OR2	3	0.6	2	0.6	1	0.75	1	1
OR3	4	0.57	2	0.8	1.38	0.67	2	0.57
XNOR2	8	0.57	2	0.8	1.38	0.67	2	0.57
XNOR3	9	0.56	3	0.625	1.62	0.71	2	0.71
XOR2	8	0.57	2	0.8	1.38	0.67	2	0.57
XOR3	9	0.56	3	0.625	1.62	0.71	2	0.71

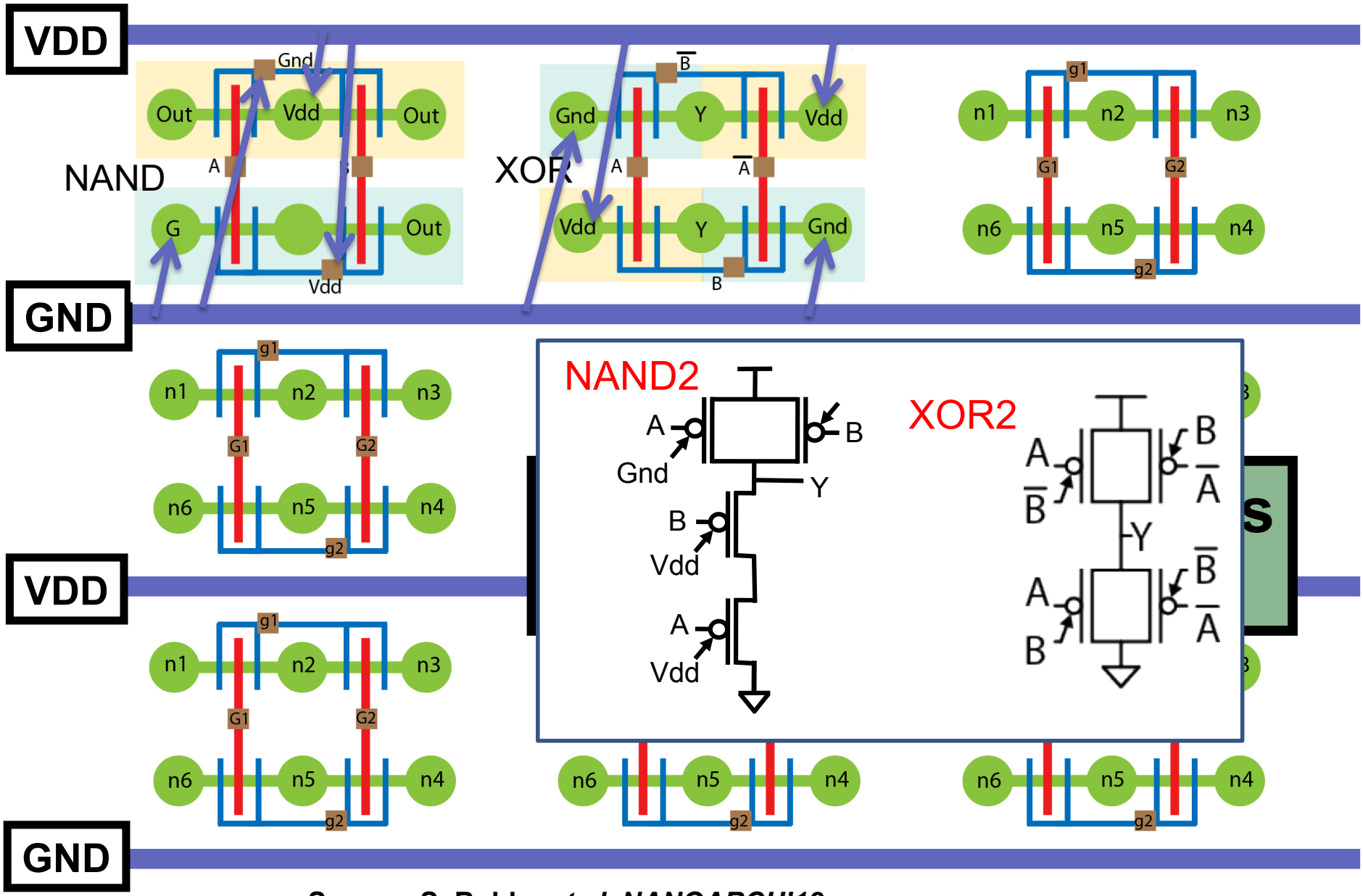


Result: Impact on Area



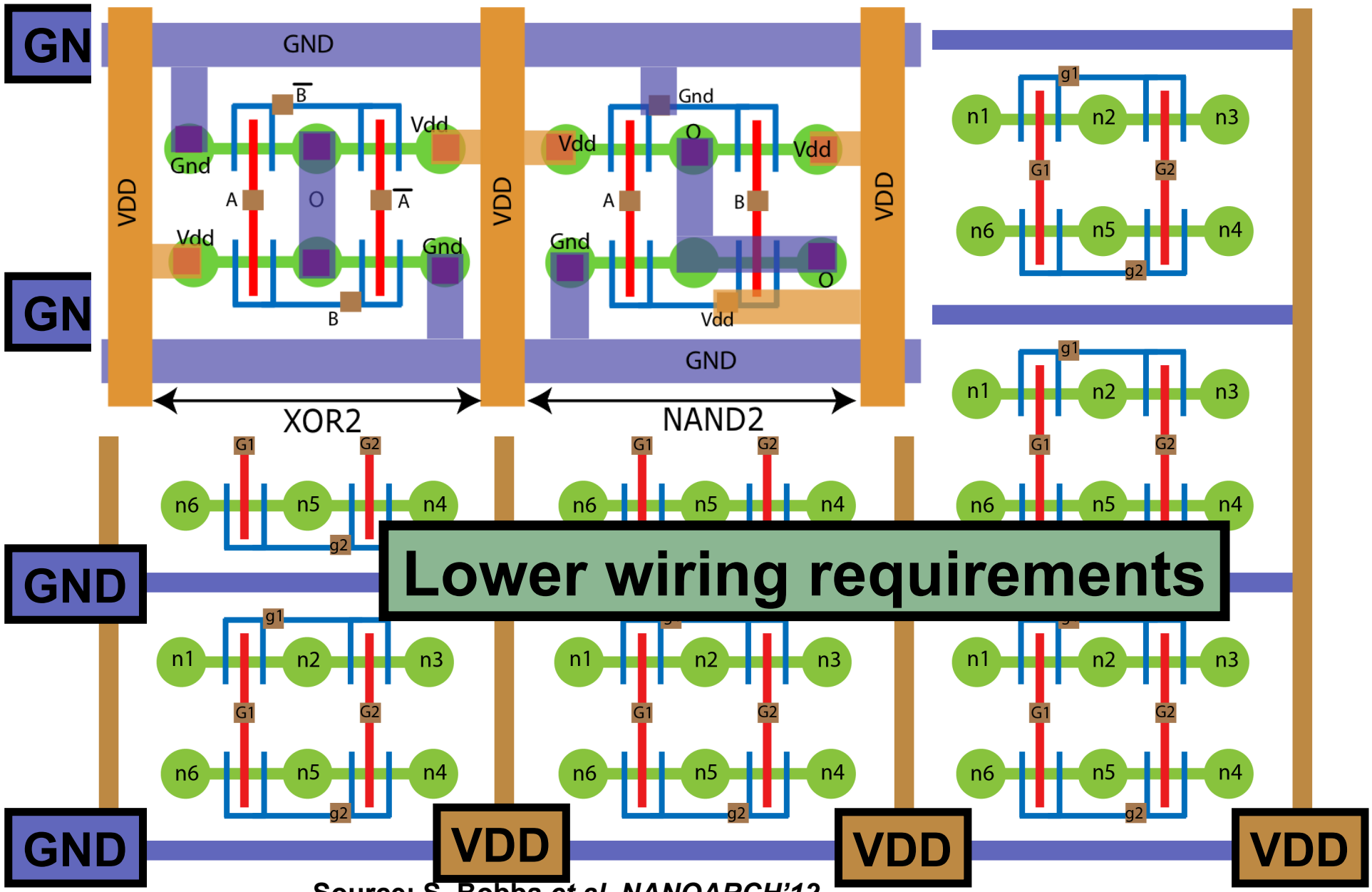
- Tile$_{G2}$ and Tile$_{G1h2}$ optimal for mapping logic gates, with respect to reduced routing complexity thereby reducing in the overall active area

Sea-of-Tiles Power Distribution…



Source: S. Bobba *et al*, *NANOARCH'12*

Sea-of-Tiles Power Distribution



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- Layout Technique for DG-SiNW FET
- Sea-of-Tiles
- Simulation Results
  - Arithmetic Circuits
  - Circuit level Benchmarking
- Conclusion

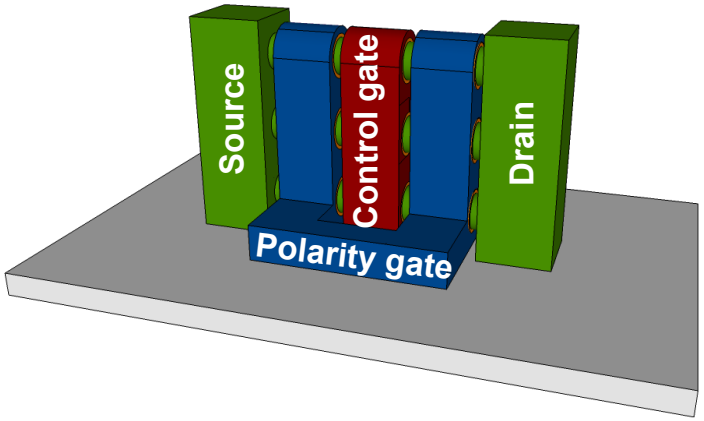
Case study: Arithmetic Circuits

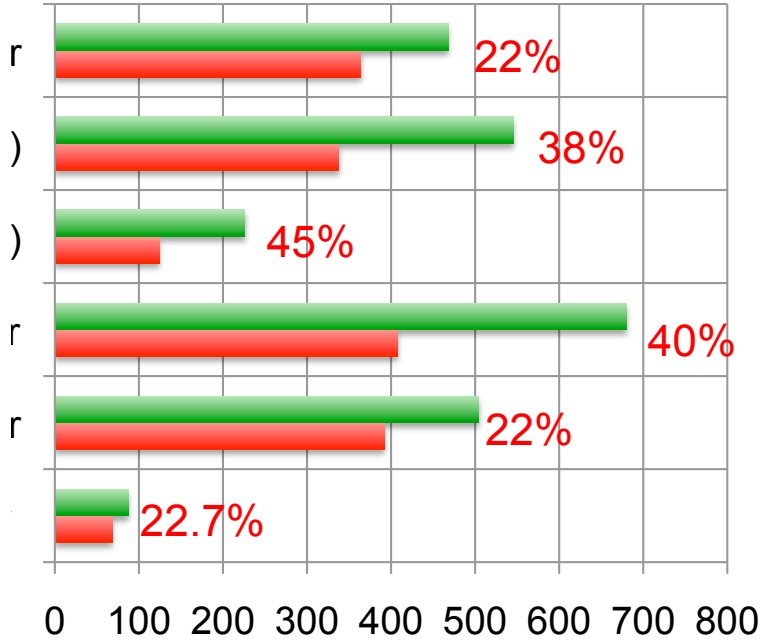
Logic gates	FinFET (ns)	DG-SiNW (ns)		Si-CMOS (ns)
		CG -> Out	PG -> Out	
INV	0.056	0.043	X	0.139
NAND2	0.066	0.05	X	0.148
NOR2	0.062	0.072	X	0.172
XOR2	0.081	0.046	0.108	0.191
XOR3	0.198	0.079	0.11	0.38

Logic Gates (FO4 delay)

Gate	Ambipolar Logic		CMOS logic	
	Area	Delay	Area	Delay
XOR2	8	1	12	1
XOR3	10	1.19	24	2
Half adder	12	1	16	1
Full adder	14	1.19	18	2
4-2 Compressor	26	2	42	4
5-3 Compressor	38	3	64	4

Arithmetic Cell Library





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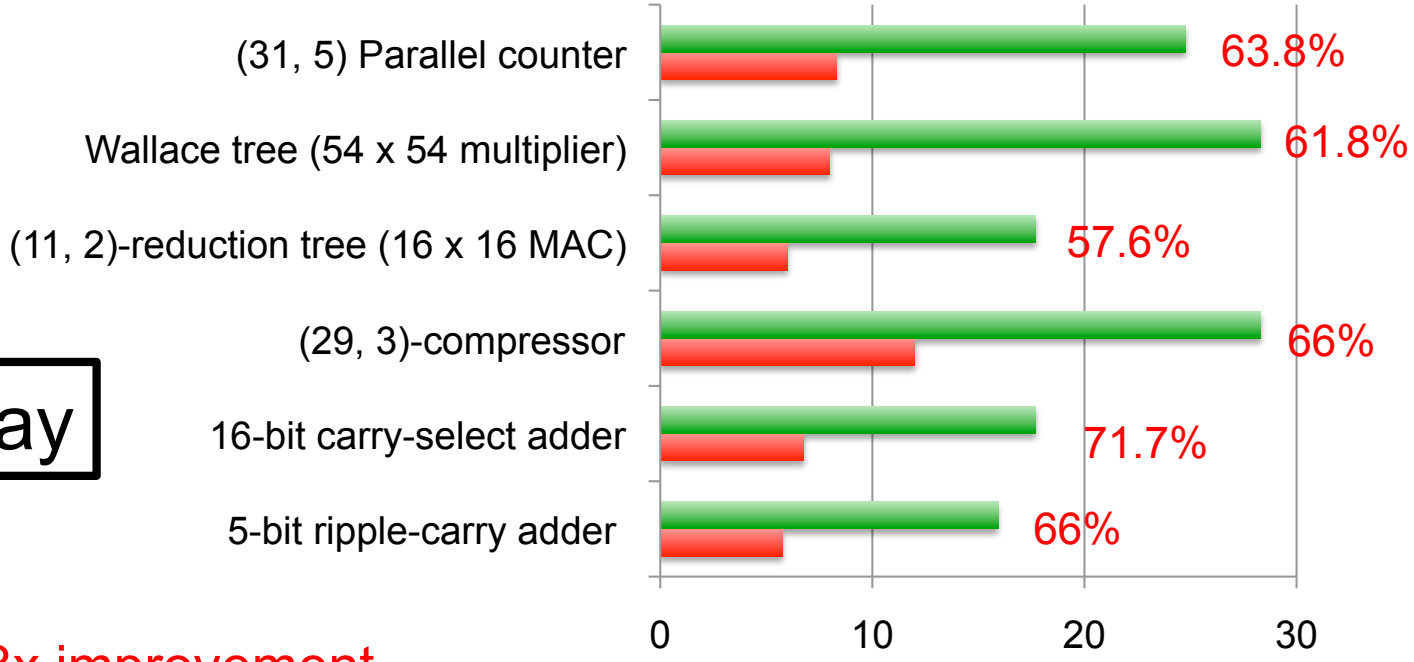
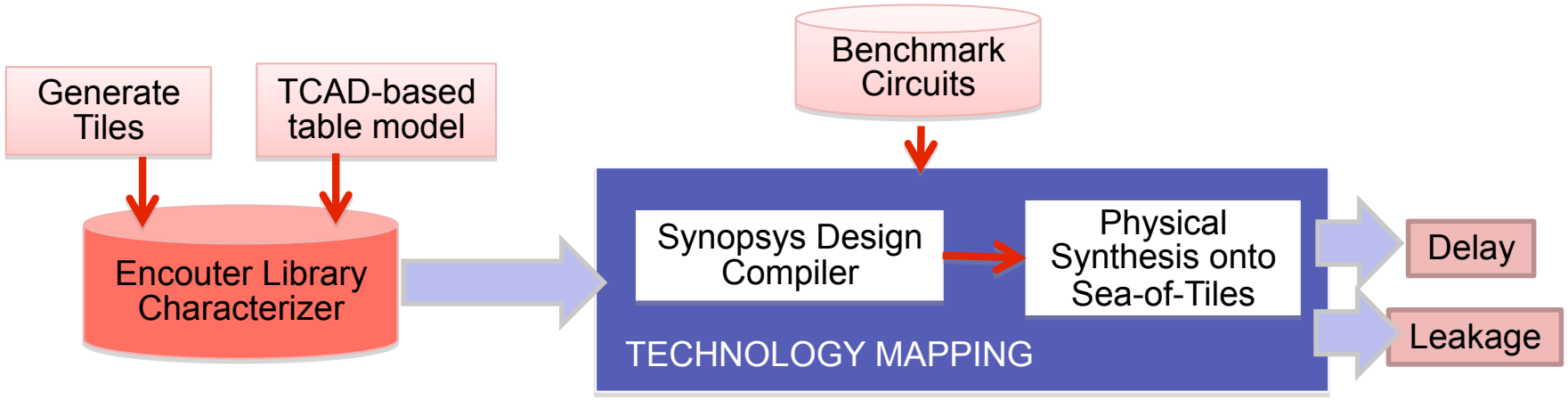
Arithmetic Cell Library

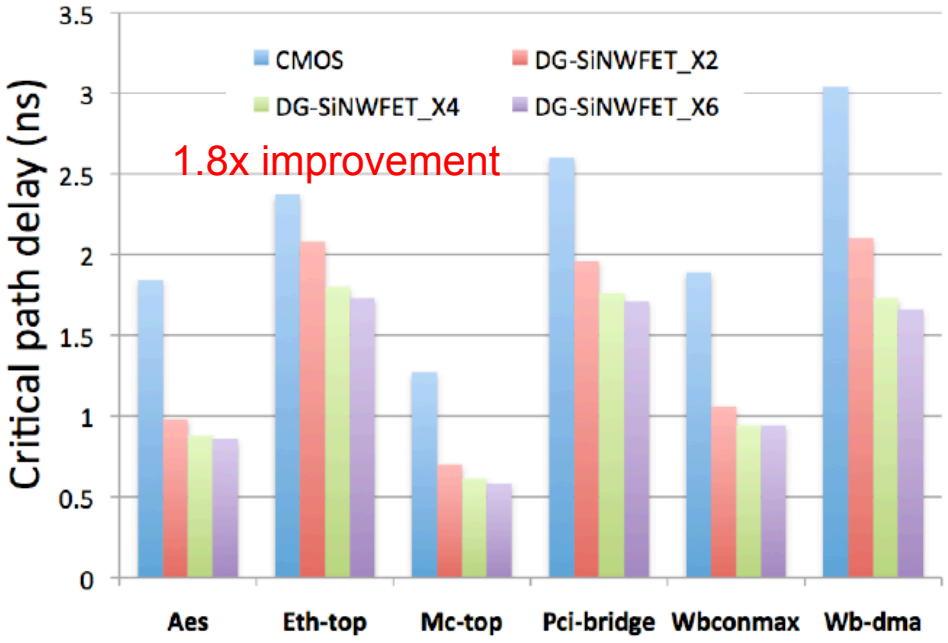
Delay

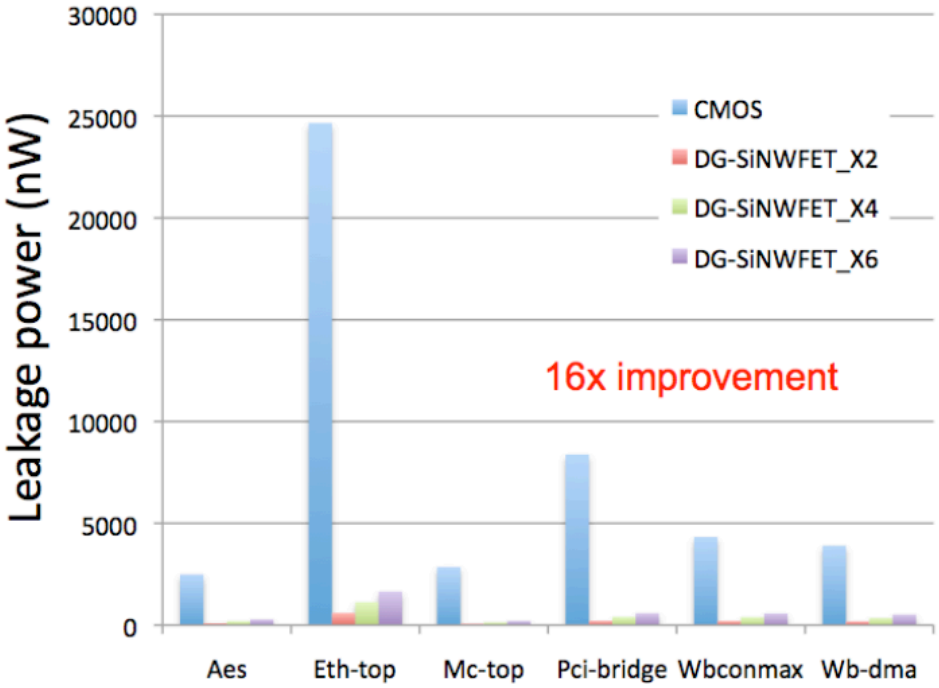


2.8x improvement

Circuit Level Benchmarking







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Conclusion

- Proposed a novel layout methodology and algorithm for Boolean functions with embedded XOR
- Showed an efficient implementation of Ambipolar circuits with Sea-of-Tiles design methodology
  - Area optimal tiles $Tile_{G2}$ and $Tile_{G1h2}$
- Circuit Level Benchmarking
  - Maximum improvement for Arithmetic circuits (2.8x)
  - Reduction in Leakage power (16x)

Thank You