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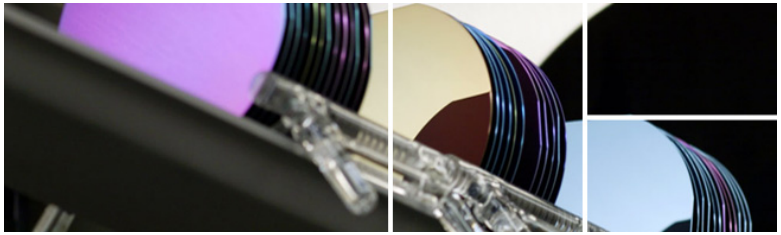

FPGA Design with Double-Gate Carbon Nanotube Transistors

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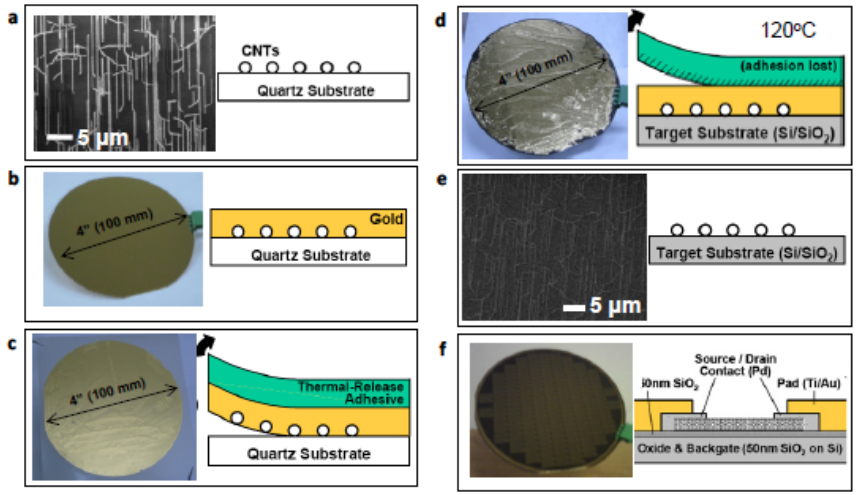
Seminar – Integrated Systems Centre

October 20th, 2011 – EPFL, Switzerland

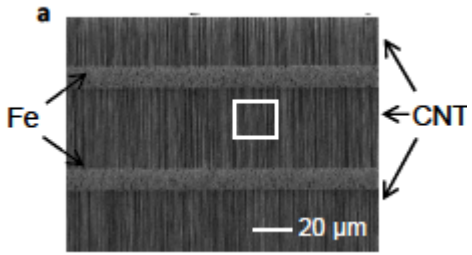
Outline

- Introduction
- Technology and Modeling of DG-CNTFETs
- Fine-Grain Reconfigurable Architecture
- Simulation Results
- Conclusions

Large Scale Directional Carbon Nanotubes

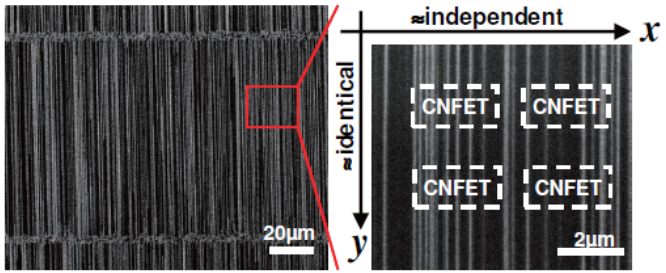


Large scale CNT technology

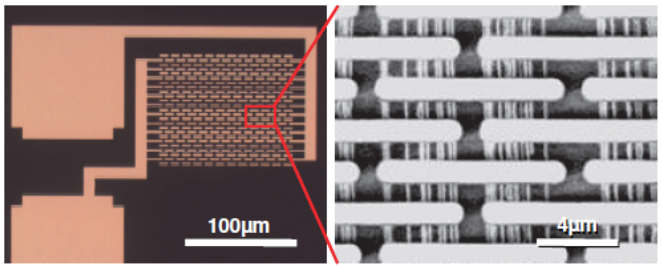


Large scale directional CNT transfer

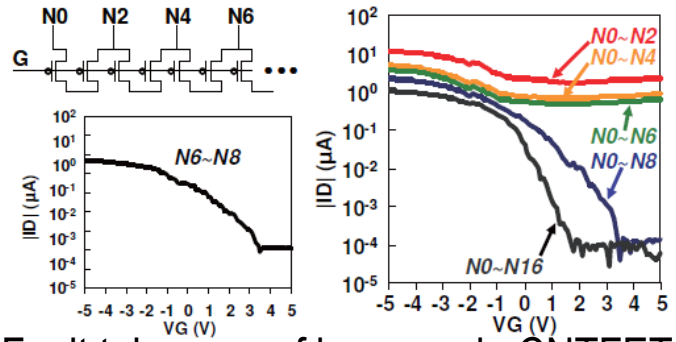
N. Patil et al., Sym. VLSI Tech. '08



Asymetrical Correlation of CNTs



Metallic-CNT-aware CNTFET technique

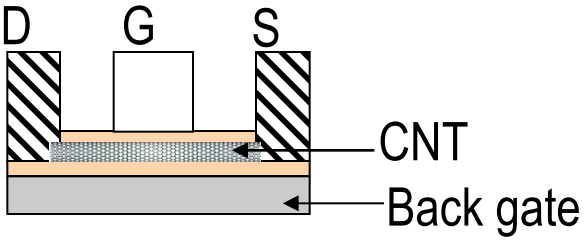


Fault tolerance of large scale CNTFETs

A. Lin et al., Sym. VLSI Tech. '09

Ambipolar CNT Technology

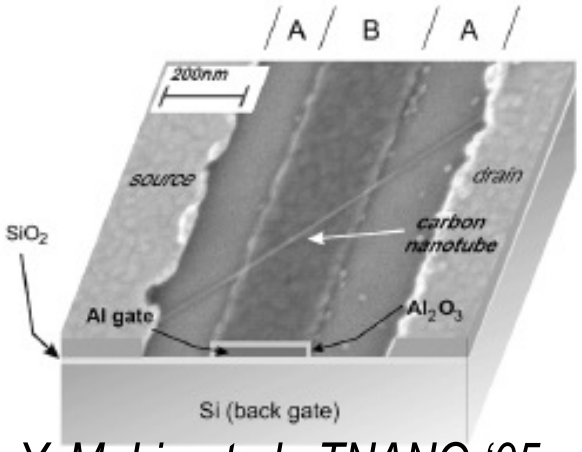
- Ambipolar behavior reported on CNTFETs:
  - Conduction under both low and high gate voltage
- Technology demonstration with:
  - Undoped channel
  - Mid-gap D/S contact metal
- Polarity control with a double gate:
  - Double gate ambipolar CNTFET [Lin et al., TNANO'05]
  - P-type if low bias on back gate
  - N-type if high bias on back gate



- Ultimate goal:
  - Leveraging electrical benefits of CNTFETs: energy-delay-product (EDP) of CNTFET: 13x better vs. CMOS [Deng et al, ISSCC'07]
  - Controlling device operation (n- or p-type) during circuit operation

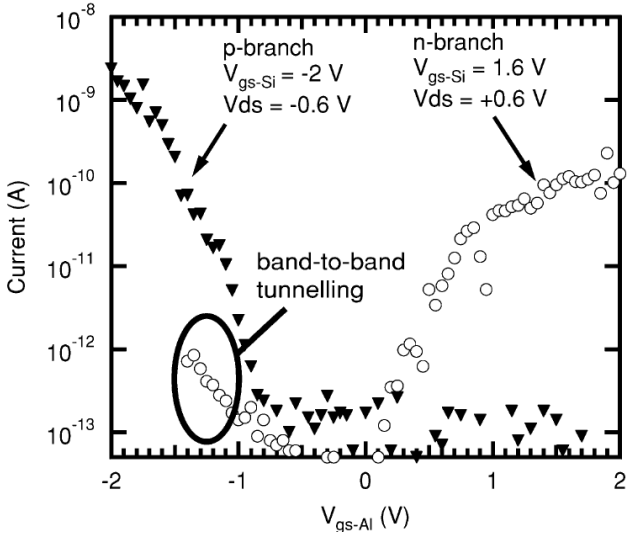
Fabrication of Ambipolar CNTFETs (1/2)

Demonstration of polarity tuning of double-gate carbon nanotube transistors (DG-CNTFET)

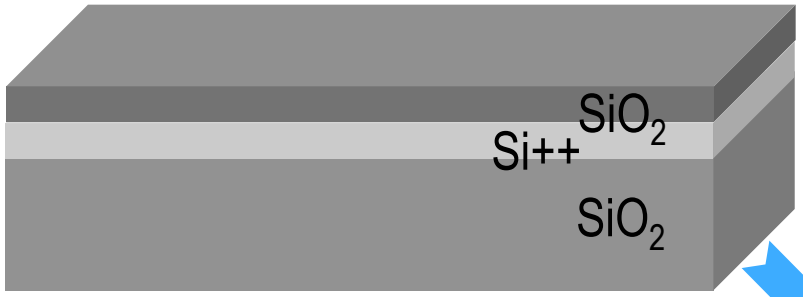


Y.-M. Lin et al., TNANO '05

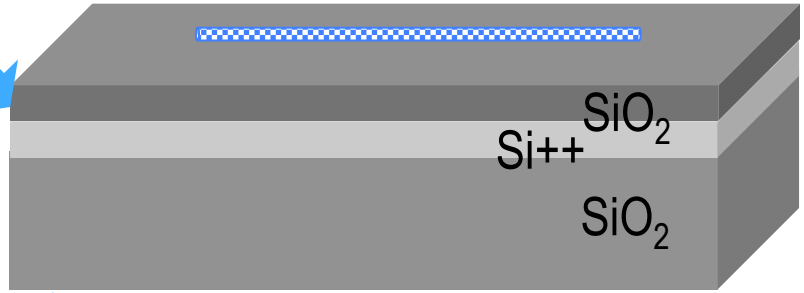
V_{fg}	V_{bg}	state
+V	+V	on (n)
-V	+V	off (n)
+V	-V	off (p)
-V	-V	on (p)
X	0	off (n/p)



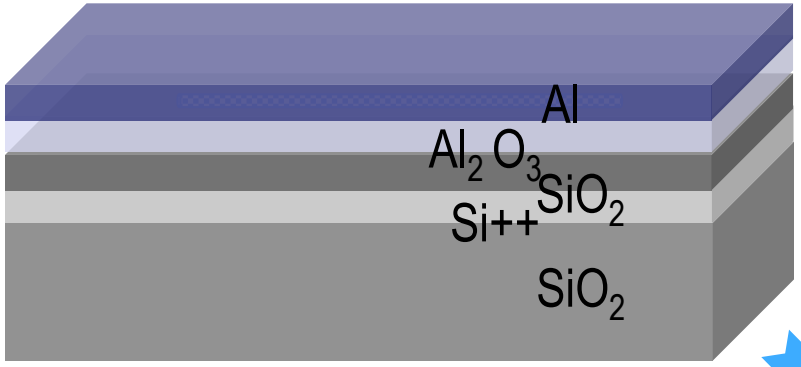
Fabrication of Ambipolar CNTFETs (2/2)



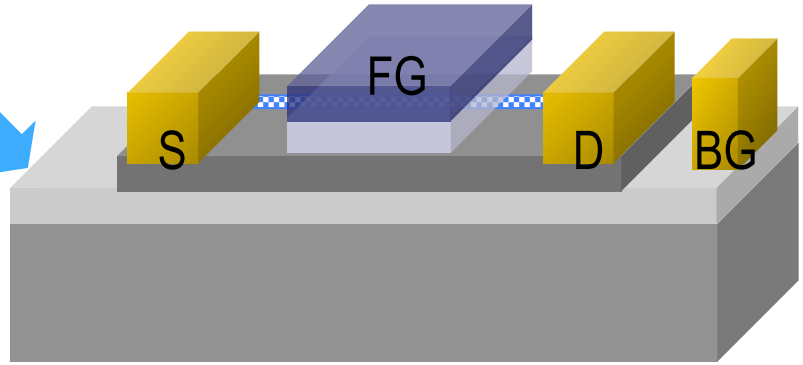
SOI substrate (only BOX and Si visible)
P++ doping of Si
Dry Si oxidation (top SiO_2)



CNT deposition or transfer

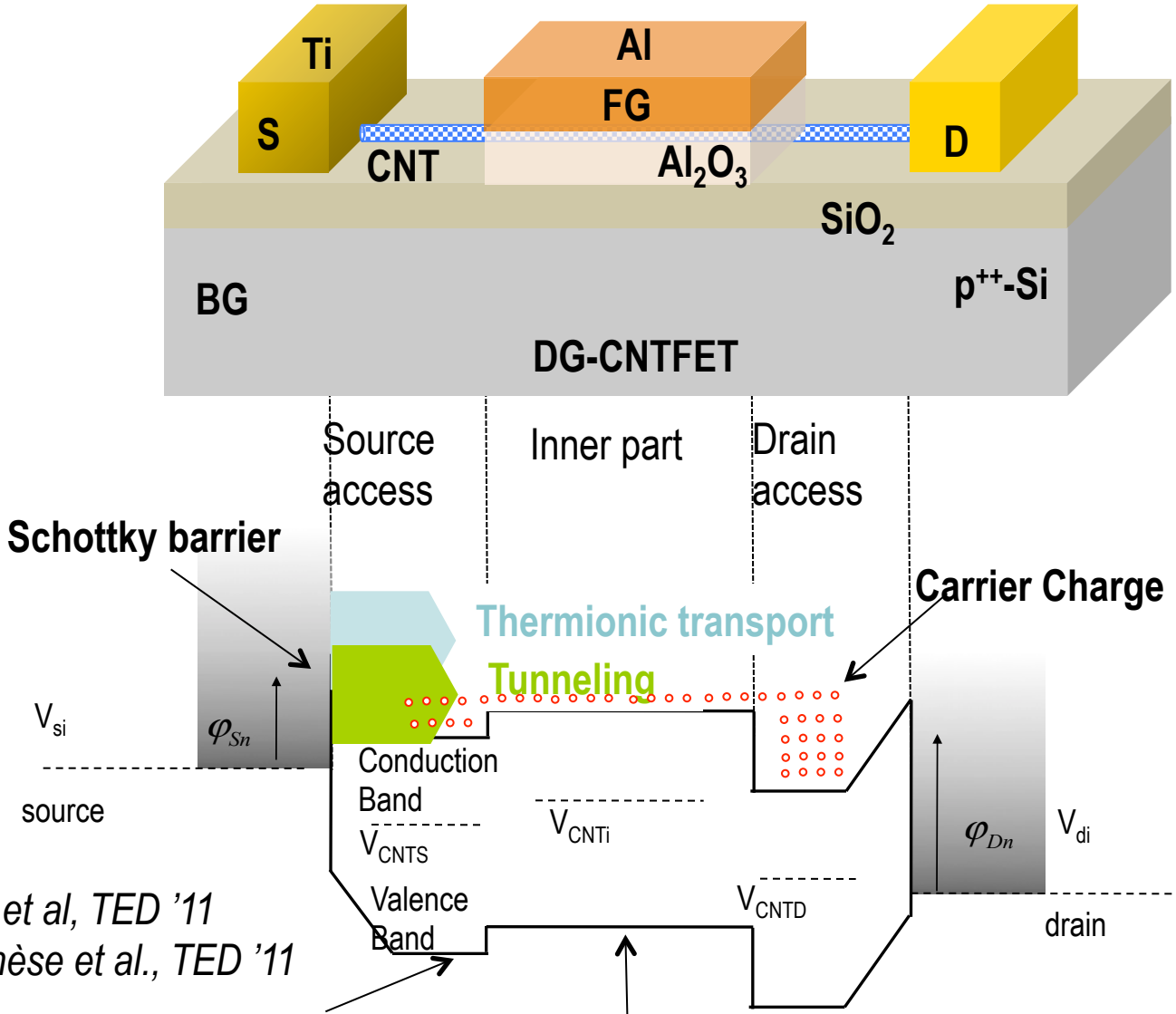


Al_2O_3 (or HfO_2) sputtering
Al sputtering (top gate)



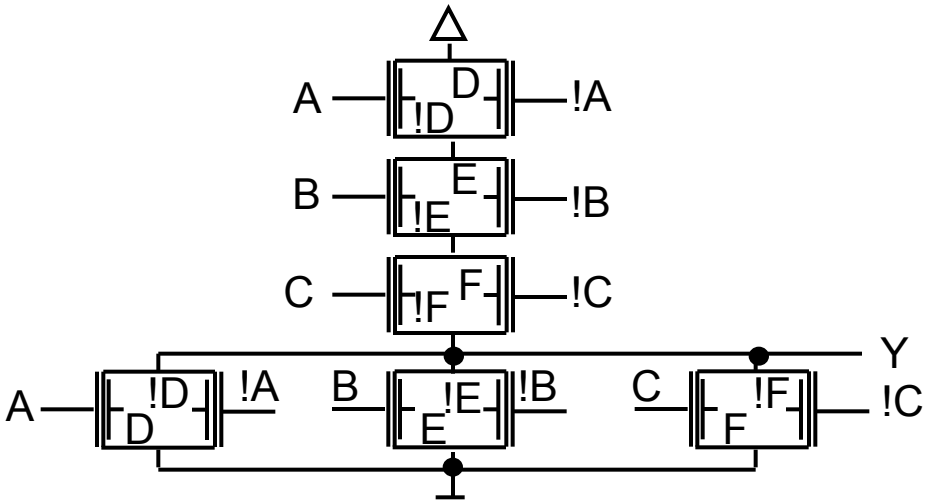
Gate etch
Eventually SiO_2 etch (via opening)
Metallization (eventually different metals)

Double-Gate Channel Control



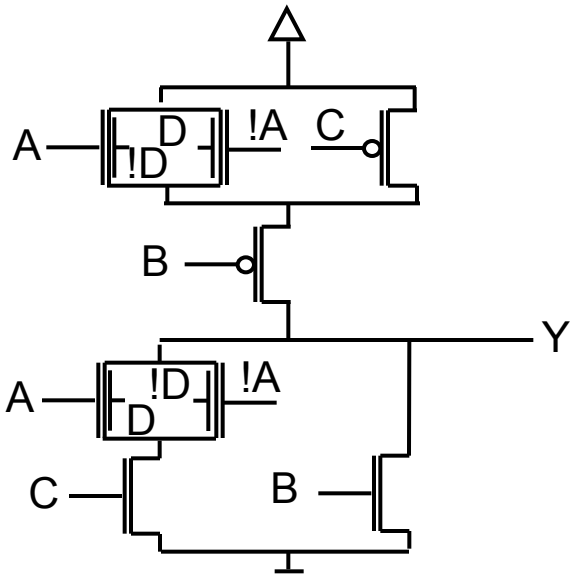
M. Najari et al, TED '11
S. Frégonèse et al., TED '11

Design of Static Ambipolar Logic Gates



$$Y = \overline{A \oplus D + B \oplus E + C \oplus F}$$

GNAND-style structure



$$Y = \overline{(A \oplus D + B) \cdot C}$$

GAOI-style structure

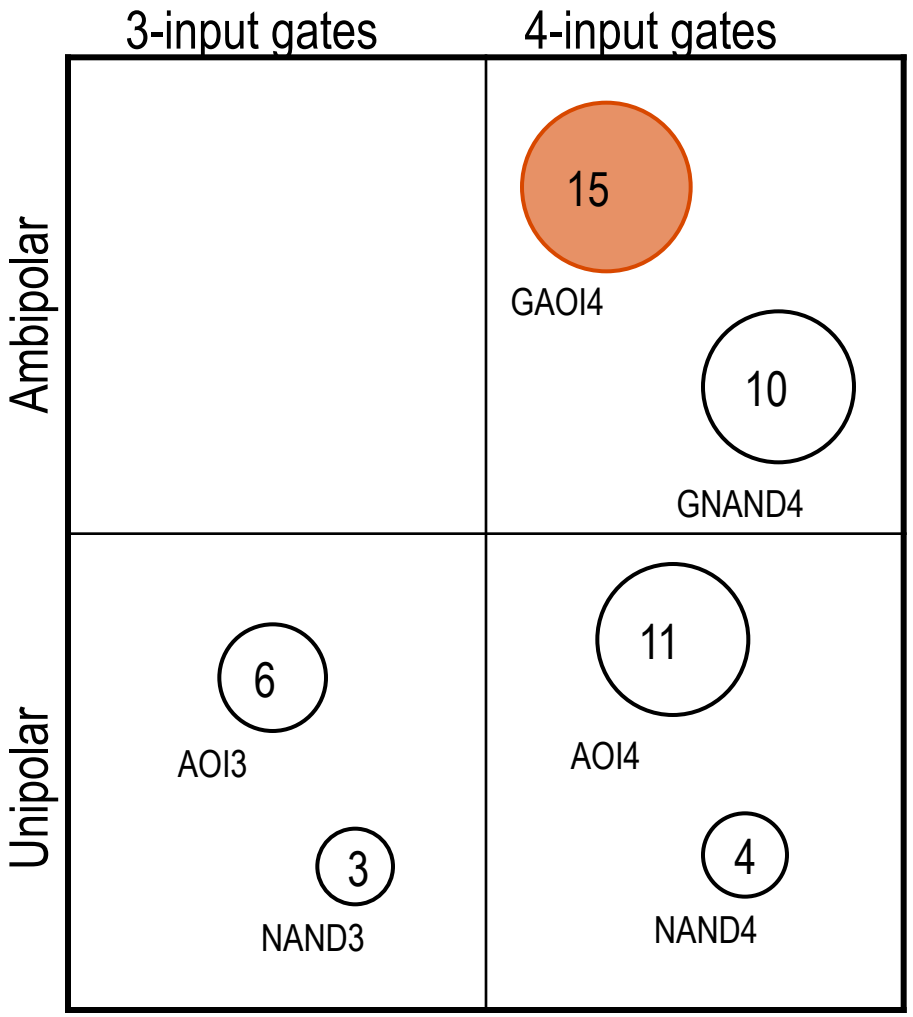
De Marchi et al., Nanoarch '10

Ben Jamaa et al., DATE '09

High Configurability of Ambipolar Logic Gates

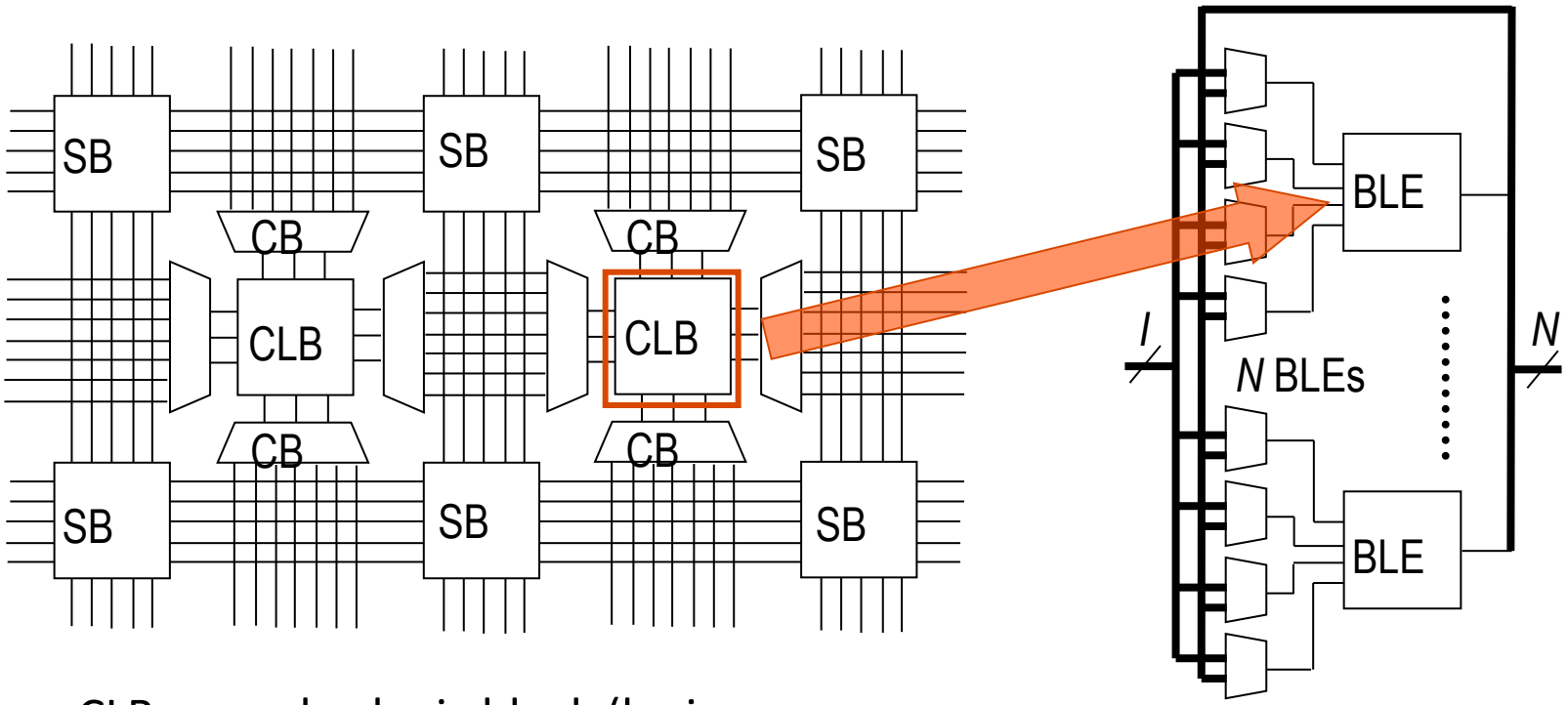
!A
A
!A + A·(!B)
(!A)·(!B)+A
(!A)·(!B)
A·(!B)
(!A)·(!B)+A·B
(!A)·(!C)+A·(!B)+A·B·(!C)
(!A)·(!B)+(!A)·B·(!C)+A·(!B)
(!A)·(!B)+(!A)·B·(!C)+A·(!B)·(!C)+A·B
(!A)·(!B)·(!C)+A·B·(!C)
(!A)·(!C)+A·(!B)·(!C)
(!A)·(!B)·(!C)+A·(!B)
(!A)·(!B)·(!C)+(!A)·(!B)·C·(!D)+(!A)·B·(!D) +A·(!B)·(!D)+A·B·(!C)+A·B·C·(!D)
(!A)·(!B)·(!D)+(!A)·B·(!C)·(!D)+ A·(!B)·(! C)·(!D)+A·B·(!D)

Functionality of GAOI4



Benchmark of functionalities

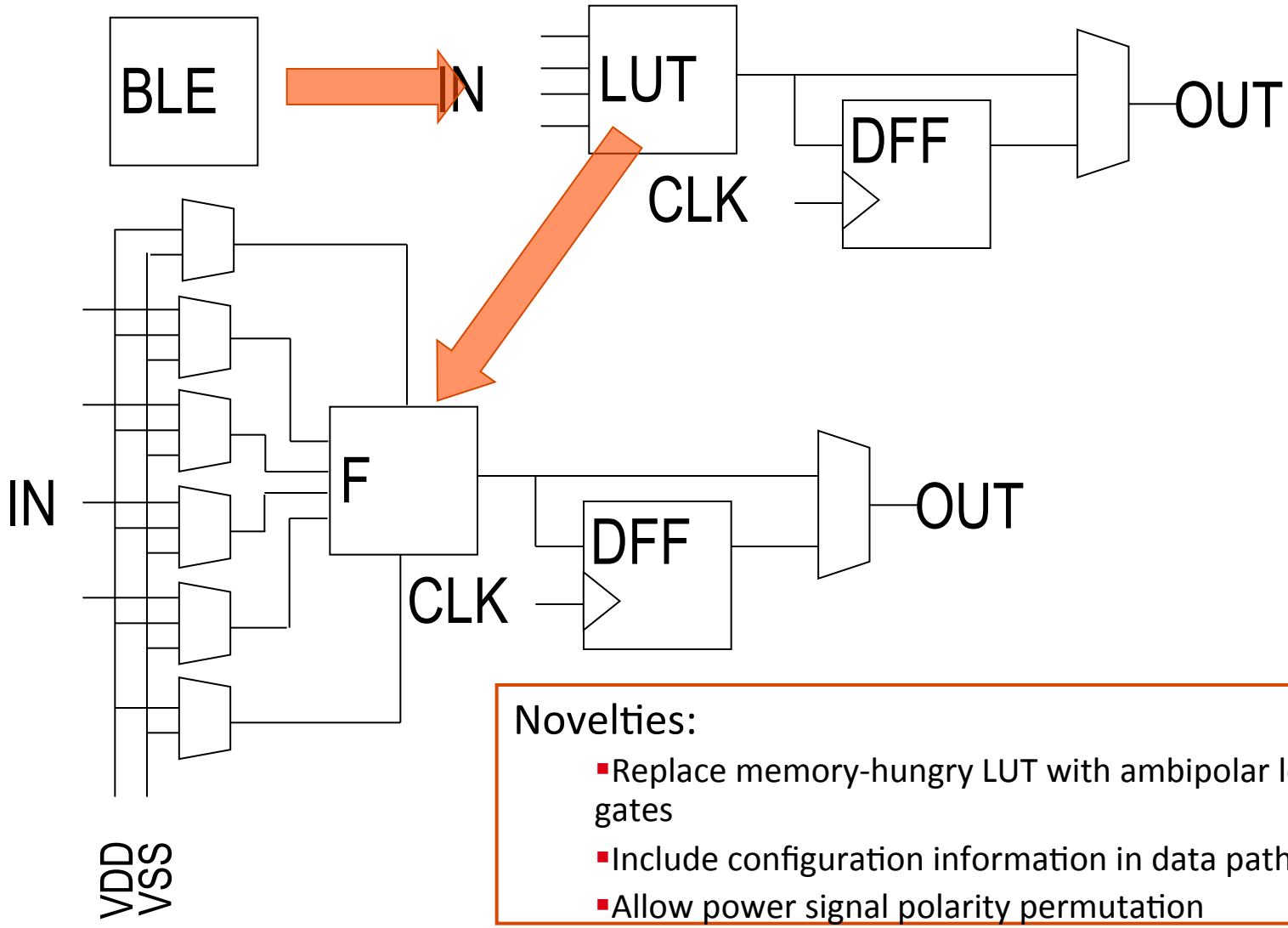
Reconfigurable FPGA Architecture



- CLB: complex logic block (logic macro-cell) with *I* inputs and *N* outputs
- CB: connection block (routing)
- SB: switch block (routing)
- BLE: basic logic element

V. Betz et al., "Architecture and CAD for Deep-Submicron FPGAs", Kluwer Academic Publishers '99

Enhanced FPGA Architecture



Novelties:

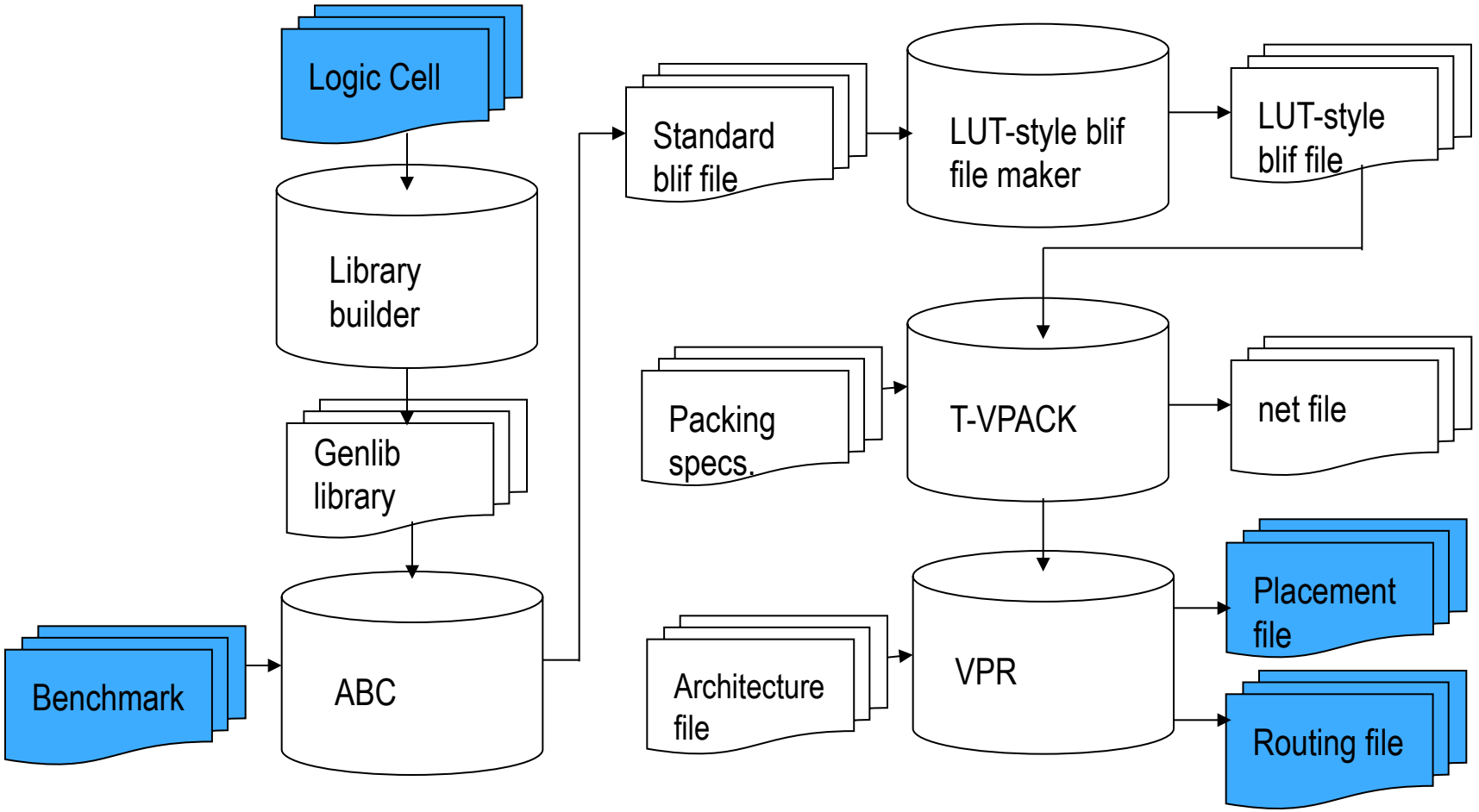
- Replace memory-hungry LUT with ambipolar logic gates
- Include configuration information in data path
- Allow power signal polarity permutation

Simulation Scenarios

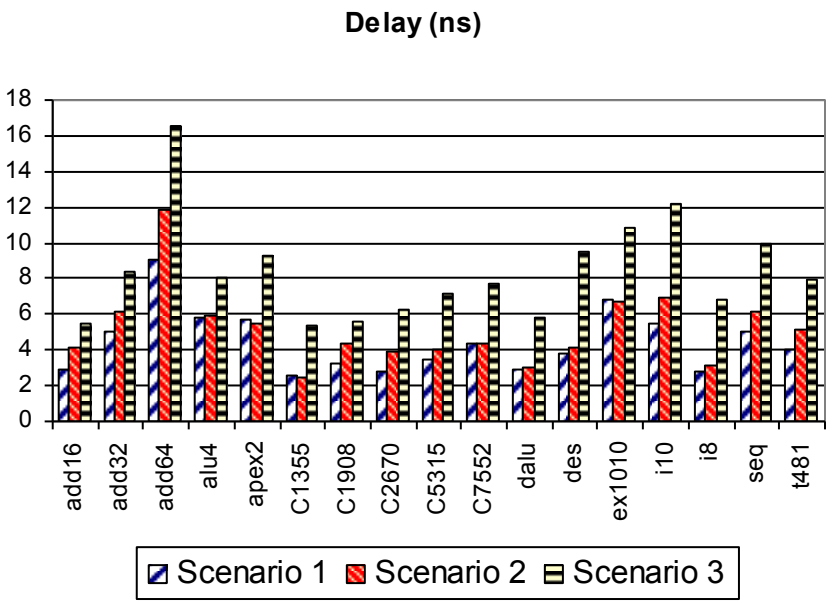
Scenario	Logic type	N	I	Norm. CLB area	Intra-CLB delay (ps)	Inter-CLB delay (ps)
S1	Reconf. ambipolar gates	1	4	2419	47	25
S2	LUT	1	4	2560	50	25
S3	Reconf. ambipolar gates	10	22	17167	200	423

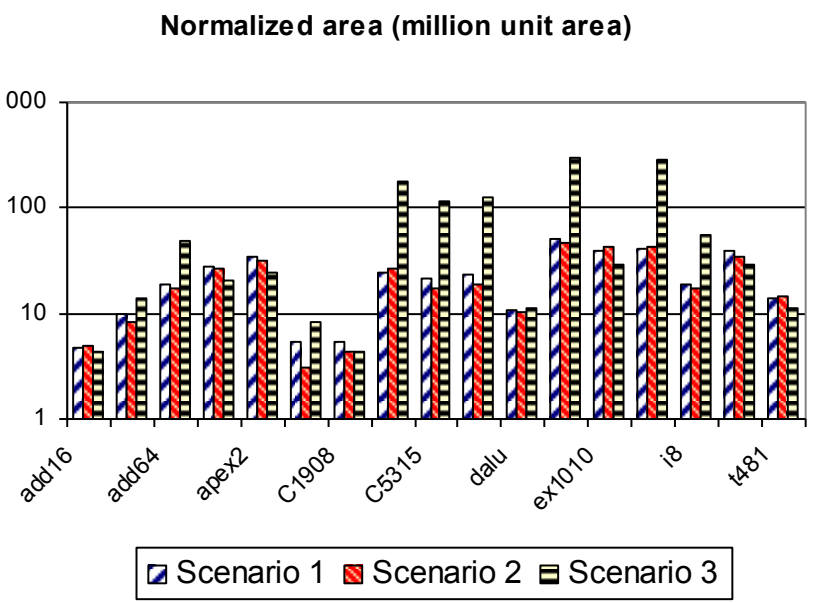
- Fine-grain architectures have smaller area- and intra-CLB delay.
- They have a lower inter-CLB delay because of lower load on CLB in- and outputs.
- Gate-based architectures are more compact because of a lower need for memory and the compact gate design.

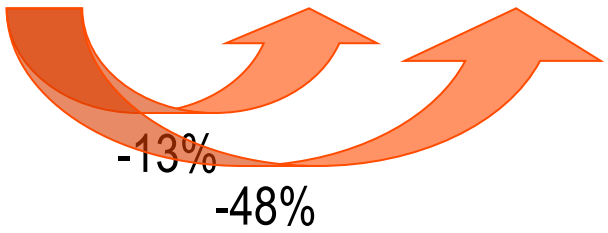
Synthesis Flow

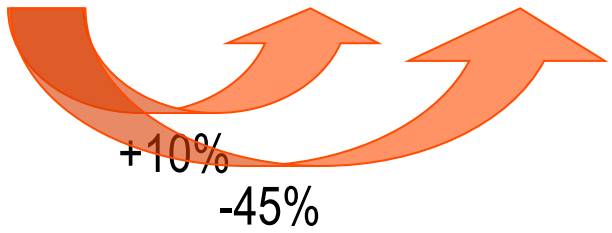


Simulation Results









Conclusions

- Double-gate carbon nanotubes FETs offer the opportunity to tune the device polarity.
- Reconfigurable FETs can be used in fine-grain reconfigurable logic circuits, such as FPGAs.
- These devices have a higher functionality that we leveraged in FPGAs design:
  - Compact logic, polarity permutation, configuration through the data path
- The approach offers faster FPGAs especially for fine-grain systems

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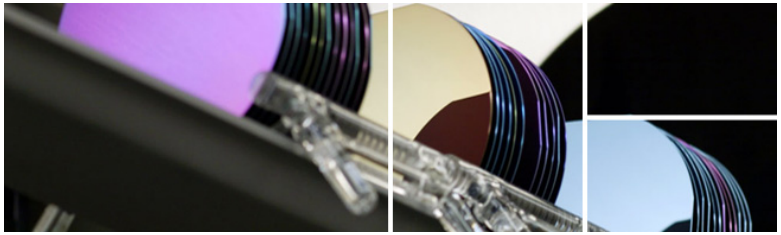

Thank you for your attention

Questions ?

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