

Emerging technologies and applications

The elephants in the technology room



Giovanni De Micheli
Marco Casale-Rossi

A free exchange symposium

- Objective is to discuss freely important topics
- Active participation and discussion is important
- Forward looking attitude

EVERYTHING
EVERYWHERE
ALL AT ONCE



SHOWTIME

**EVERYTHING (TECH & APPS)
IN MONTREUX
ALL AT ONCE**

SRAM Bitcells Are 10X Bigger than They Should Be

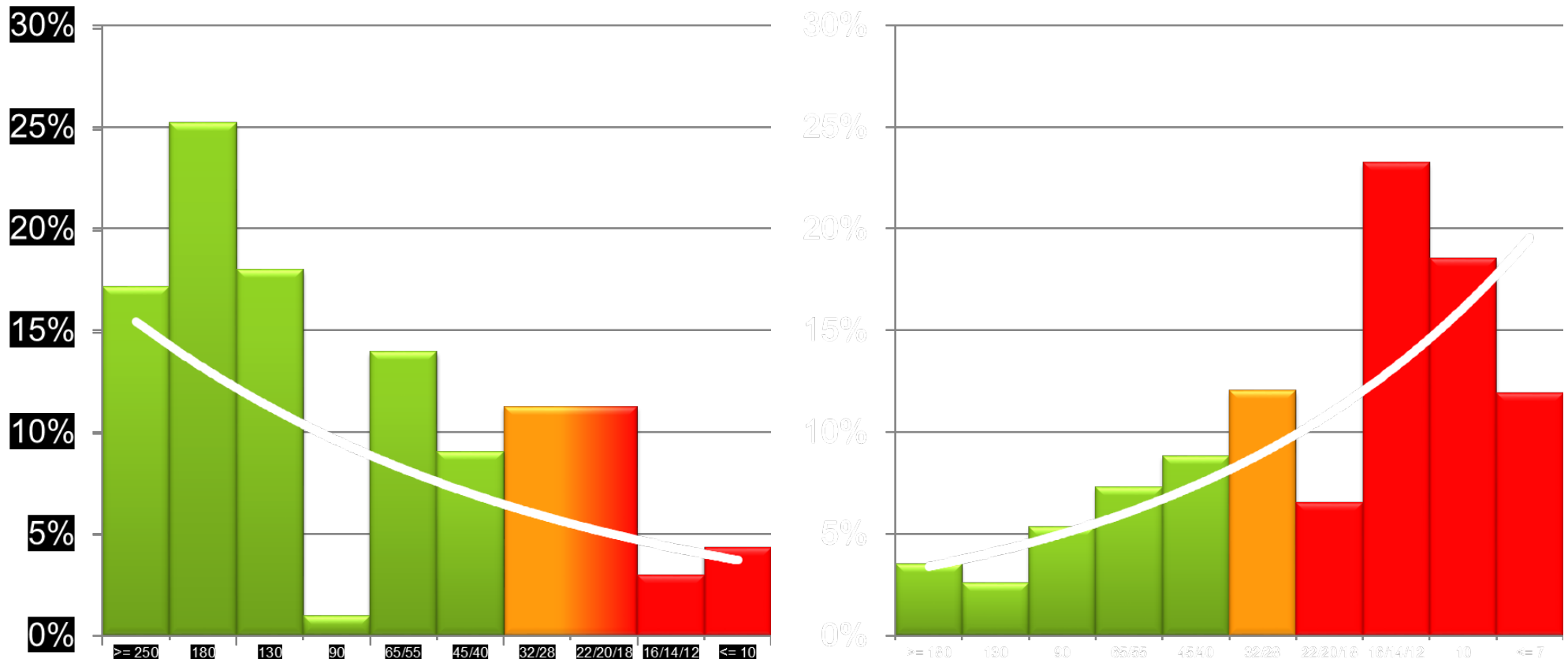
Technology Nodes Are Actually Half-Nodes, Barely

		N90	N65	N45	N32/28	N22/20	N16/14	N10	N7	N5	N3
	Moore's Law	1	0.5	0.25	0.125	0.0625	0.0312	0.0156	0.0078	0.0039	0.0019
Bitcell (um ²)	Intel	1	0.57	0.346	0.148 (N32 HD)	0.092 (N22 HD)	0.0499 (N14 HD)	0.0312 (HD)	0.024 (HD)	N.A.	N.A.
	Scaling (X)	-	1.75X	1.65X	2.34X	1.61X	1.84X	1.60X	1.30X	N.A.	N.A.
	TSMC				0.127 (N28 HD)	0.081 (N20 HD)	0.074 (N16 HD)	0.042 (HD)	0.027 (HD)	0.021 (HD)	0.0199 (HD)
	Scaling (X)				-	1.57X	1.09X	1.76X	1.56X	1.29X	1.05X
	Samsung				0.157 (N28 HD)	0.081 (N20 HD)	0.064 (N14 HD)	0.040 (HD)	0.0269 (HD)	0.026 (HD)	N.A.
	Scaling (X)				-	1.94X	1.27X	1.6X	1.54X	1X	N.A.

Source: S. Natarajan, Intel, IEDM 2014; K. Mistry, Intel Technology & Manufacturing Day, 2017;
 J. Chang, et al., TSMC, ISSCC 2013, 2017, 2020; Y.-H. Chen, et al., TSMC, ISSCC 2014; C.H. Chang, et al., TSMC, IEDM 2022; www.wikichip.org, 2023

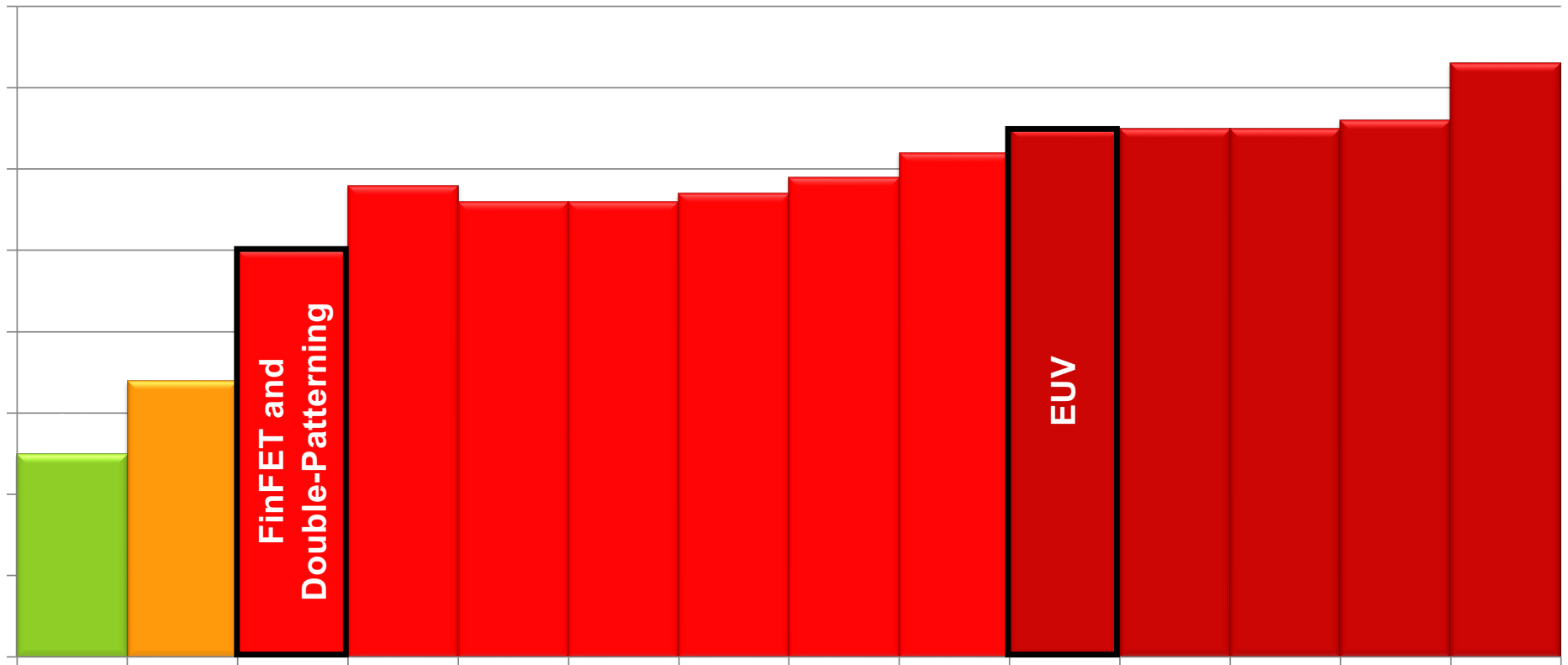
There Is an Inverse Relationship

Between % of Design Starts and % of Silicon Manufactured, by Technology Node
Nota Bene: No Design Starts/Silicon Manufactured @ 5/3 Nanometers in Europe

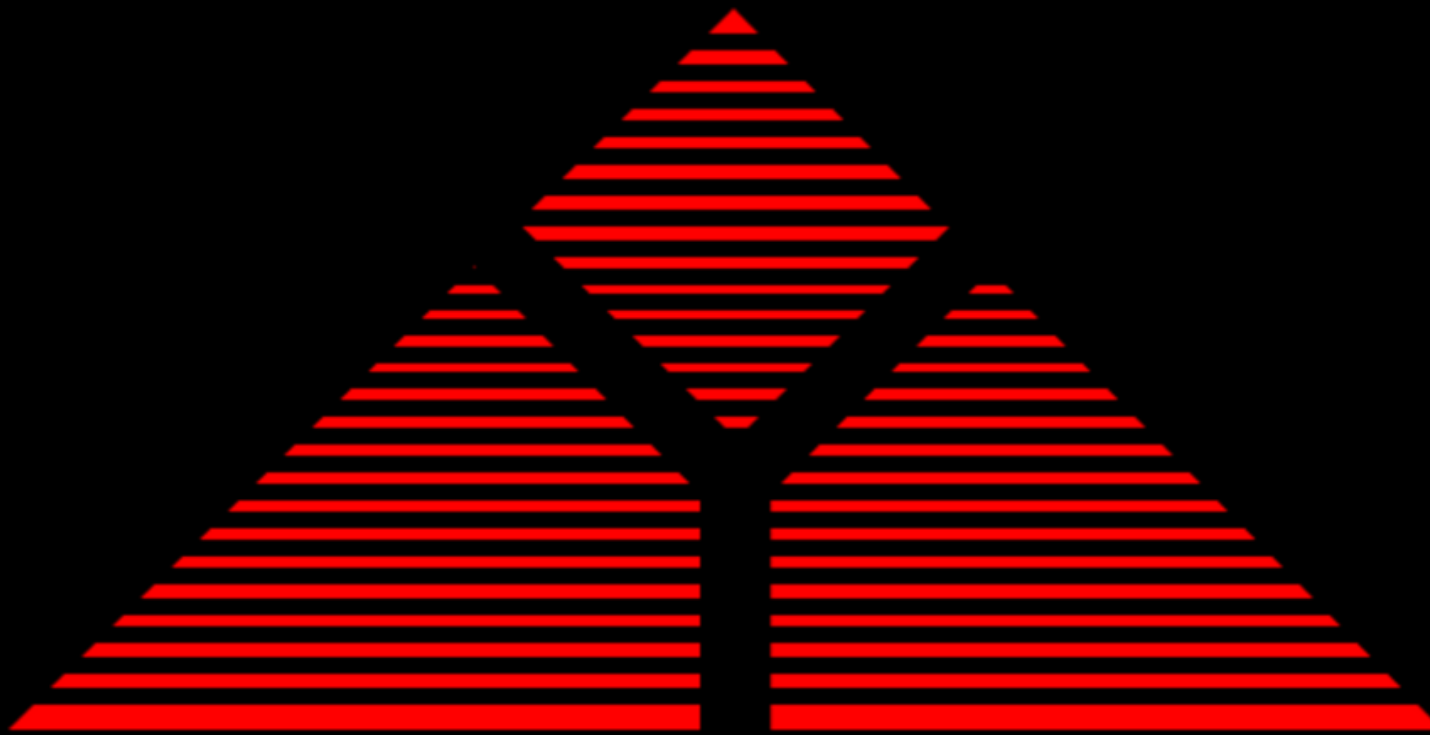


Gini Coefficient Applied To Semiconductor Industry

This Chart Shows the Evolution of the Distribution Inequality of Silicon Manufactured vs Number of Design Starts at a Given Technology Node Over the Last 10 Years



Source: Synopsys Research MAY2023



SKYNET

NEURAL NET-BASED ARTIFICIAL INTELLIGENCE

The Program

Thursday Morning: Future of Technical Exchange, Quantum Comp

- **8:15 Welcome: Giovanni De Micheli, EPFL & Marco Casale-Rossi, Synopsys**
- **8:45 - 9:30 Keynote: Joachim Kunkel, Synopsys: The changing landscape of the semiconductor industry**
- **9.30 – 10:00 Discussion**
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- **10:00 – 10:30 Coffee break**
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- **10:30 - 11:15 Keynote: Jason Cong, UCLA: Layout Synthesis and Architecture Customization for QC**
- **11:15 – 12:30 Panel: How will QC be designed? Chair: Robert Wille, T.U. Munich**

Thursday Afternoon: Safety, Security, Privacy

- **14:00 – 14:45 Keynote: Mike Borza, Synopsys:** Having Our Cake and Eating It Too: Are Safety, Security and Privacy Possible Simultaneously?
- **14:45 – 15:30 Keynote: Ingrid Verbauwede, KU Leuven:** Hardware: an essential partner to cryptography
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- **15:30 – 16:00 Coffee Break**
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- **16:00 – 17:15 Panel: Will information security be a reality for everyone?**
Chair: Wayne Burleson, U.M. Amherst

Thursday Evening

- **19:00 – 20:00 Cocktail**
- **20:00 – 23:00 Dinner**
- **22:00 – 22:30 Dinner Keynote: Patrick Groeneveld, Cerebras: Sustainable innovation: Are we not fooling ourselves?**



Friday Morning: The Metaverse of Things

- **8:30 – 9:15 Keynote: Jan Rabaey, UC Berkeley:** The Mirror World – The Land between the Meta- and the Omniverse
- **9:15 – 10:00 Keynote: Alessandro Cremonesi, STMicroelectronics:** *The beauty of being the "Enabler of the Future"*
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- **10:00 – 10:30 Coffee break**
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- **10:30 – 11:45 Panel: Humans vs. Things on the metaverse. Chair: Jamil Kawa, Synopsys**
- **11:45 – 12:30 Keynote: Tibor Merey, Boston Consulting Group:** How the Metaverse will Remake your Strategy

Friday Afternoon: Technology of the 30s

- **14:00 – 14:45 Keynote: Raul Camposano, Silvaco** – TCAD Digital Twins for semiconductor manufacturing
- **14:45 – 15:30 Keynote: Subhasish Mitra, Stanford University** – The Future of Hardware Technologies for computing
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- **15:30 – 16:00 Coffee Break**
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- **16:00 – 17:15 Panel: Is In-Memory computing a niche area or the main hardware platform for AI/ML? Chair: Luca Benini, ETHZ**

Thanks

- The speakers for their effort
- EPFL and Synopsys for their support
- Chantal Demont and the Suisse Majestic staff

