SILVACO

Digital Twins for Semiconductor Manufacturing

Montreux, 2023

Raúl Camposano
CTO

April 2023

Agenda

- Introduction
- TCAD
- Digital Twin Foundations

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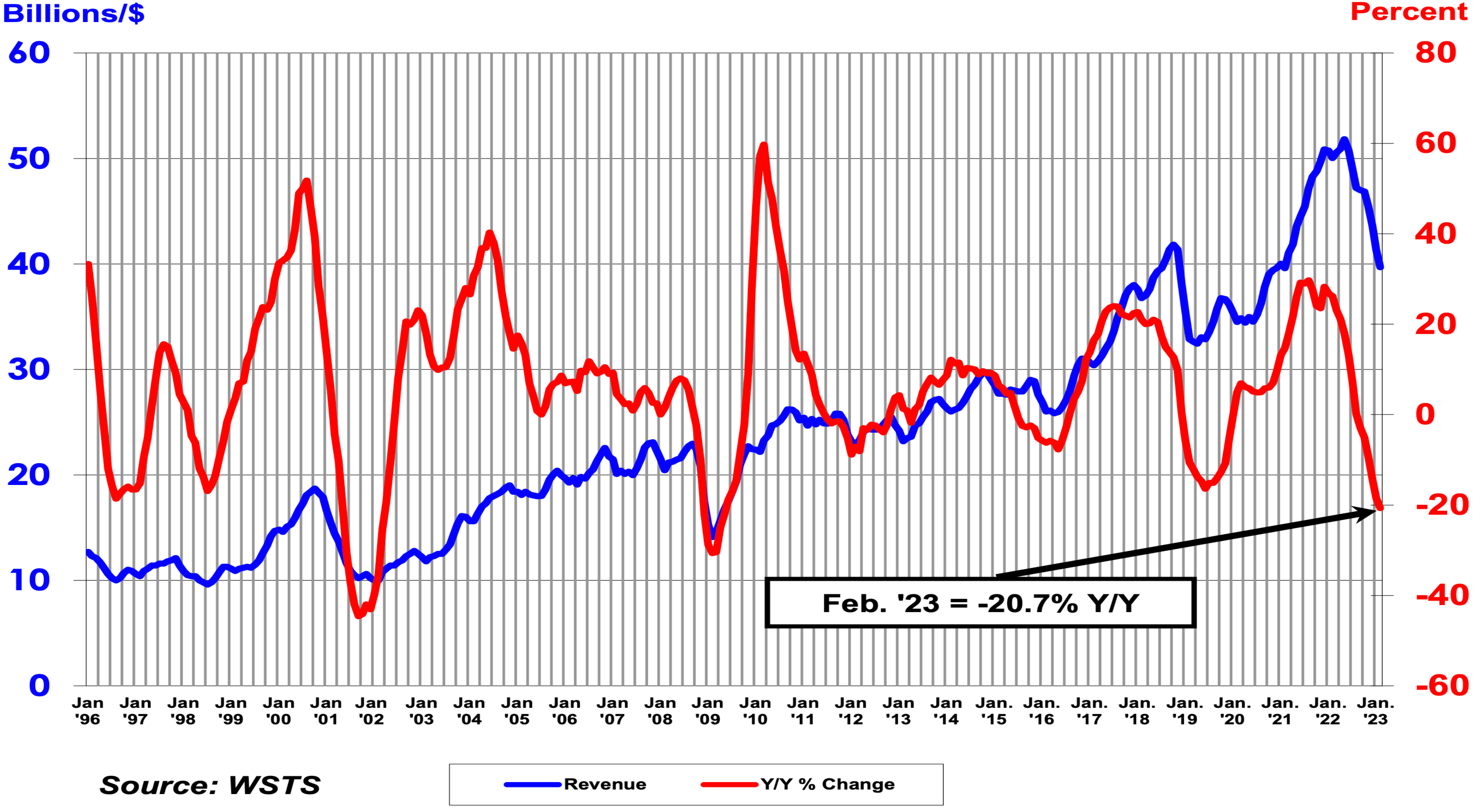
Semiconductors



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Rock's Law

Just in case someone has not seen it….
Moore's Original graph

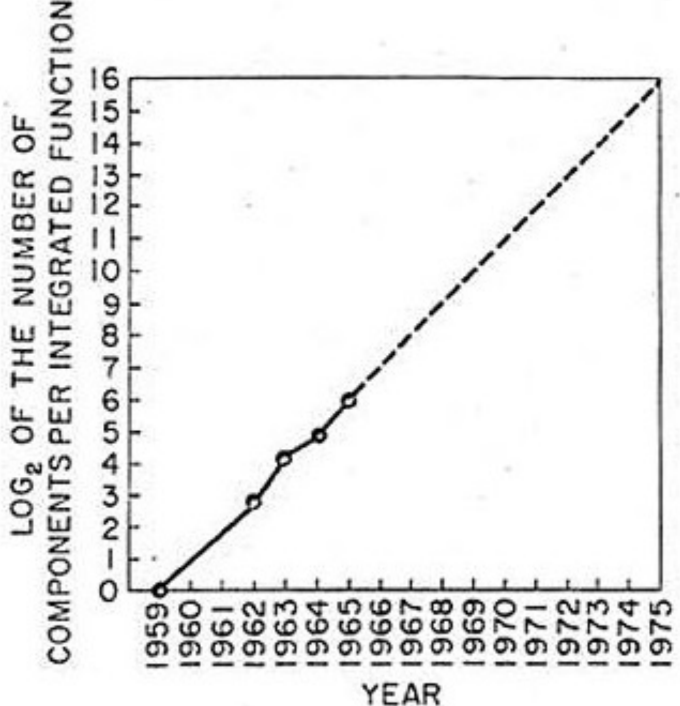


Fig. 2 Number of components per integrated function for minimum cost per component extrapolated vs time.

Source: Gordon E. Moore,
Cramming More Components onto Integrated Circuits,
Electronics, pp. 114–117, April 19, 1965.

Rock's Law
The cost of semiconductor chip fabrication doubles every 4 years
(Arthur Rock, VC, 1965?)

"This fab could cost upwards of $20 billion and represents TSMC's commitment to drive technology forward," Co-Chief Executive Mark Liu…

MARKETPLACE
EUROPE

Intel will invest nearly $90 billion in Europe's chipmaking industry

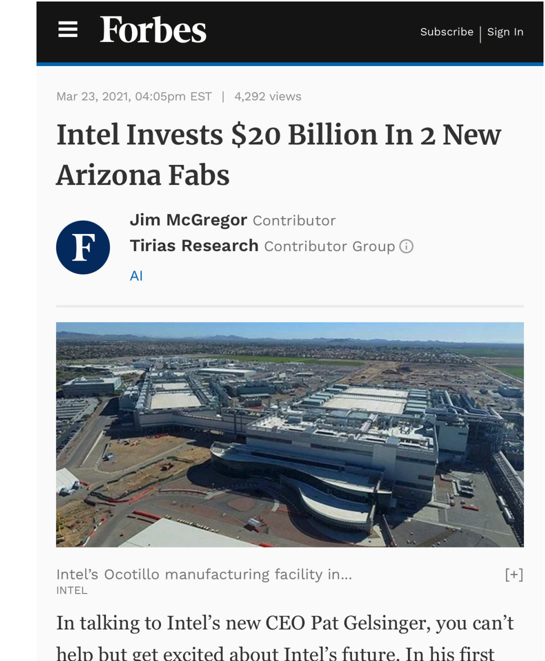
By Anna Cooban, CNN Business

Updated 1:17 PM ET, Tue March 15, 2022

THE WALL STREET JOURNAL.

EU Seeks to Double Share of World Chip Market by 2030 in 'Digital Sovereignty' Drive

Bloc pledges more than $150 billion to bolster technological independence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Mar 23, 2021, 04:05pm EST | 4,292 views

Intel Invests $20 Billion In 2 New Arizona Fabs

Jim McGregor Contributor
Tirias Research Contributor Group
AI

Intel's Ocotillo manufacturing facility in... [+]
INTEL

In talking to Intel's new CEO Pat Gelsinger, you can't help but get excited about Intel's future. In his first major announcement, or should I say announcements, as CEO, Mr. Gelsinger unveiled a revised company manufacturing strategy, business strategy, and commitment to company goals. Mr.

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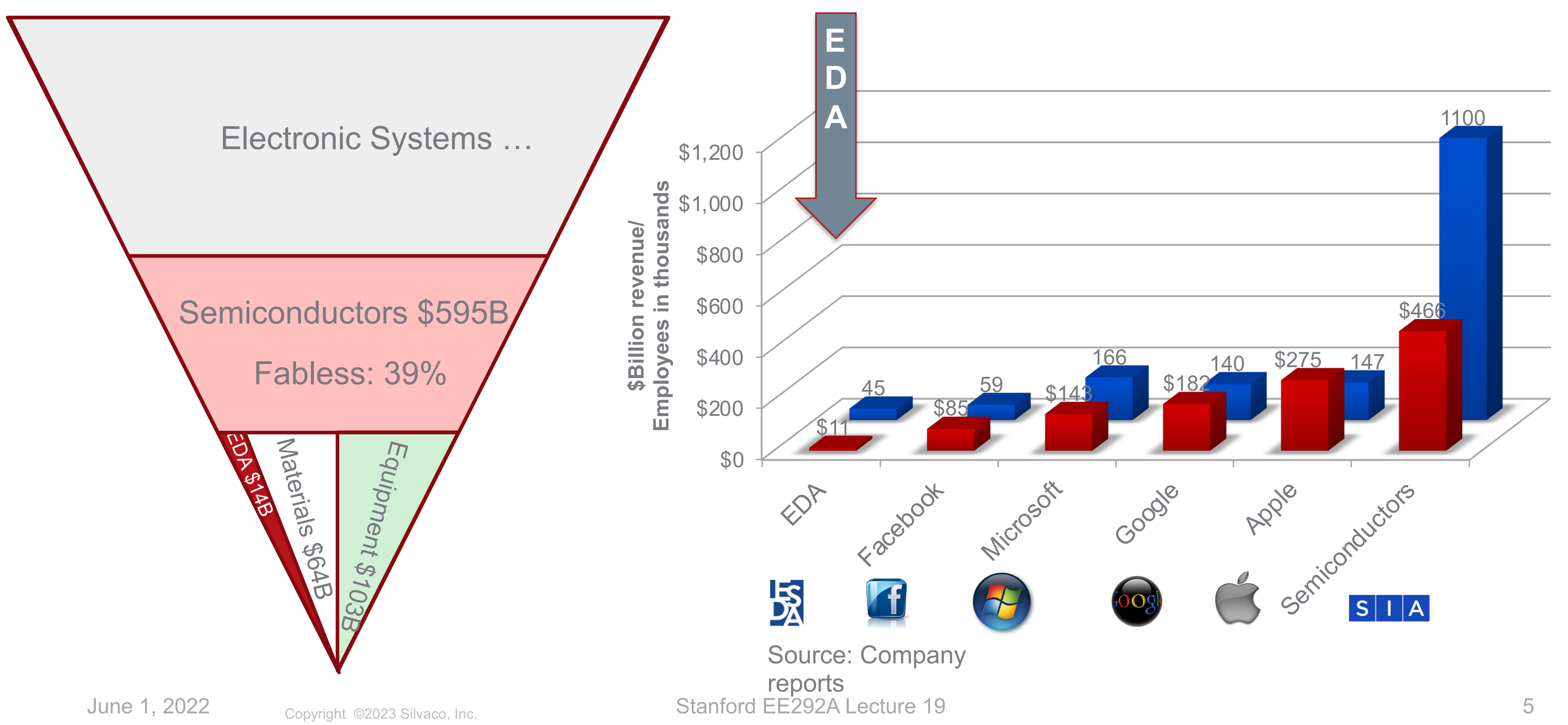
The EDA Industry in Perspective



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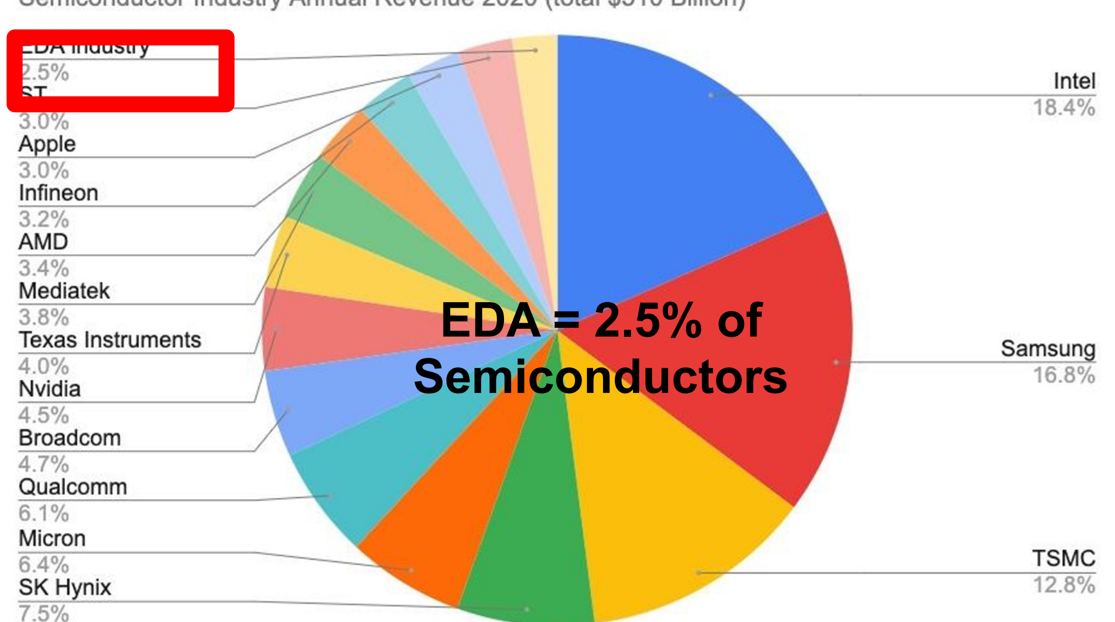
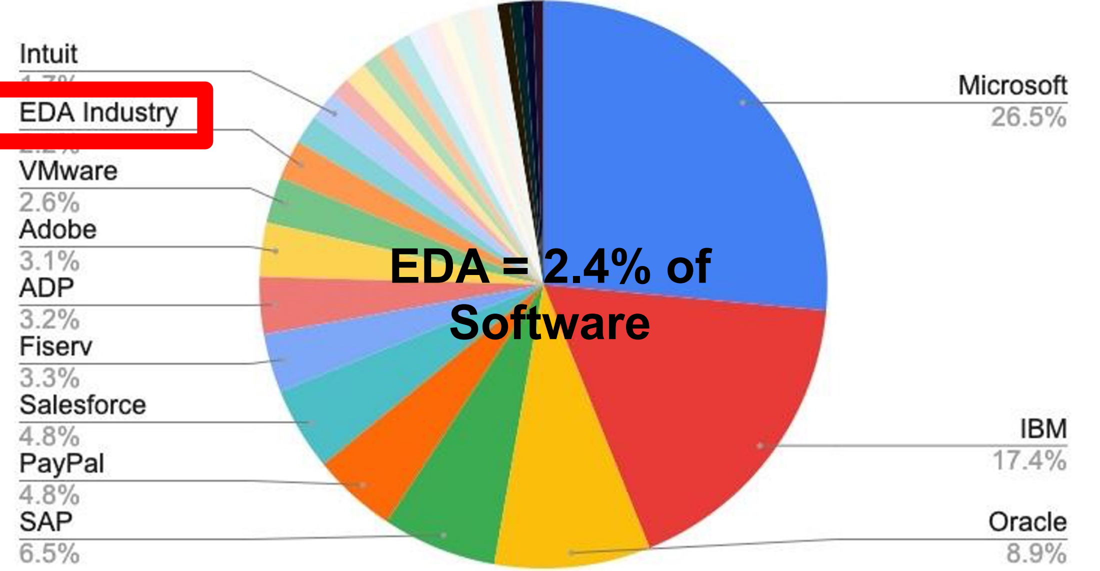
EDA Industry: Semiconductor + Software

Company	Employees	Annual Sales	Market value	Major Locations, other than Silicon Valley
Synopsys	15,000	$3.7B	$52B	India, China, Europe, Armenia
Cadence	10,000	$2.7B	$50B	India, China, Europe, Taiwan
Siemens EDA (Mentor)	~6,000	~$1.6B	~$20B	Oregon, India
Other EDA & IP	~24,000	~$6.5B	?	Worldwide
Total EDA approx.	**55,369**	**$14.5B**	**>$150B**	Worldwide

Semiconductor companies

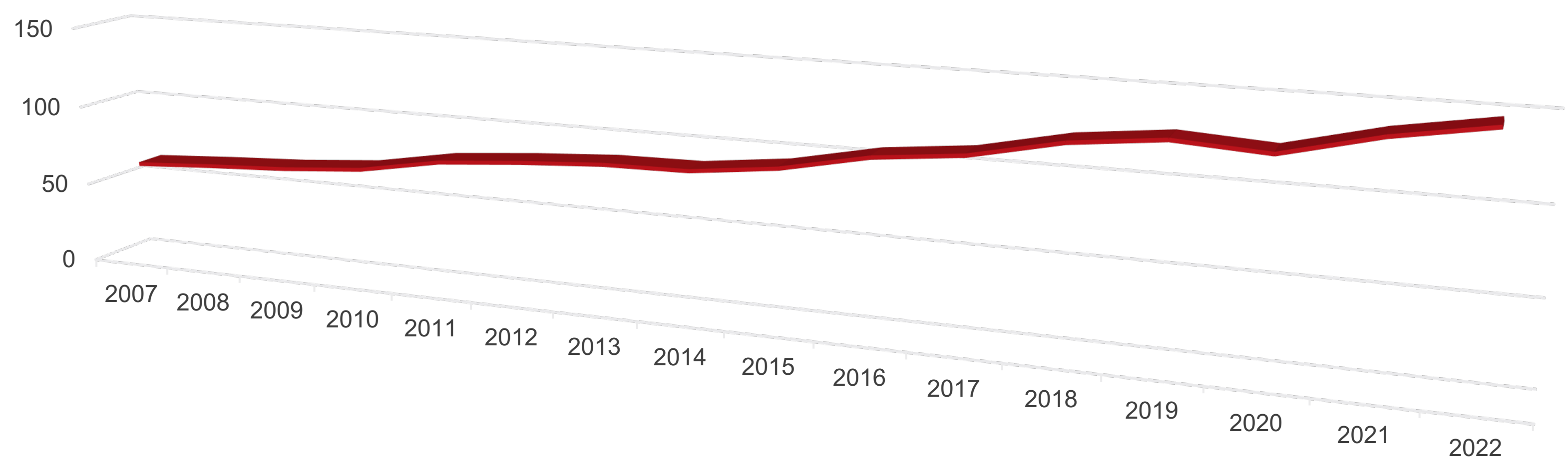
Semiconductor Industry Annual Revenue 2020 (total $510 Billion)





Software companies

TCAD Market



WW CAGR 2007-2022

TCAD	5.9% - 8.0%
EDA	5.5%
SEMI	5.5%
GDP	3.7%

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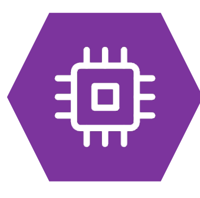
Silvaco at a Glance

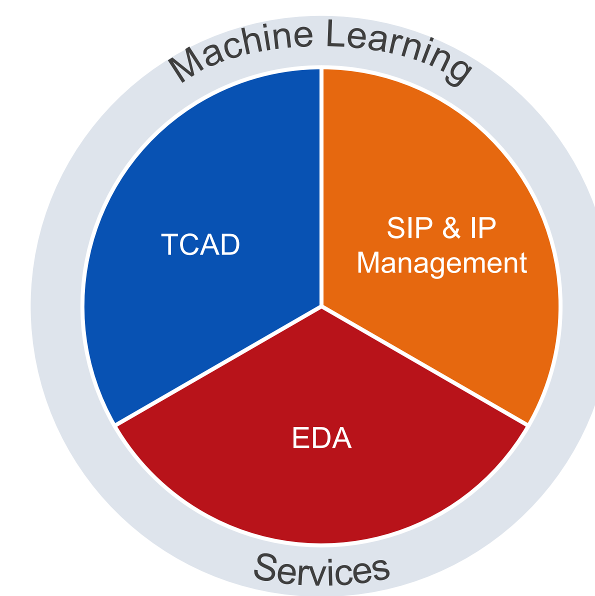
600+
Customers Worldwide

200+
University Customers Worldwide

250+
Employees



#1
TCAD and Modeling for Flat Panel, Power



Targeted academic research and sponsorships:
TU Vienna, Purdue, CEA Leti, INRIA, ST, Surrey…

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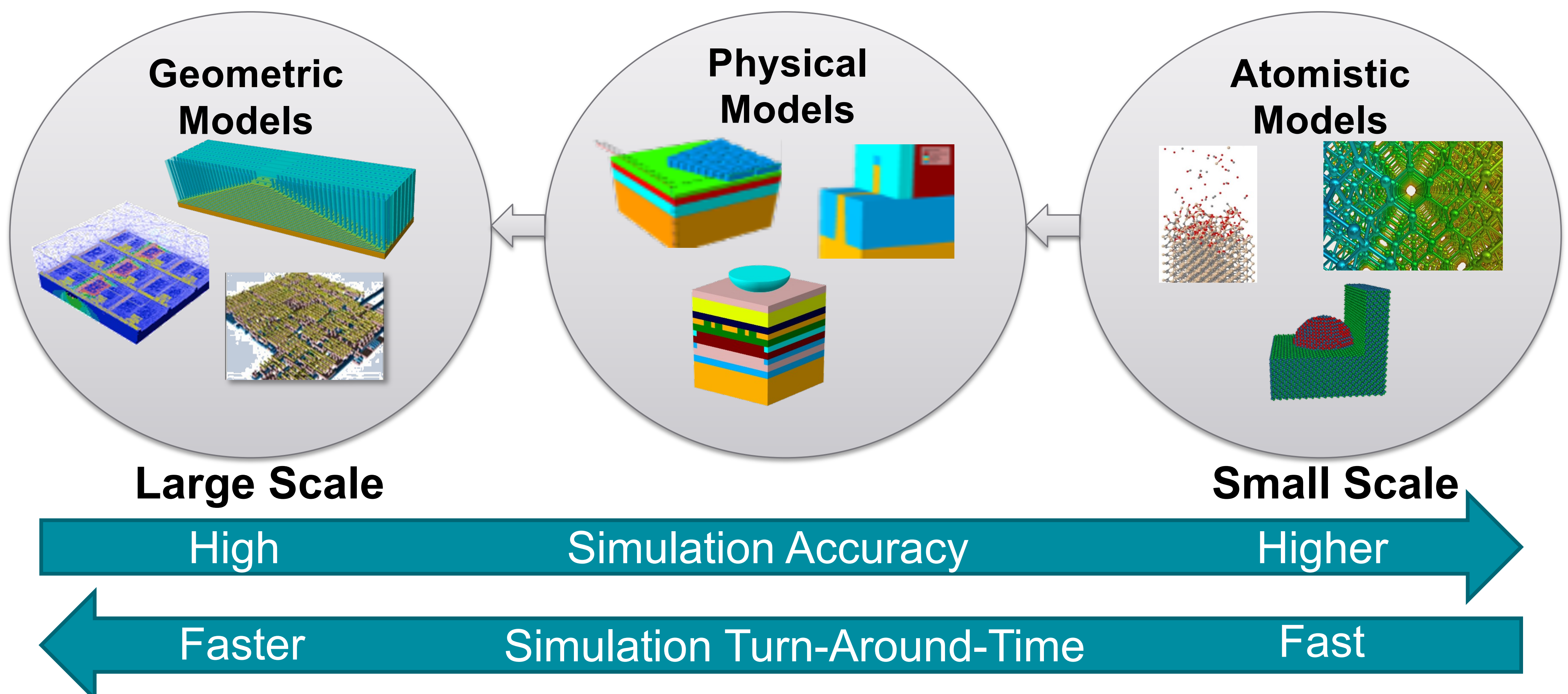
TCAD Solutions

From Atomistic to Large Scale



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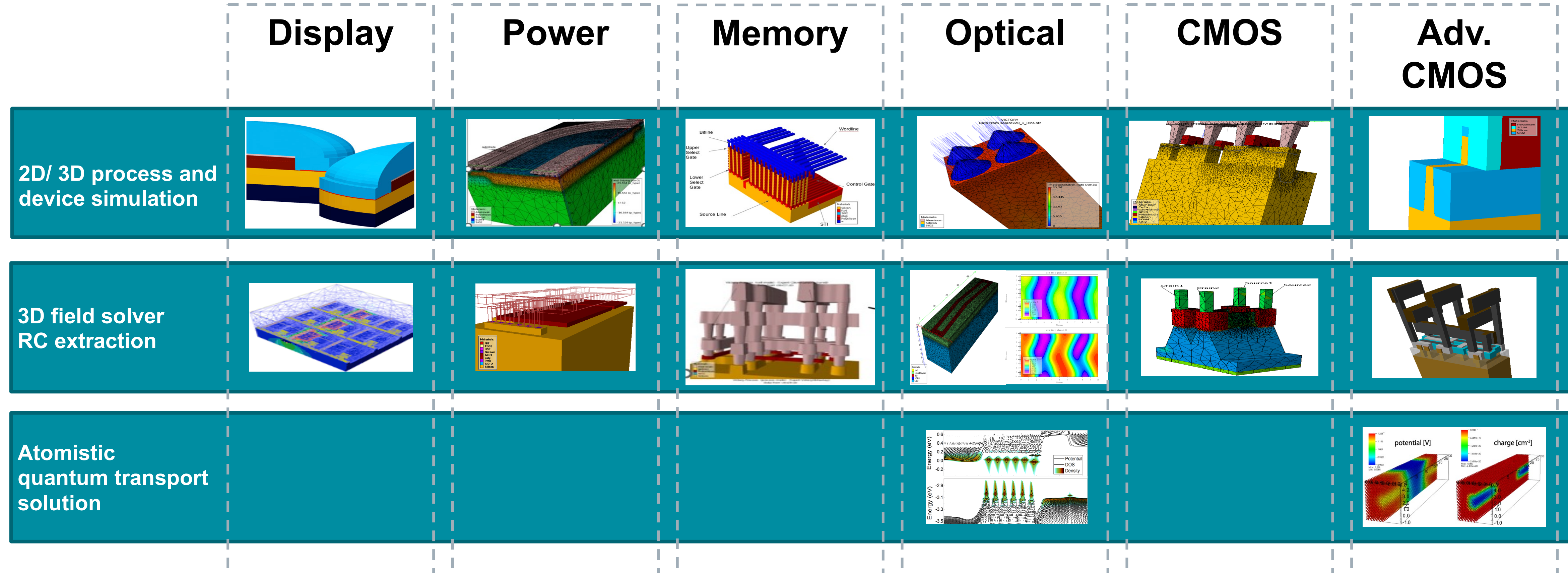
TCAD Target Markets



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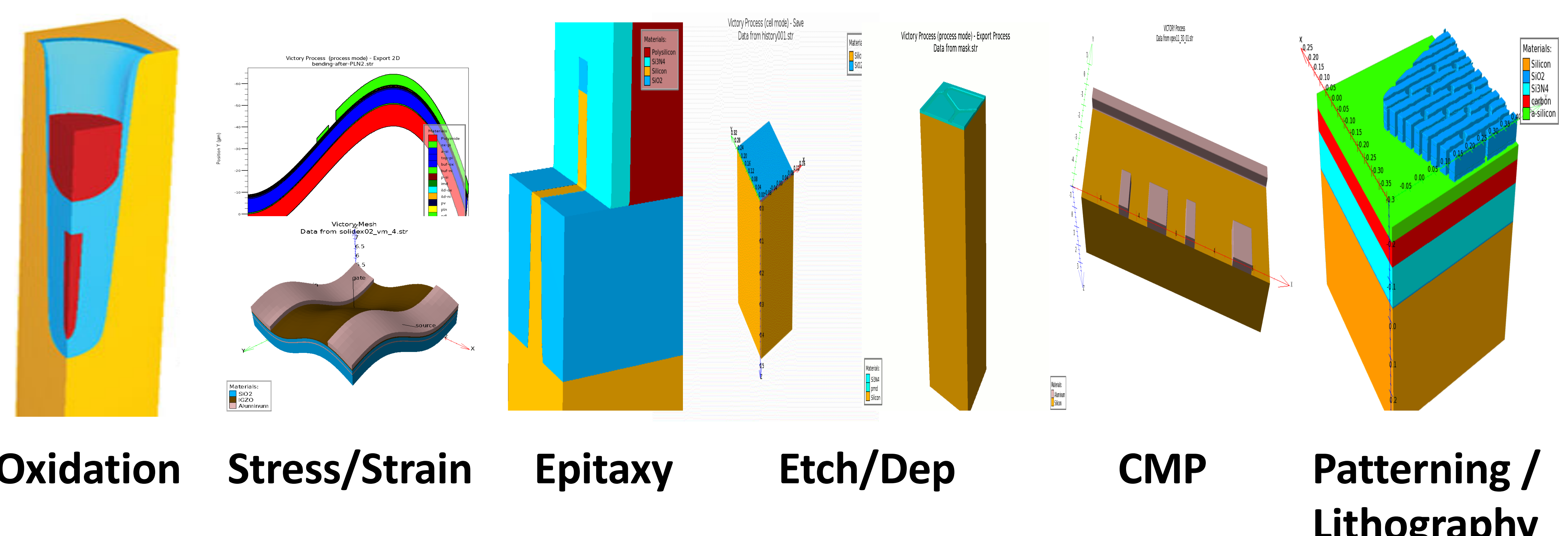
Typical Manufacturing Steps Simulated in TCAD



Oxidation **Stress/Strain** **Epitaxy** **Etch/Dep** **CMP** **Patterning / Lithography**

From Unit Process to Process Integration

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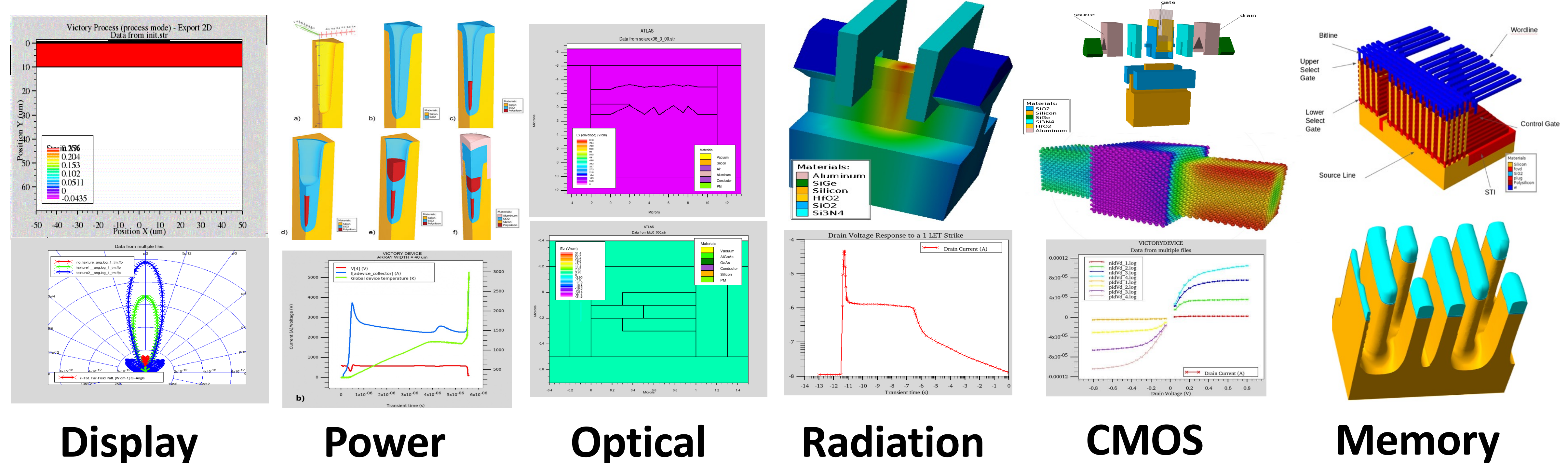
Typical Devices Simulated in TCAD

Modeling Semiconductor Device Operation



Display **Power** **Optical** **Radiation** **CMOS** **Memory**

Electro-Optical-Thermal-Stress-Chemistry

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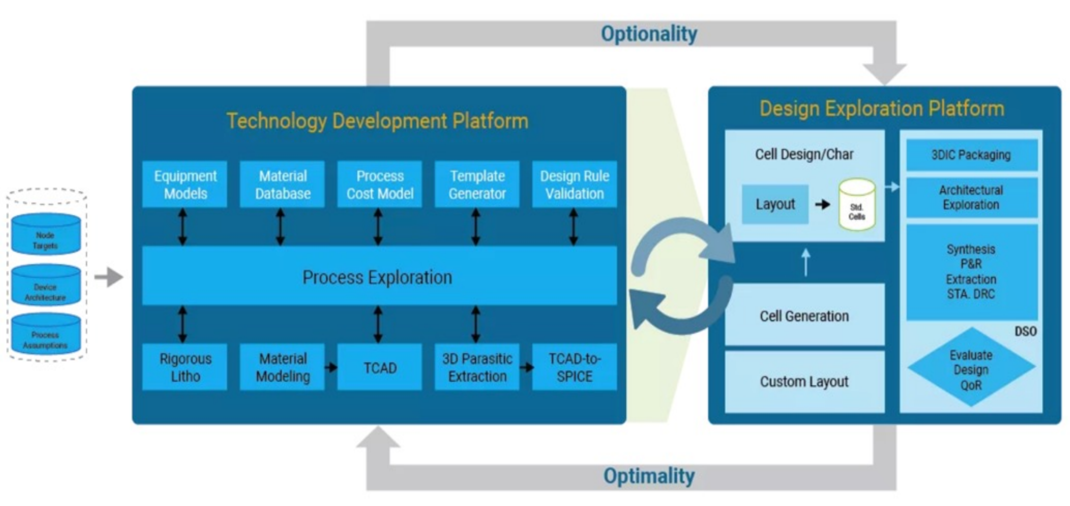
DTCO: Connecting Semiconductor Physics to Circuit Design

Silvaco DTCO Flow



Synopsys DTCO Flow

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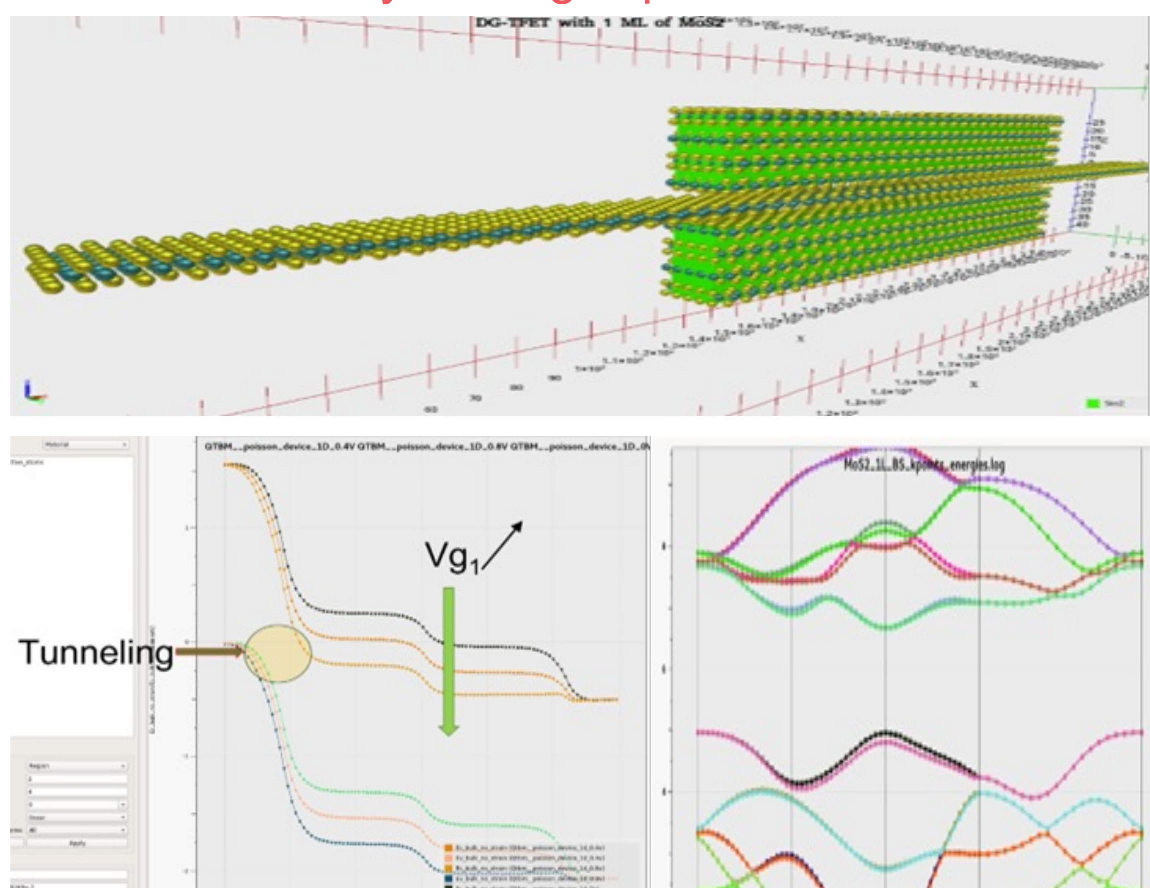
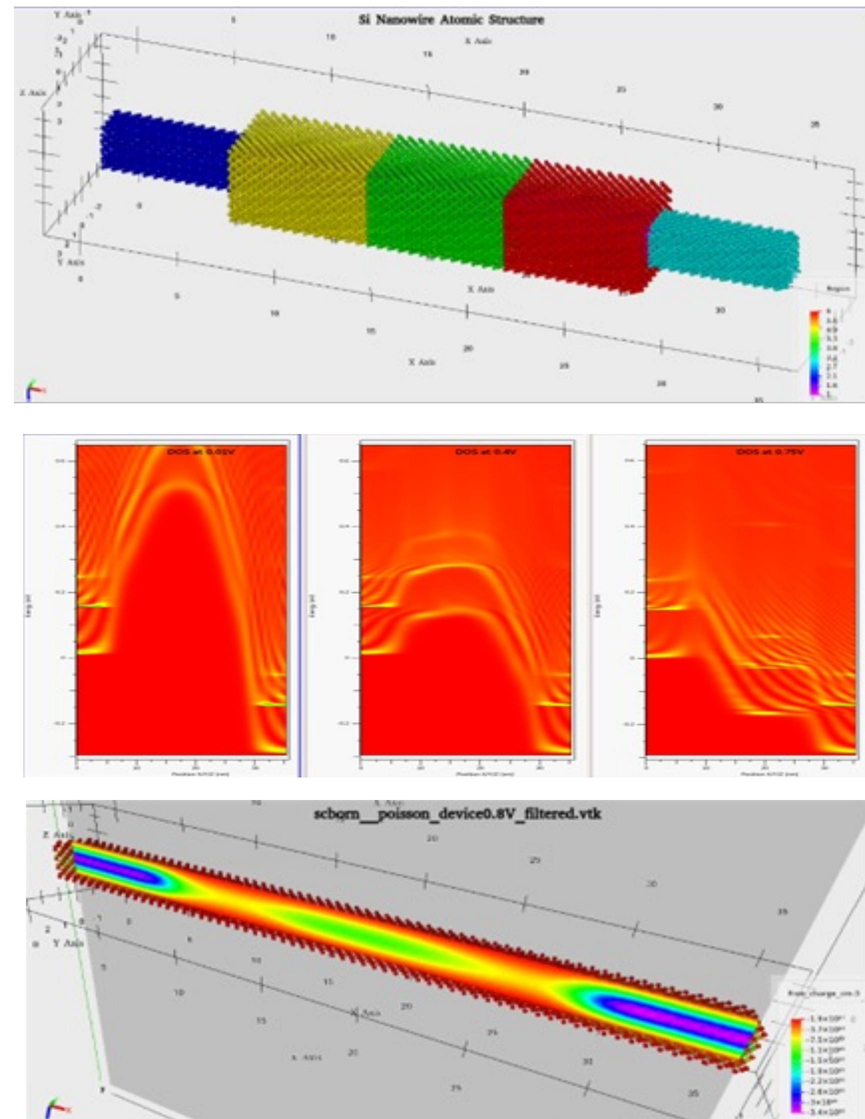
Visualization

TCAD is not only solving Equations



Dual-gate Tunnel FET with one monolayer of MoS_2
Top: device structure with insulator (green), Mo (blue) and S (yellow) atoms
Bottom left: Band Structure of the Wannier Hamiltonian
Bottom right: TFET 1D band profile function of the gate voltage applied



A silicon nanowire FET with 20 orbitals per atom and 8 000 atoms with modespace and electron-phonon scattering: visualization of the NEGF results with Victory Visual
Top: NWFET structure with spacers
Middle: Density of States resolved in space and energy for different grid voltages
Bottom: Free charges in the NWFET

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Digital Twins

- The concept and model of the digital twin was first publicly introduced in 2002 by Michael Grieves, at a Society of Manufacturing Engineers conference in Troy, Michigan as the conceptual model underlying PLM - now "Industry 4.0"
- NASA's solution for fixing the damaged Apollo 13 spacecraft is one of the earliest examples of digital twin usage: 15 simulators which were used to train NASA astronauts and controllers in every aspect of the mission, including failure scenarios.
- Models can be better than observations (in chip design this is obvious)

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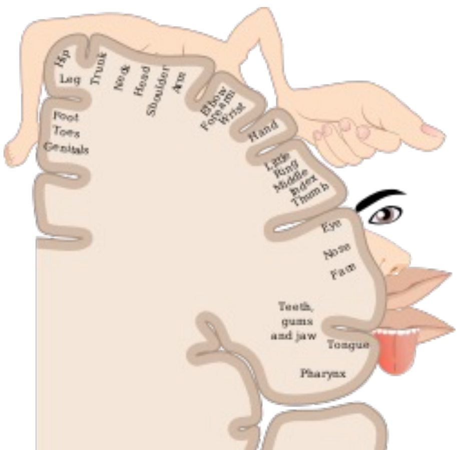
Digital Twins (1)

- Homunculus fallacy, dualism
- Neurological map within the sensory cortex

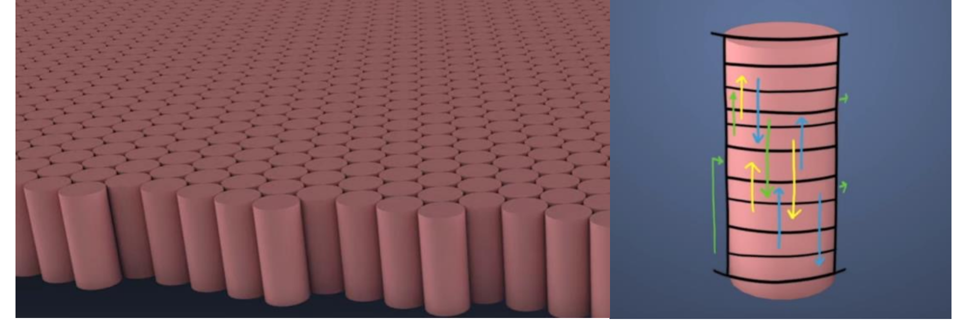


- Model of the world

New brain

aka neocortex

Jeff Hawkins. *A Thousand Brains*, Basic Books, 2021



~150,000 similar cortical columns

Every part of the neocortex has the same complex circuitry, then every part is doing the same thing (Mountcastle, 1978)

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Digital Twins (2)

- On Exactitude in Science (*Borges, 1946, El Rigor En La Ciencia*)

  Imagines an empire where the science of cartography becomes so exact that only a map on 1:1 scale of the empire itself will suffice

- Sylvie and Bruno (*Lewis Carrol, 1889)*

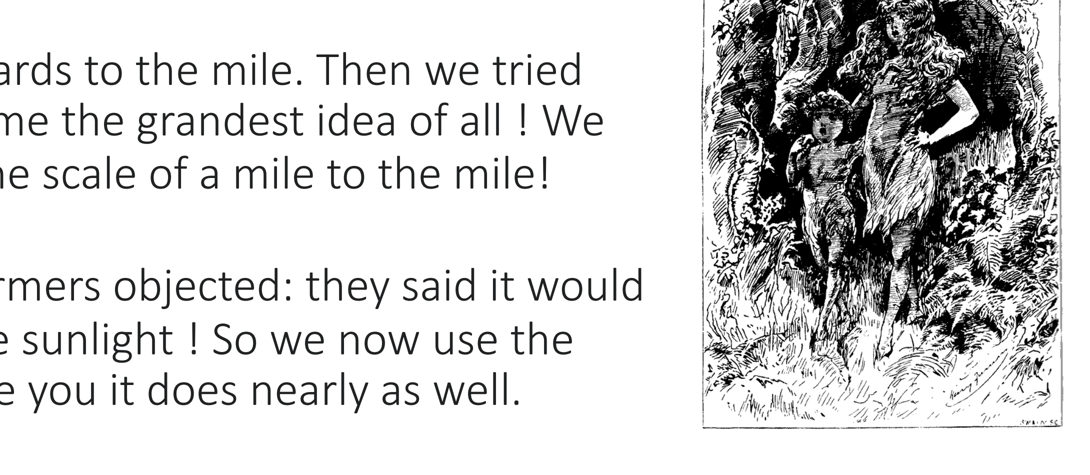
  What do you consider the largest map that would be really useful?

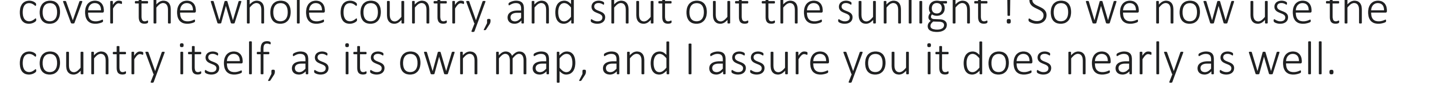
  About six inches to the mile.

  Only six inches! We very soon got to six yards to the mile. Then we tried a hundred yards to the mile. And then came the grandest idea of all ! We actually made a map of the country, on the scale of a mile to the mile!

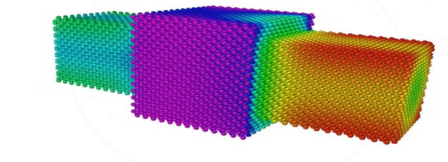
  Have you used it much?

  ”it has never been spread out, yet, the farmers objected: they said it would cover the whole country, and shut out the sunlight ! So we now use the country itself, as its own map, and I assure you it does nearly as well.





- Atomistic 1:1



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Digital Twins (3)

The Economist, May 7th, 2022

Such a plane would, in some sense, be ***"aware"*** of how its various components were performing… Researchers use it as an excuse for describing the system as "***conscious"***, a term which they say reflects a direction of travel rather than a goal.

The Cranfield team hope to have a whole-aircraft digital twin operating with a degree of self-awareness flying on an aircraft by 2035. Whether such a system will include a sense of shame for lousy cabin service remains to be seen.

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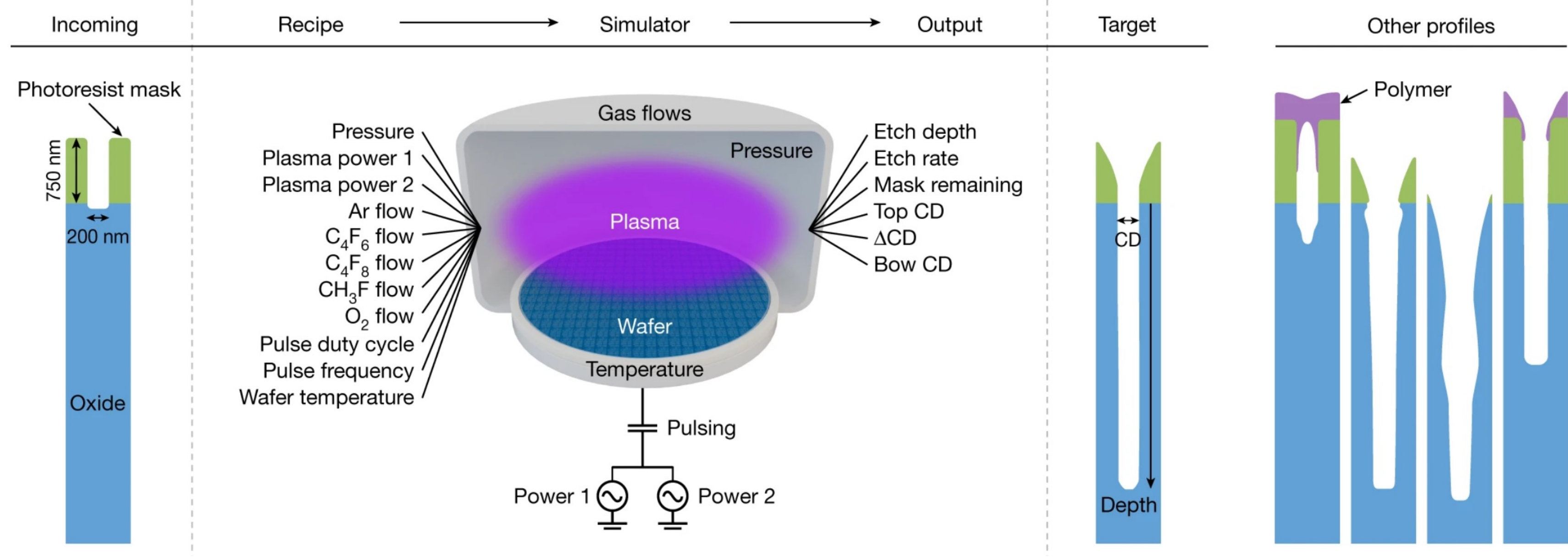
Virtual Process

Fig. 1: Schematic of the virtual process used in the game.

From: Human–machine collaboration for improving semiconductor process development



The input of the virtual process is a 'recipe' that controls the plasma interactions with a silicon wafer. For a given recipe, the simulator outputs metrics along with a cross-sectional image of a profile on the wafer. The target profile is shown along with examples of other profiles that do not meet target. The goal of the game is to find a suitable recipe at the lowest cost-to-target. CD, critical dimension.

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Nature (*Nature*) | ISSN 1476-4687 (online) | ISSN 0028-0836 (print)

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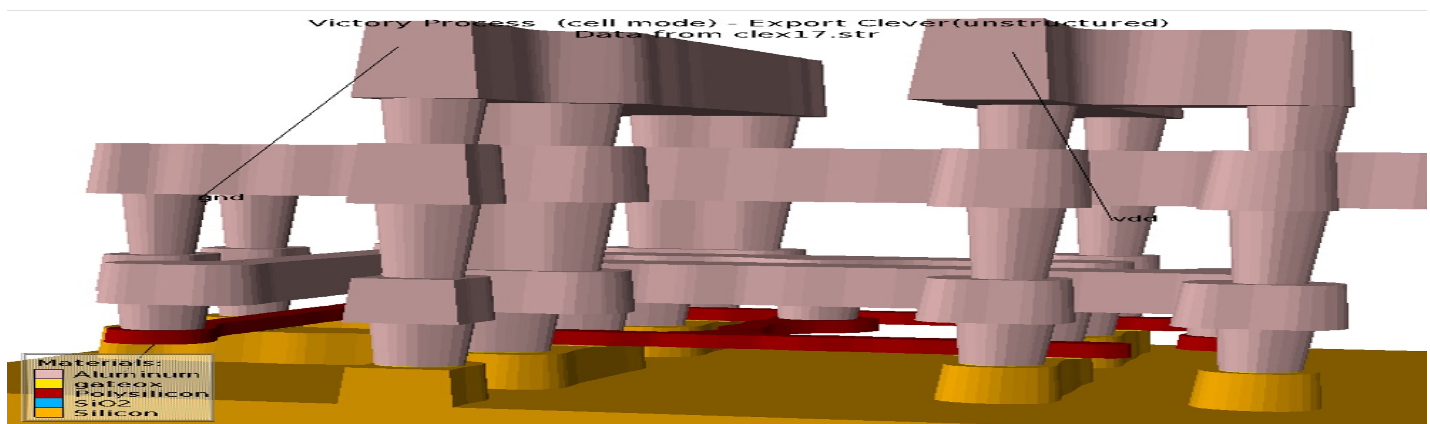
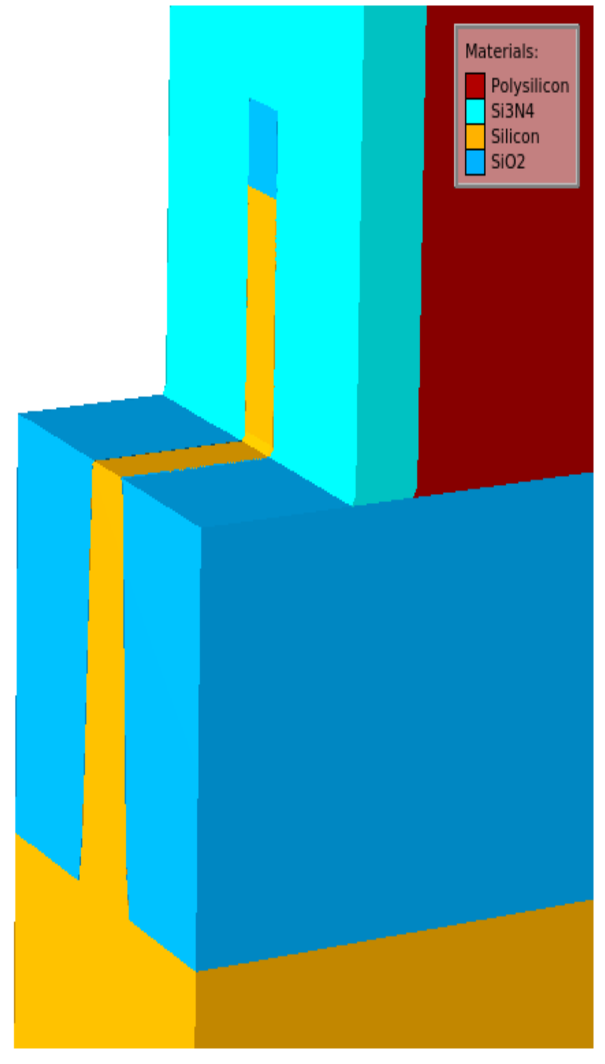
Exploring The Digital Twin Concept

- TCAD Process simulation virtualizes manufacturing
- Virtualizing the manufacturing process allows organizations to maintain a "digital twin" of their semiconductor process
- Accurate digital twins can focus on predictive power rather than on real time monitoring





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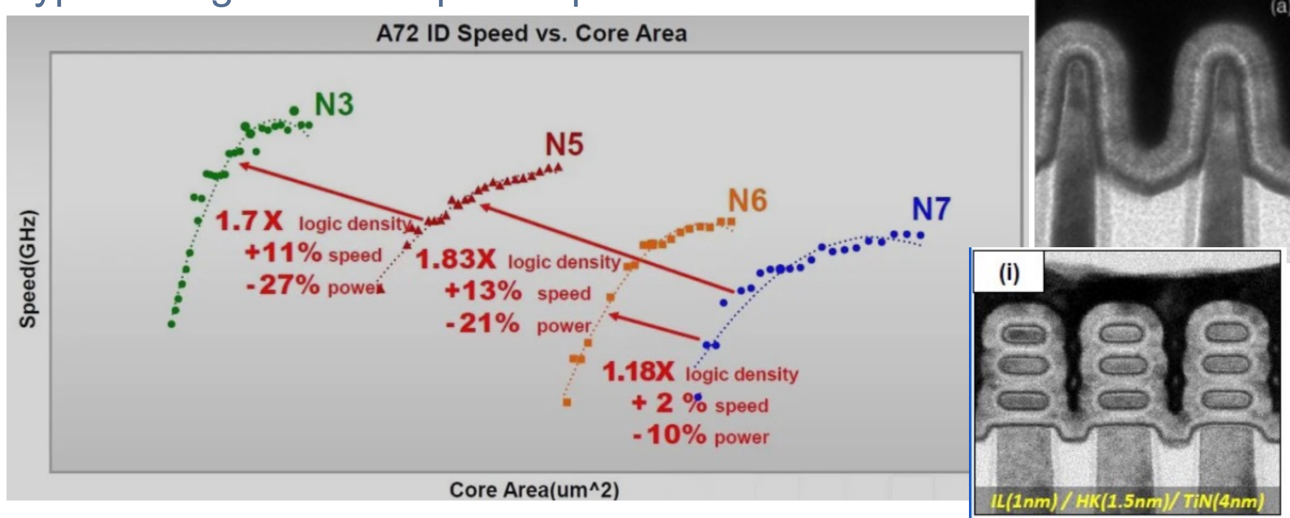
Digital Twin for Circuit Optimization

Chip Level Performance (Real World)

Typical diagram for chip level performance PPA



Chip level Performance-Area benchmark requires

- Accurate structures
- Device characteristics
- Parasitic component extraction
- Spice model parameter from device sim
- Layout editor, tools…

Performance

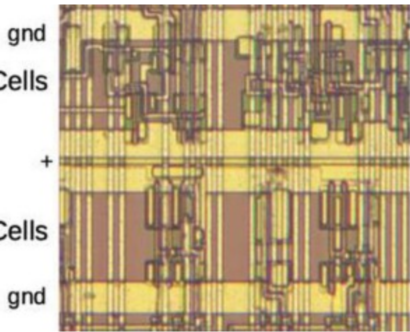
Chip speed is driven by

- transistor performance
- parasitic capacitance
- resistance

Area

Chip area is driven by

- transistor technology (FinFET, NW)
- standard cell architecture (PN ratio, Vdd/Vss scheme)



Power

- …

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Digital Twin for Circuit Optimization

Chip Level Performance (Virtual World)

Simulation methodology for developing new technologies considering how technology (process and device design) impacts circuit performance

Expert
Layout

Silvaco TCAD
Process Emulation
Process
Device

Clever
Parasitic Extraction

SmartSPICE
Spice

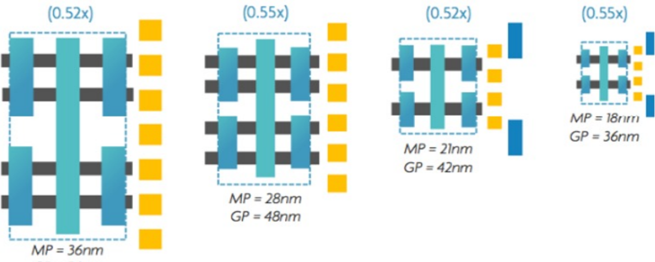
Spice Modeling
Utmost IV

Advanced Transport
Material Modeling Ab Initio
Victory Atomistic

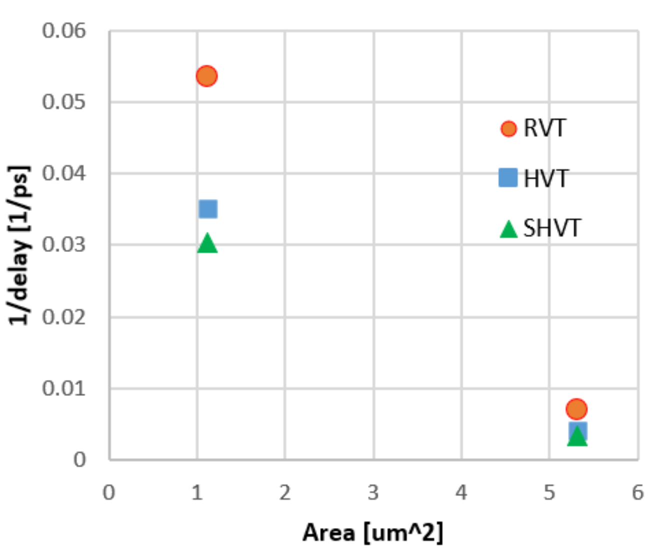
FinFET

Nano Sheet

RCx



Various standard cell architectures



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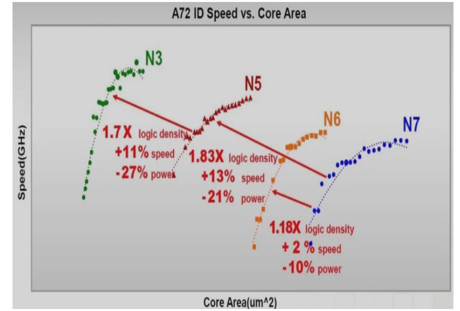
Digital Twin for Circuit Optimization

Chip Level Performance

Real World



Optimized Sampling & Data Generation

DoE design

TCAD

Digital Twin

FAB

Data analysis, Data mining, visualization

Supervised ML for Nonlinear Modeling

Until Good Model

Good Model

Model-based Optimization

Virtual World

Area-Performance

RVT
HVT
SHVT

1/delay [1/ps]

Area [um^2]

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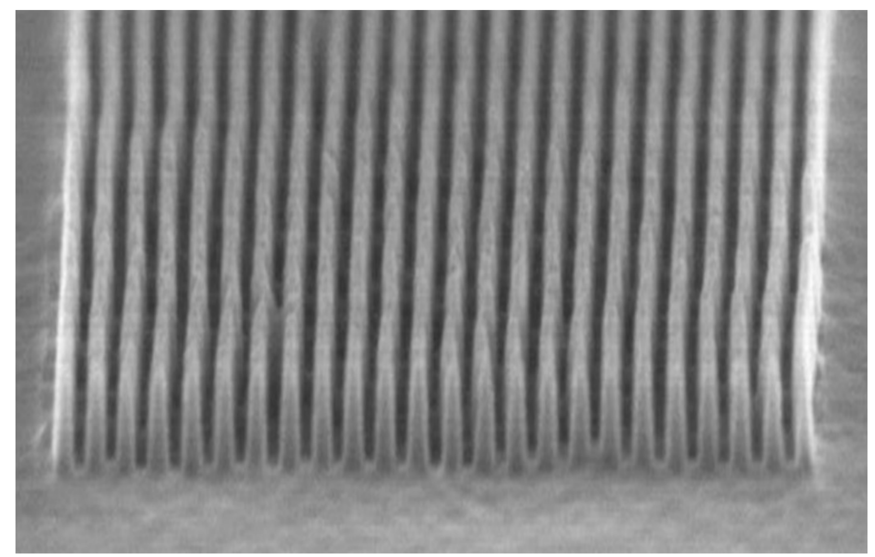
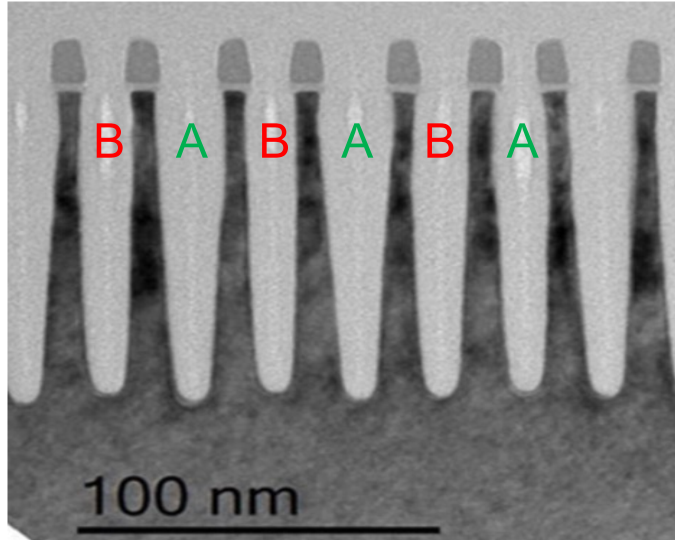
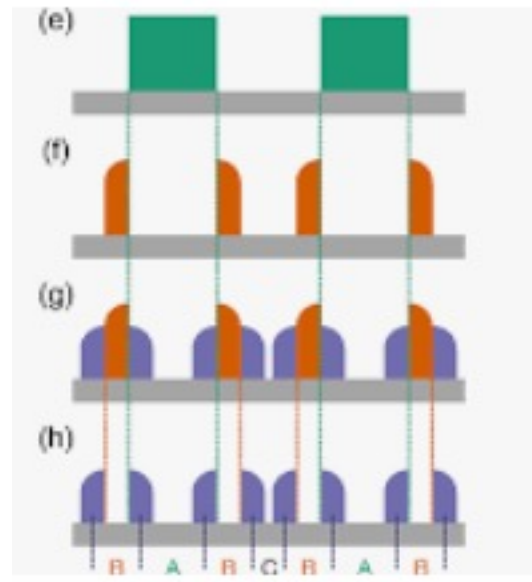
Digital Twin for Process Optimization

FinFET Fin Process (Real World)







Pitch Walking, space between Fins is uneven (A>B)

Process control of FIN module is daunting task

- Previous process steps strongly influence the shape of the fin
- FIN etch chamber physics changes the fin profile
- Total number of process variables is massive (from litho uniformity to chamber conditions)
- Interactions between process conditions play a big role

Foundries must understand the root cause of Pitch Walking (A B) and Critical Dimension (CD) uniformity issue throughout the process flow

➔ Need very accurate process simulation combined with statistical analysis

	Target	delta
Fin CD	10 nm	5%
Fin Height	90 nm	4%
Pitch Walking	4 nm	4%
Last Fin Fat	2 nm	6%

Typical Fin module control parameter

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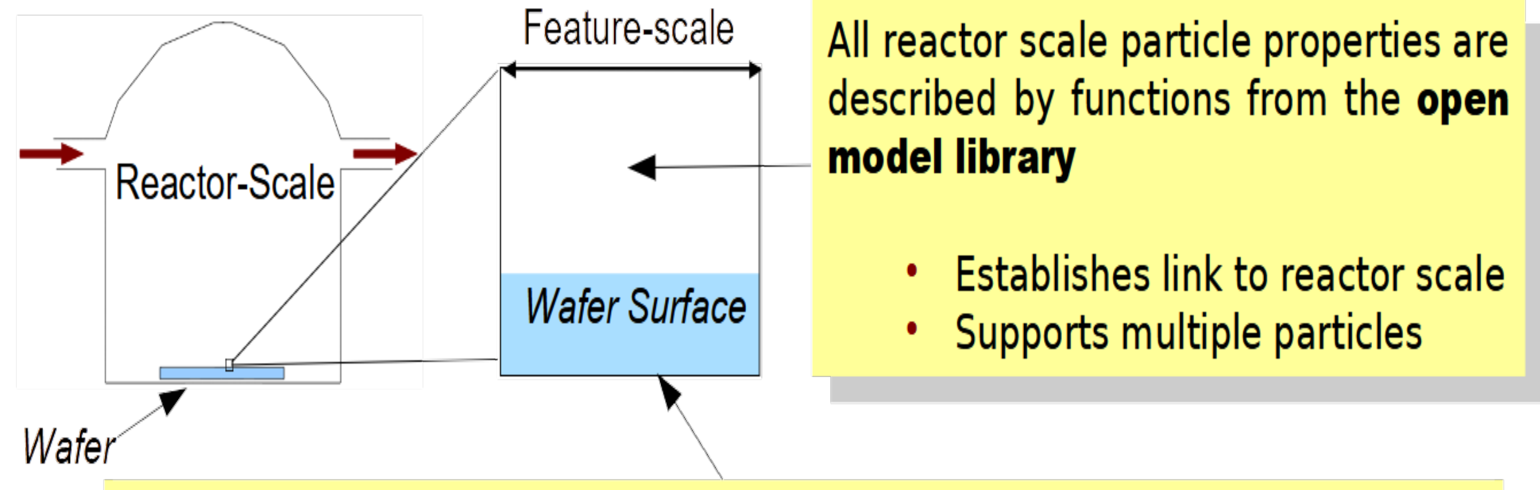
Digital Twin for Process Optimization

Fin Process Flow Simulation, Etch Chamber Model (Virtual word)

- Process simulation solutions offer a hierarchy of models going from solid modelling-based structure generation towards considering physical details of processes used when manufacturing devices
- Equipment properties are included in the simulation, including transport of particles from the reactor into the feature scale domain



Self Aligned Quadruple Patterning SAQP process flow

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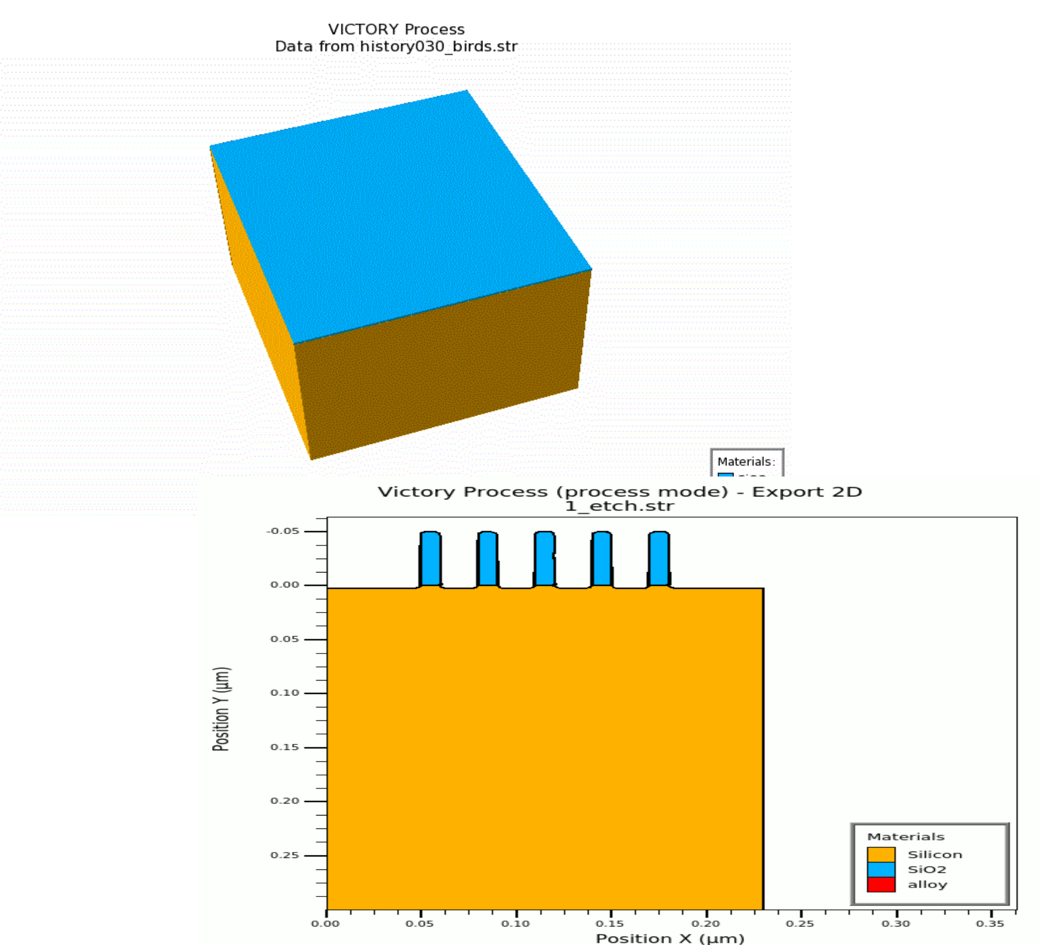
Digital Twin for Process Optimization

Fin Process Flow Simulation (Virtual word)

Simulation structures based on the Self Aligned Quadruple Patterning SAQP process flow



The shape of the FIN is driven by complex physical phenomena

- Selectivity of the materials w.r.t plasma
- Plasma flux distribution
- Polymer formation during the etch process
- Loading effect (Dense vs Open area)

Animation:

- Etch chamber modulate neutral and ion flux
- Chemical reaction create polymer at the sidewall enhancing vertical profile
- Large open area receive more etchant undergoing deeper etch
- Thickness of polymer at last fin is thicker making last fin fatter

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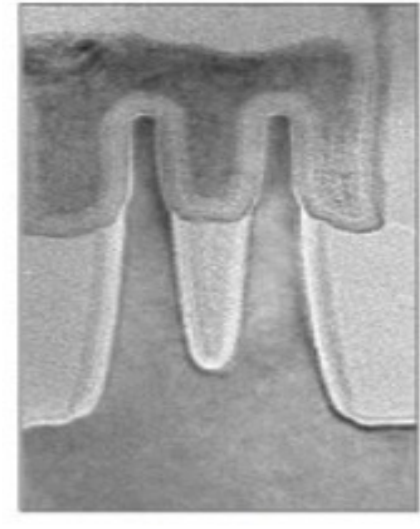
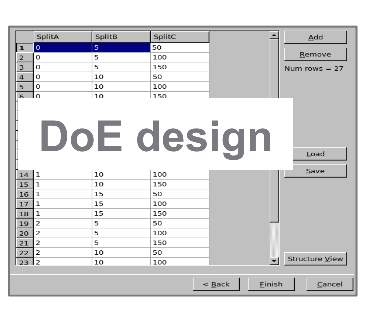
Digital Twin for Process Optimization

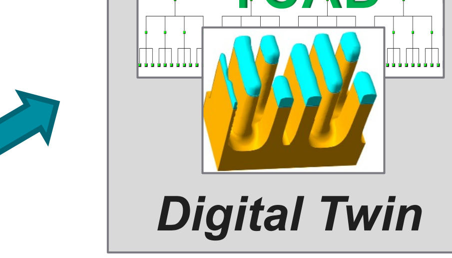
Digital Twin of the Fin Process

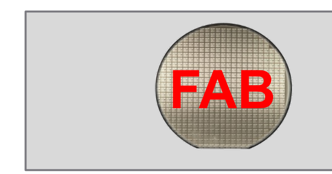
Real World



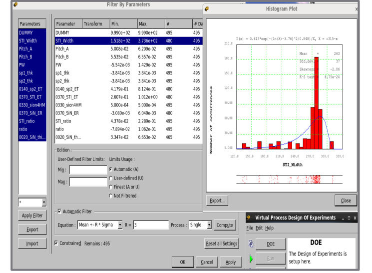
Optimized Sampling & Data Generation

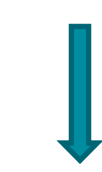






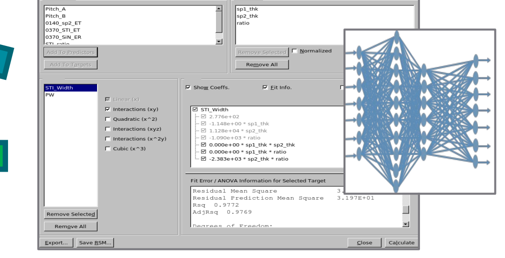
Data analysis, Data mining, visualization





Virtual World

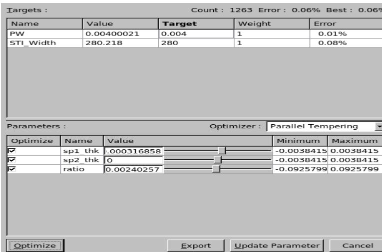
Supervised ML for Nonlinear Modeling



Until Good Model

Good Model

Model-based Optimization



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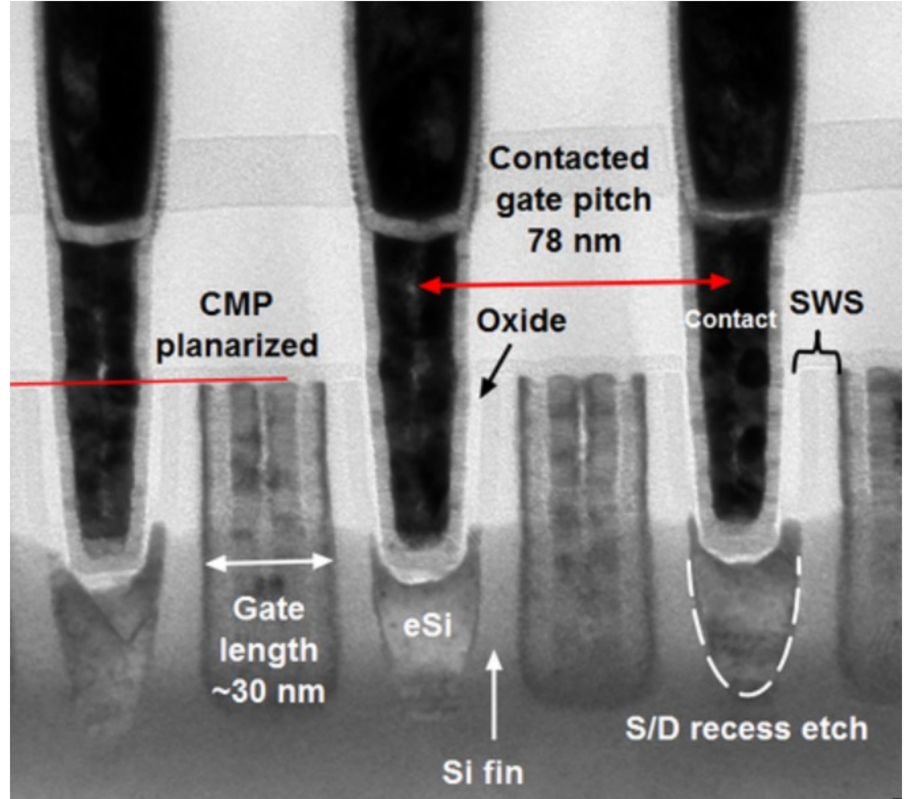
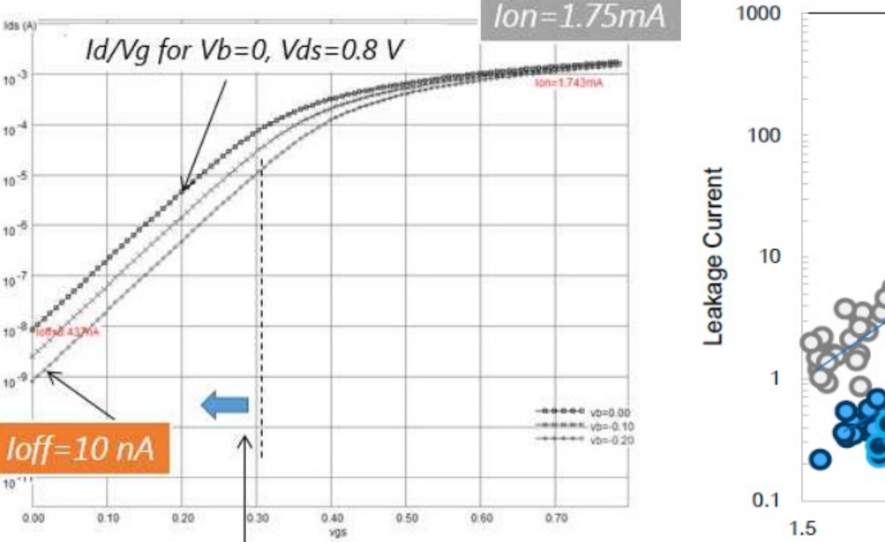
Digital Twin for Device Optimization

FinFET Electrical Characteristics (Real World)

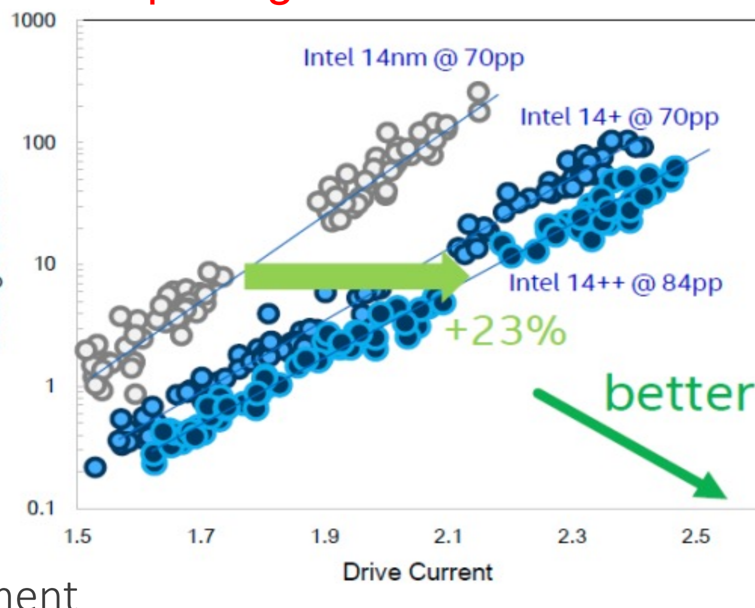
Step1: FinFET structure



Step2: Individual Tr. characteristics



Step3: Figure of Merit



FINFET device performance improvement

- Many factors influence transistor dc characteristics
  - Channel length, Fin width, Vth/Well implantation, contact resistance, High-K characteristics etc.
- Transistor performance is gauged by figure of merit, which contains variation sources
- Accurate physics based TCAD device solver is required

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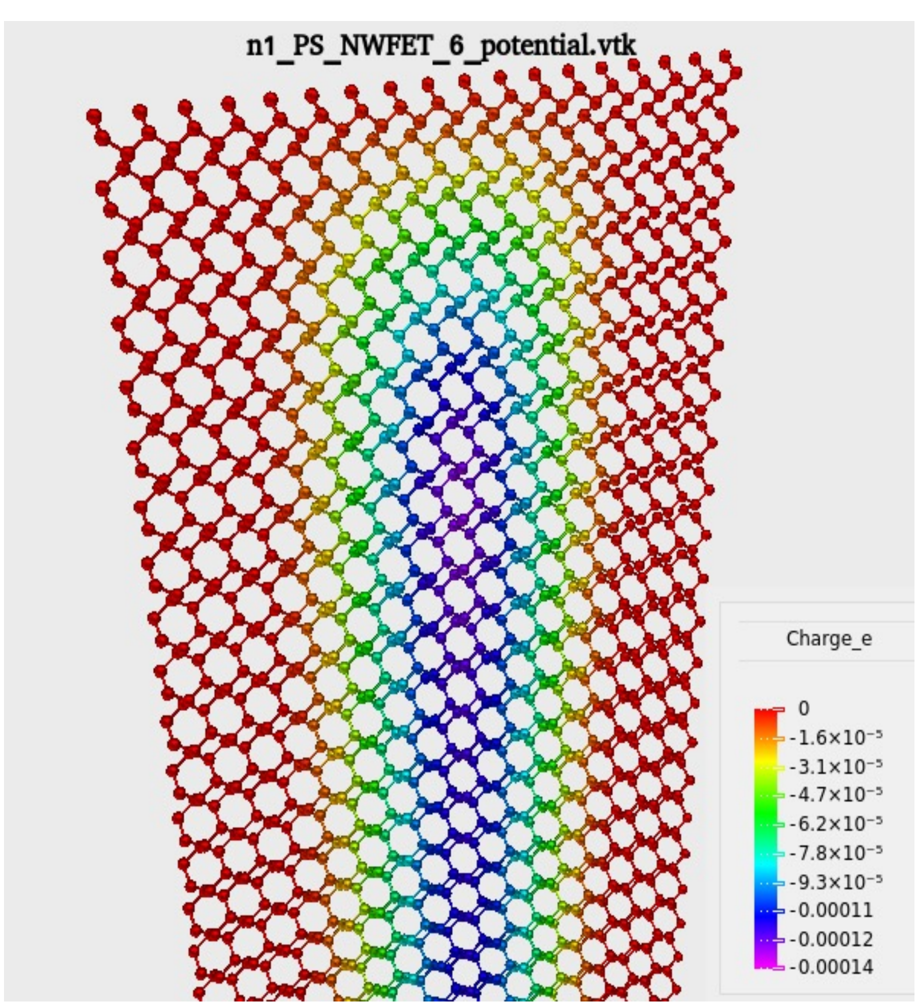
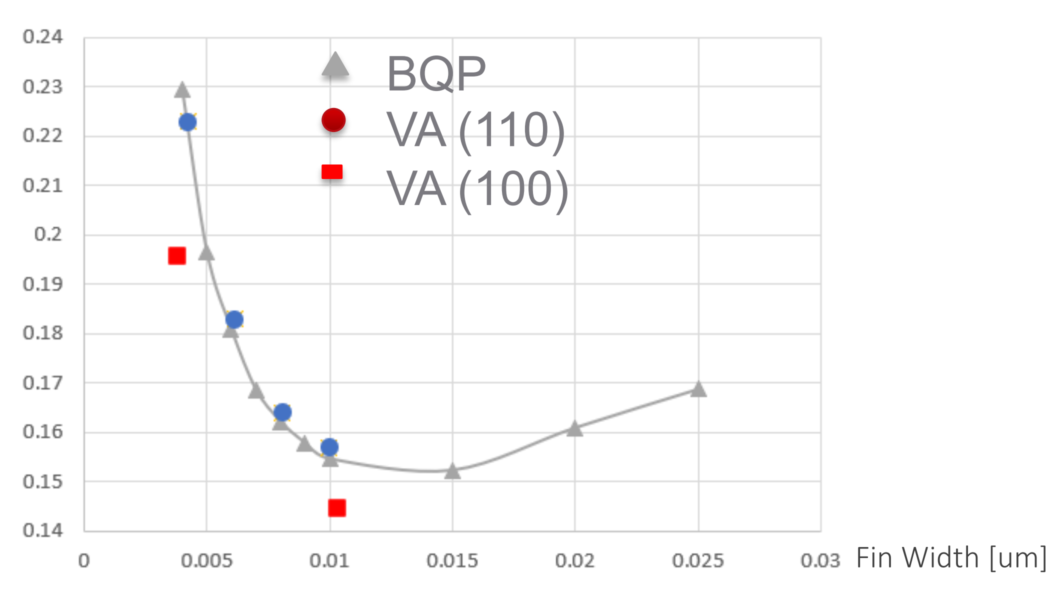
Digital Twin for Device Optimization

FinFET Electrical Characteristics: Atomistic Simulation (Virtual World)





FINFET device characteristics by atomistic simulation

- As FinFET width is decreasing, the threshold voltage is increased
- Mechanism known as quantum confinement effect
- Atomistic simulation provides accurate model
- Fin surface orientation changes quantum effect ➔ Important factor for gate around transistor optimization

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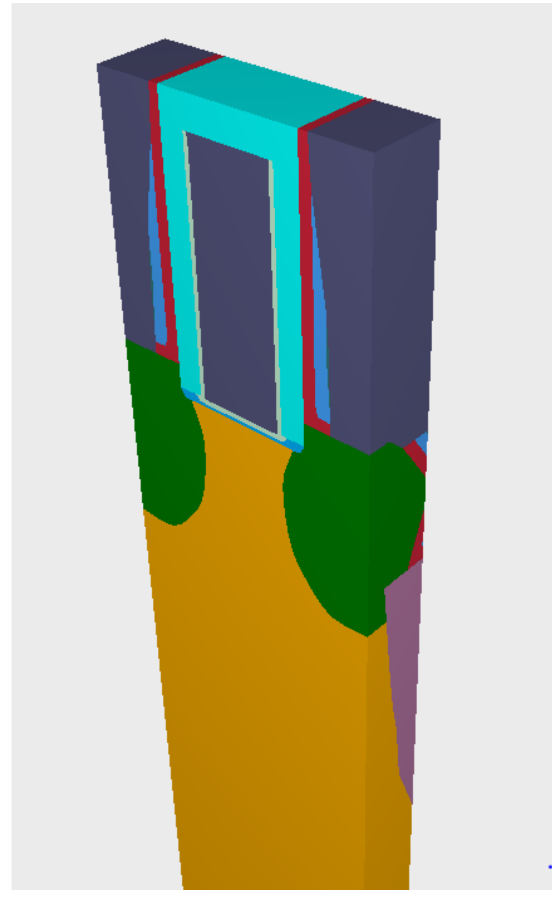
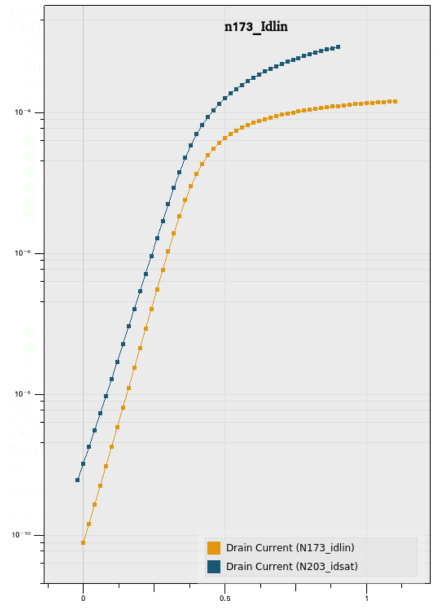
Digital Twin for Device Optimization

FinFET Electrical Characteristics: TCAD Simulation Flow (Virtual World)

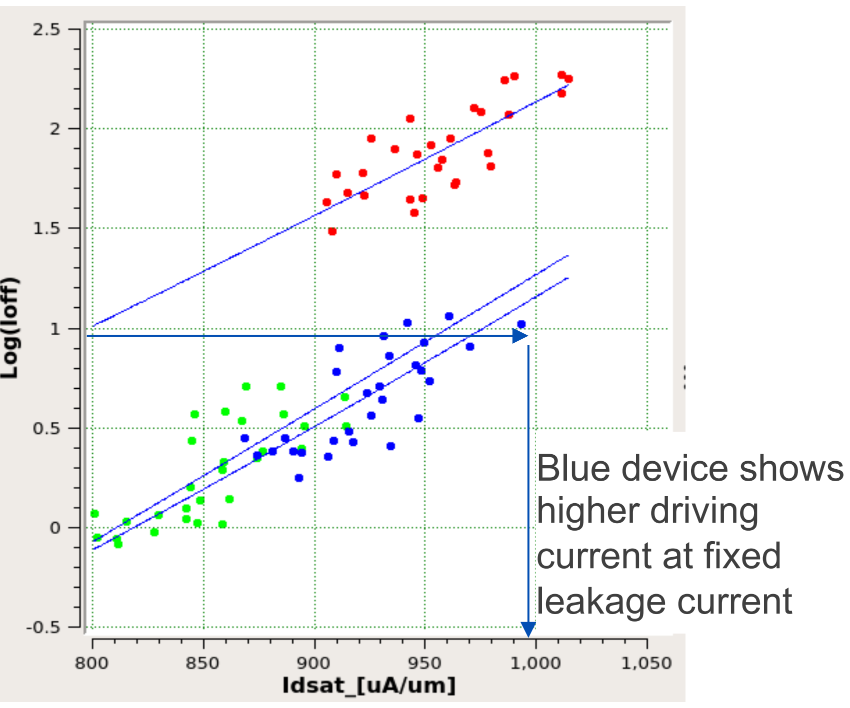
Step1:FinFET structure



Step2: Individual Tr. Characteristics



Step3: Figure of Merit



FINFET device structure & device characteristics

- Victory Process for structure build
- Victory Device for device characterization
- Variation aware process/device simulation for extracting figure of merit

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Digital Twin for Device Optimization

Digital Twin of FinFET Electrical Characteristics

Real World

Optimized Sampling & Data Generation

DoE design

TCAD

Digital Twin

FAB

Data analysis, Data mining, visualization

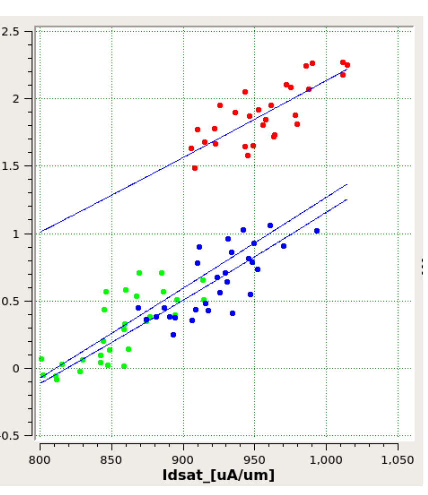
Supervised ML for Nonlinear Modeling

Model-based Optimization

Until Good Model

Good Model

Virtual World



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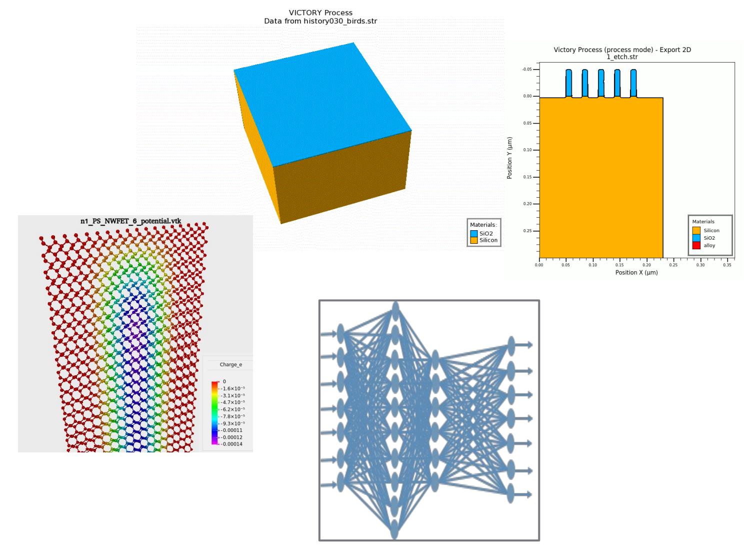
Digital Twin Foundations

- A strong foundation is the key for an accurate digital twin
  - Accurate process structure simulation
  - Physics based process model
  - Atomic level device simulation
  - ML based data analytics
- Compute power is here
- Secretive industry Equipment ⇔ Fab ⇔ EDA ⇔ Design
- TCAD growing faster than industry overall, enables Virtual Fab



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