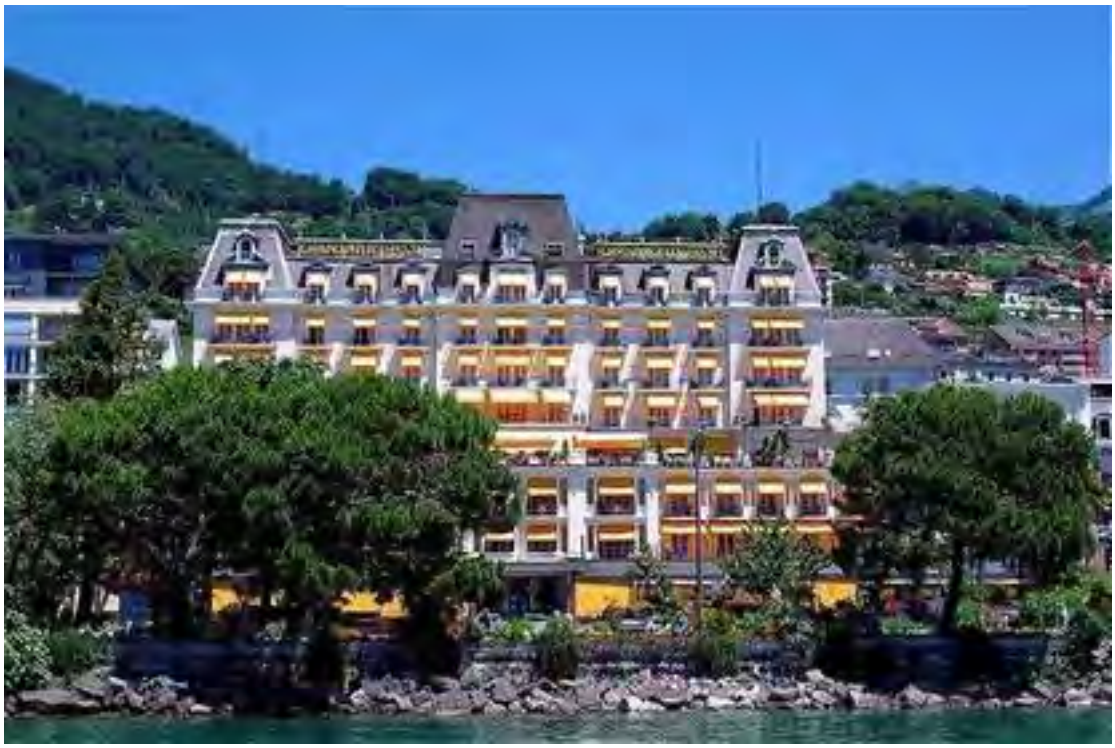
# Emerging technologies and applications

## The elephants in the technology room



Suisse Majestic Hotel
Montreux

April 20-21, 2023

# Emerging technologies and applications: the elephants in the technology room

**A free-exchange technical symposium**

# Emerging technologies and applications: the elephants in the technology room

## Welcome

We are very glad and honored to welcome you to this Symposium that has the purpose to discuss some important topics in electronic systems and their design.

First and foremost, the Symposium will address the future of free technical exchange as a means to support the design and the manufacturing of complex systems whose suppliers and customers are spread around the world. In particular, any restriction in the supply chain – which includes raw materials, manufacturing equipment, and software tools - will limit the prevalence of computing and communication systems worldwide with a negative effect on the world economy. These restrictions are currently being used as geopolitical weapons and are already impacting the ability of many companies to conduct their business abroad.

Next, the symposium will address two upcoming changes of paradigms: the introduction of quantum computing and the holistic application of safety, security, and privacy in computing. Within the former domain, it will be important to arrive at a comprehensive design methodology for quantum computing systems, as much as possible independent of their physical implementation, because all *ad hoc* solutions - reminiscent of "pre-4004" processors and "pre-Mead&Conway" integrated circuits - are likely not to be scalable. Moreover, even more critical, such implementations will pose serious accessibility limitations for small, medium businesses and academic institutions.

In the latter area, it will be important to realize that security, safety and privacy must be addressed as a single entity, thus a new design goal will be to find the appropriate balance for these metrics in new systems design, bearing in mind that an increasing number of mission- and life-critical systems are being deployed within our bodies, homes, and cities, and that personal data are often the currency of exchange for many popular apps.

The second day of the symposium will feature a discussion on the Metaverse of Things (MoT), as a revolutionary evolution of the broad paradigm and market of the Internet of Things (IoT). Indeed, it is the opinion of the organizers that a huge space for innovation relates to applying the metaverse concept to smart objects, ranging from cars, to homes, to cities and infrastructures, that need to work in global consonance, and need to be trained in this direction.

Finally, the symposium will feature a discussion on the technologies for the upcoming decade, ranging from devices, to technologies and manufacturing issues, in the wake of the nanometer CMOS innovation stalemate. Indeed, SRAM bit-cells, once utilized as a proxy of process node integration capabilities, are, by now, about 10X bigger than they should be according to Moore's law. The interaction between these emerging technologies and the evolution of both von Neumann and non-von Neumann computing architectures will close the symposium.

We are grateful to EPFL and Synopsys for the generous support that has made this Symposium possible. We warmly thank Chantal Demont, and the Suisse Majestic Hotel staff for the arrangements.

Giovanni De Micheli
LSI, EPFL

Marco Casale-Rossi
Synopsys

**Emerging technologies and applications – the elephants in the technology room**
**Thursday, April 20, 2023**

**8:15 Welcome (Giovanni De Micheli, EPFL and Marco Casale-Rossi, Synopsys)**

**The future of free technical exchange (Chair: Giovanni De Micheli, EPFL)**

**8:30 – 9:15 Keynote: Alberto Sangiovanni-Vincentelli, UC Berkeley**: Back to the future: is the electronics industry moving away from the present disaggregation?

**9:15 - 10:00 Keynote: Joachim Kunkel, Synopsys:** The changing landscape of the semiconductor industry

**10:00 – 10:30 Coffee break**

**Quantum Computing (Chair: Giovanni De Micheli, EPFL)**

**10:30 - 11:15 Keynote: Jason Cong, UCLA**: Layout Synthesis and Architecture Customization for Quantum Computing

**11:15 – 12:30 Panel. How will QC be designed? Chair: Robert Wille, T.U. Munich**

Panelists:
Luca Amaru, Synopsys
Edoardo Charbon, EPFL
Thomas Haener, Amazon
Mathias Soeken, Microsoft
Andrei Vladimirescu, U.C. Berkeley

**12:30 – 14:00 Lunch**

**Safety, security, privacy (Chair: Marco Casale-Rossi, Synopsys)**

**14:00 – 14:45 Keynote: Mike Borza, Synopsys:** Having Our Cake and Eating It Too: Are Safety, Security and Privacy Possible Simultaneously?

**14:45 – 15:30 Keynote: Ingrid Verbauwede, KU Leuven:** Hardware: an essential partner to cryptography

**15:30 – 16:00 Coffee Break**

**16:00 – 17:15 Panel: Will information security be a reality for everyone? Chair: Wayne Burleson, U.M. Amherst**

Panelists:
Lejla Batina, Radboud University
Rajesh Gupta, U.C. San Diego
Farinaz Koushanfar, U.C. San Diego
Alena Simalatsar, HES-SO, Sion
Yankin Tanurhan, Synopsys
Marilyn Wolf, U.N. Lincoln

**19:00 -- 20:00 Cocktail**
**20:00 – 23:00 Dinner**
**22:00 – 22:30 Dinner Keynote: Patrick Groeneveld, Cerebras:** Sustainable innovation: Are we not fooling ourselves?

**Emerging technologies and applications – the elephants in the technology room**
**Friday, April 21, 2023**

**The metaverse of things: the future of IoT in a global context (Chair Marco Casale-Rossi)**

**8:30 – 9:15 Keynote: Jan Rabaey, UC Berkeley:** The Mirror World – The Land between the Meta- and the Omniverse

**9:15 – 10:00 Keynote: Alessandro Cremonesi, STMicroelectronics:** The *beauty* of being the "Enabler of the Future"

**10:00 – 10:30 Coffee break**

**10:30 – 11:45 Panel: Humans vs. things on the metaverse. Chair: Jamil Kawa, Synopsys**

Panelists:
David Atienza, EPFL
Joseph Friedman, U.T. Austin
Victor Grimblatt, Synopsys
Jan Rabaey, U.C. Berkeley
Tajana Simunic, U.C. San Diego

**11:45 – 12:30 Keynote: Tibor Mérey, Boston Consulting Group**: How the Metaverse will Remake your Strategy.

**12:30 – 14:00 Lunch**

**Technology of the 30s (Chair Giovanni De Micheli)**

**14:00 – 14:45 Keynote: Raul Camposano, Silvaco** – TCAD Digital Twins for semiconductor manufacturing

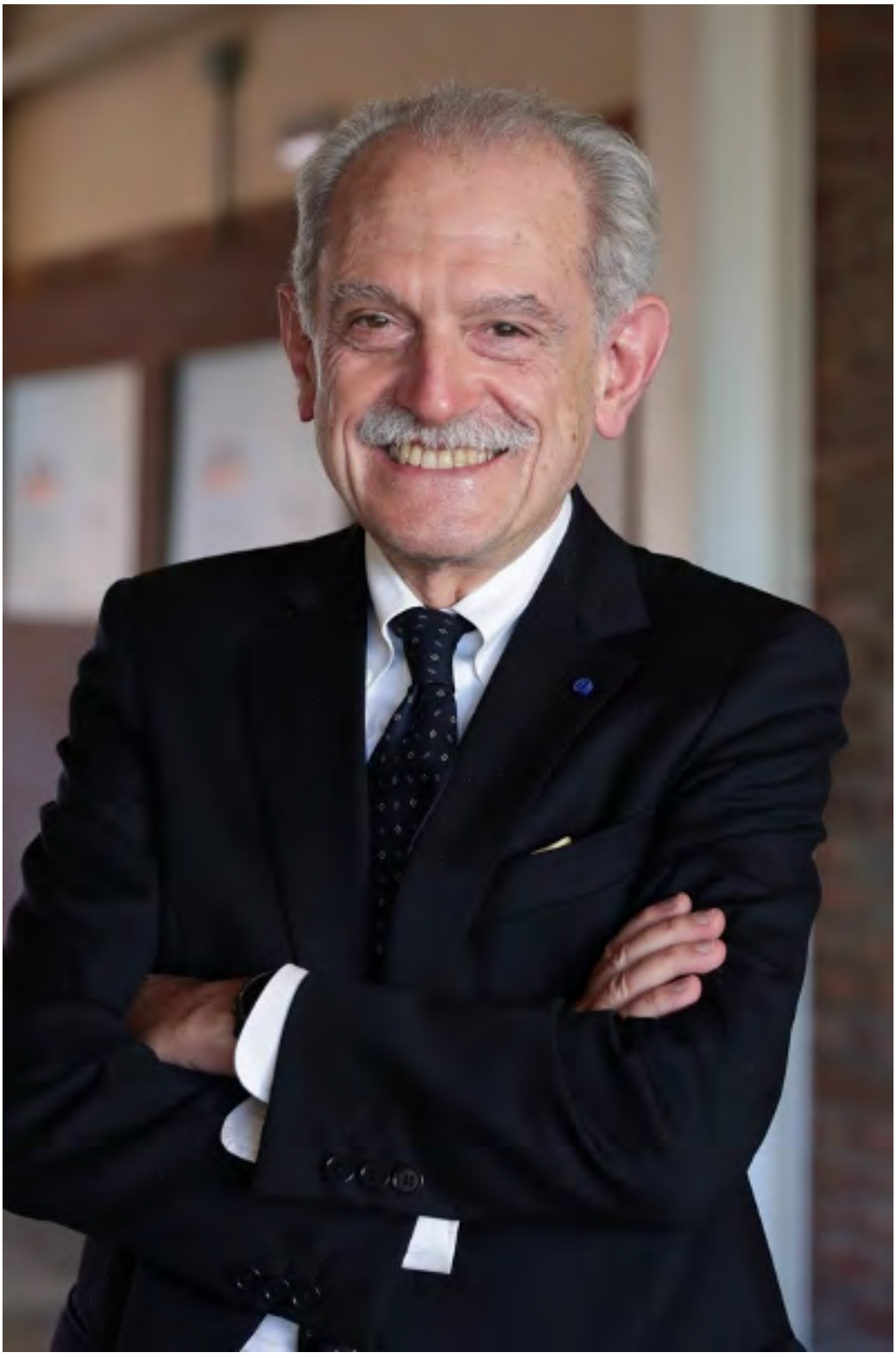
**14:45 – 15:30 Keynote: Subhasish Mitra, Stanford University** – The Future of Hardware Technologies for computing

**15:30 – 16:00 Coffee Break**

**16:00 – 17:15 Panel: Is In-Memory computing a niche area or the main hardware platform for AI/ML? Chair: Luca Benini, ETHZ**

Panelists:
Pierre-Emmanuel Gaillardon, University of Utah
Patrick Groeneweld, Cerebras
Daniele Ielmini, Politecnico di Milano
Shahar Kvatinsky, Technion
Amrita Mathuria, Kepler Computing
Abu Sebastian, IBM Research, Zurich

**Alberto Sangiovanni-Vincentelli**
UC Berkeley



**Back to the future:**
**Is the electronics industry moving away from the present disaggregation?**

Alberto Sangiovanni Vincentelli
The Edgar L. And Harold H. Buttner Chair of EECS
University of California, Berkeley

**Abstract :**

In the early days of integrated circuits, most system companies such as IBM, ATT, GTE, GE, RCA, Hughes, CDC, and Rockwell, designed and manufactured the integrated circuits that were needed in their systems claiming that this approach gave them a competitive advantage. Large Japan companies did the same (Hitachi, Fujitsu, NEC, Toshiba, Mitsubishi). IBM was indeed the largest producer of integrated circuits in the world. In addition, all these vertically integrated companies had a significant effort in computer aided design to speed up the design process of electronics. In parallel, the birth of silicon valley created a rich ecosystem of companies that were based on the design and manufacture of just semiconductors, offered an option of buying components that were better performing that the internal designs. In the 1980s and 1990s, most of the system companies in US abandoned the manufacturing of semiconductors, IBM being the last one to resist before selling his operation to Global Foundries. Since the 1990s, even semiconductor companies have shed their manufacturing operations because of the emergence of pure foundries such as TSMC and eventually Global Foundries. For example, AMD sold its manufacturing plants to Global Foundries. In parallel, internal CAD group shrunk considerable because of the emergence of the EDA industry yielding a massive disintegration of the electronics system industry. Fast forward to now, when the premier system companies started designing their own chips. Tesla, Apple, Amazon and Google for example, have developed impressive processing units that rival with off the shelf components provided by the integrated circuit companies. Will this trend continue to the point of these dominant companies setting up a manufacturing plant? Will the geopolitical situation have an impact on this trend? Is this sound or will make the entire industry go through inefficiencies and trade wars?

**Speaker Bio :**

Alberto Sangiovanni Vincentelli is the Edgar L. and Harold H. Buttner Chair of Electrical Engineering and Computer Sciences at the University of California at Berkeley. He is an author of over 1000 papers, 17 books and 2 patents. He was a co-founder of Cadence and Synopsys, the two leading companies in the area of Electronic Design Automation. He was a consultant or member of the Advisory Boards of several companies such as BMW, Mercedes, Magneti Marelli, Intel, ST microelectronics, HP, General Motors, United Technologies, Lutron, Lendlease and Elettronica. Currently, he is a member of the following boards: Cadence, KPIT, eGap, Exein, Cy4Gate and Chairperson of Quantum Motion, Innatera, Phoelex, e4Life and Phononic Vibes. From January 2013 to 2016, he was the President of the Strategic Committee of the Italian Strategic Fund. He was member of the Scientific Council of the Italian National Science Foundation from 2001 to 2015. From February 2010 to December 2020, he had been a member of the Executive Committee of the Italian Institute of Technology, where he is now a member of the Technical Scientific Committee. From July 2012 to July 2015, he was Chairperson of the Comitato Nazionale Garanti per la Ricerca. He is the Chairperson of the Strategy Board and of the International advisory Board of the Milano Innovation District (MIND). He is the recipient of several academic honors, including the IEEE/RSE Wolfson James Clerk Maxwell Medal *"for groundbreaking contributions that have had an exceptional impact on the development of electronics and electrical engineering or related fields* and the Kaufman EDA Award. He was awarded four Honorary Doctorates (Aalborg, KTH, AGH and University of Rome 2).

**Joachim Kunkel**

Synopsys

**The changing landscape of the semiconductor industry**

Joachim Kunkel
General Manager of the Solutions Group
Synopsys

**Abstract :**
The development and manufacturing of semiconductors takes advantage of a complex, finely tuned, global, mostly Asia based, supply chain that evolved over time towards maximum efficiency. When COVID-19 hit in 2020, many device and system companies experienced severe semiconductor supply shortages, preventing them from completing and shipping their products. The security of semiconductor supply had been taken for granted by these companies and there was no plan B. Vis a vis the nonexistent resilience of the global semiconductor supply chain and the perceived prioritization of national interests by suppliers and consumers of semiconductors, calls to onshore semiconductor manufacturing were quick to follow. Add to this the increasing geopolitical concerns related to where a large portion of semiconductors are manufactured today and the calls to onshore semiconductor manufacturing have only become louder. This talk will examine the growing economic relevance of semiconductors and how the need for supply security is changing the semiconductor manufacturing landscape.

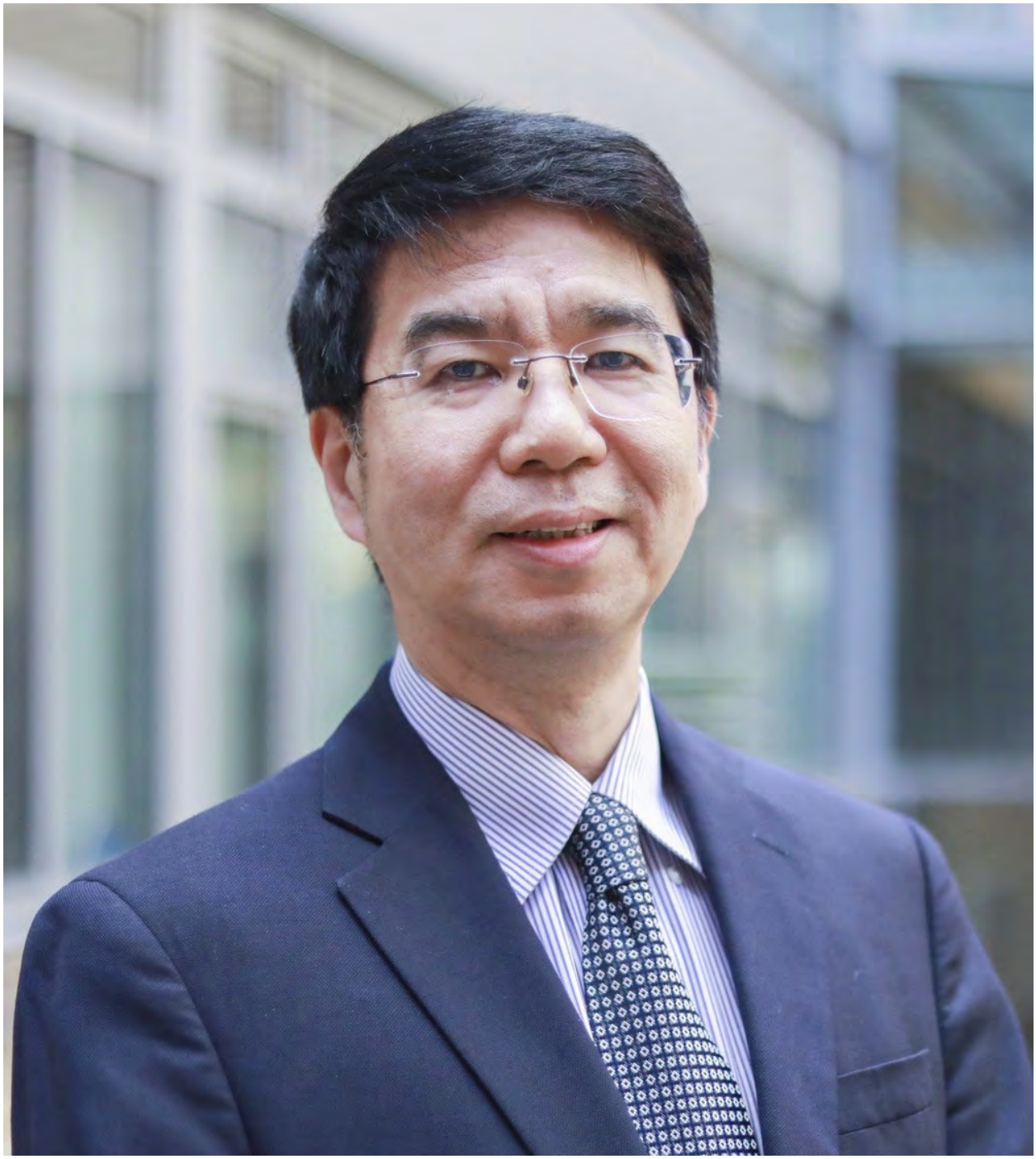
**Speaker Bio :**
Joachim Kunkel has served as the General Manager of the Solutions Group at Synopsys since October 2006, responsible for Synopsys' DesignWare® intellectual property (IP) products. Previously he served in a number of senior positions at Synopsys including Vice President of Engineering of the Solutions Group, Vice President of Marketing of IP and Design, and Vice President and General Manager of System-Level Design.

Prior to joining Synopsys in 1994, Mr. Kunkel was a managing director of CADIS GmbH, a company he had co-founded in 1989 in Aachen, Germany, focused on the development of system-level design tools for digital signal processing and providing specialized design services for digital wireless communication systems.

Mr. Kunkel holds an M.S. in Electrical Engineering from the Aachen University of Technology.

**Jason Cong**

UCLA



**Layout Synthesis and Architecture Customization for Quantum Computing**

Jason Cong
UCLA Computer Science Department
Director, Center for Domain-Specific Computing (CDSC)
http://vast.cs.ucla.edu/people/faculty/jason-cong

**Abstract :**

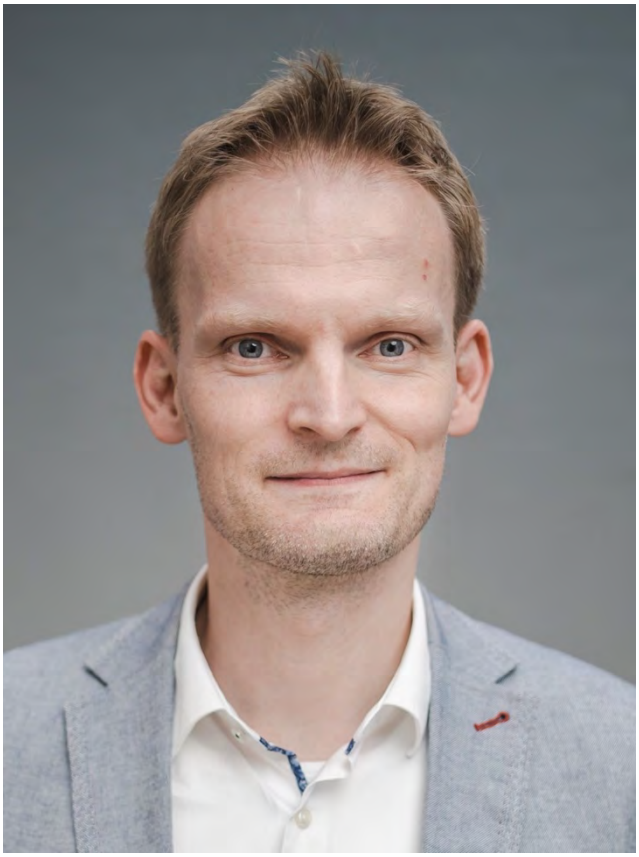
How does the mapping of logical variables in a quantum algorithm to physical qubits on a quantum device affect overall performance? As quantum computing devices continue to scale up, this question of compiling from applications to quantum devices is becoming very important. In this talk, I focus on our recent work on the qubit mapping and scheduling step. By constructing a family of quantum circuits with the known optimal mapping depths, we evaluated several leading industry and academic qubit mapping tools, including Cirq from Google, Qiskit from IBM, and t|ket> from Quantinuum. We found their performance to be surprisingly sub-optimal–by a factor of up to 45x–even on near-term feasible circuits. This motivated us to develop a tool for optimal layout synthesis for quantum computing, named OLSQ, based on a general SMT-based optimization framework. OLSQ more compactly represents the solution space with exponential reduction in computational complexity, leading to optimal mapping and scheduling solutions for currently practical quantum applications. Further speedup of OLSQ is achieved for domain-specific applications, such as quantum approximate optimization algorithm (QAOA) by exploiting gate commutation and chemical simulation with optimal swap gate absorption. We also use OLSQ for application-specific customization for NISQ-era quantum computing.

**Speaker Bio :**

JASON CONG is the Volgenau Chair for Engineering Excellence Professor at the UCLA Computer Science Department (and a former department chair), with joint appointment from the Electrical and Computer Engineering Department. He is the director of Center for Domain-Specific Computing (CDSC) and the director of VLSI Architecture, Synthesis, and Technology (VAST) Laboratory. Dr. Cong's research interests include novel architectures and compilation for customizable computing, synthesis of VLSI circuits and systems, and highly scalable algorithms. He has close to 500 publications in these areas, including 16 best paper awards, three 10-Year Most Influential Paper Awards, and three papers inducted to the FPGA and Reconfigurable Computing Hall of Fame. He and his former students co-founded AutoESL, which developed the most widely used high-level synthesis tool for FPGAs (renamed to Vivado HLS after Xilinx's acquisition). He was elected to an IEEE Fellow in 2000, ACM Fellow in 2008, the National Academy of Engineering in 2017, and the National Academy of Inventors in 2020. He is the recipient of the 2022 IEEE Robert Noyce Medal for fundamental contributions to electronic design automation and FPGA design methods.

**Panel Discussion:**
**How will Quantum Computers be designed ?**

Chair: Robert Wille
Technical University of Munich

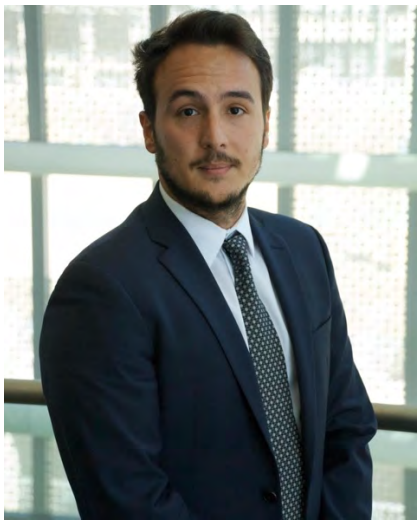


**Abstract:**

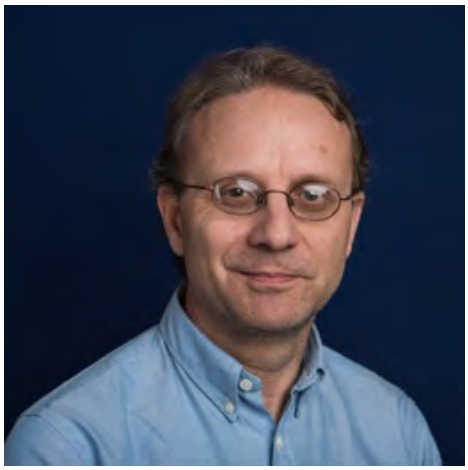
Quantum computers are a reality. And with them completely new design tasks emerged. Due to the radically different computational paradigm and physical setting, we have to re-think the design of corresponding applications and devices: How much of the established design flow for classical circuits and systems can be used for these purposes? How much has to be developed from scratch? And do we all have to become quantum physicists now? At the same time, we should be realistic about the perspective of quantum computing: Within a 10-year horizon, can we count on quantum computing to solve practically relevant problems? Do we have metrics that show the superiority over classic server farms on relevant problems? This and more will be discussed in this panel.

**Panelists**

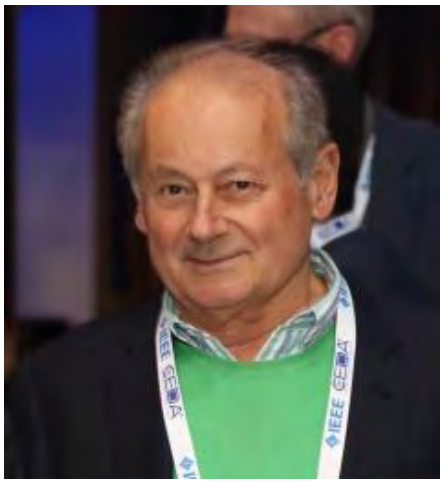
Mathias Soeken, Microsoft



Luca Amarù, Synopsys



Edoardo Charbon, EPFL

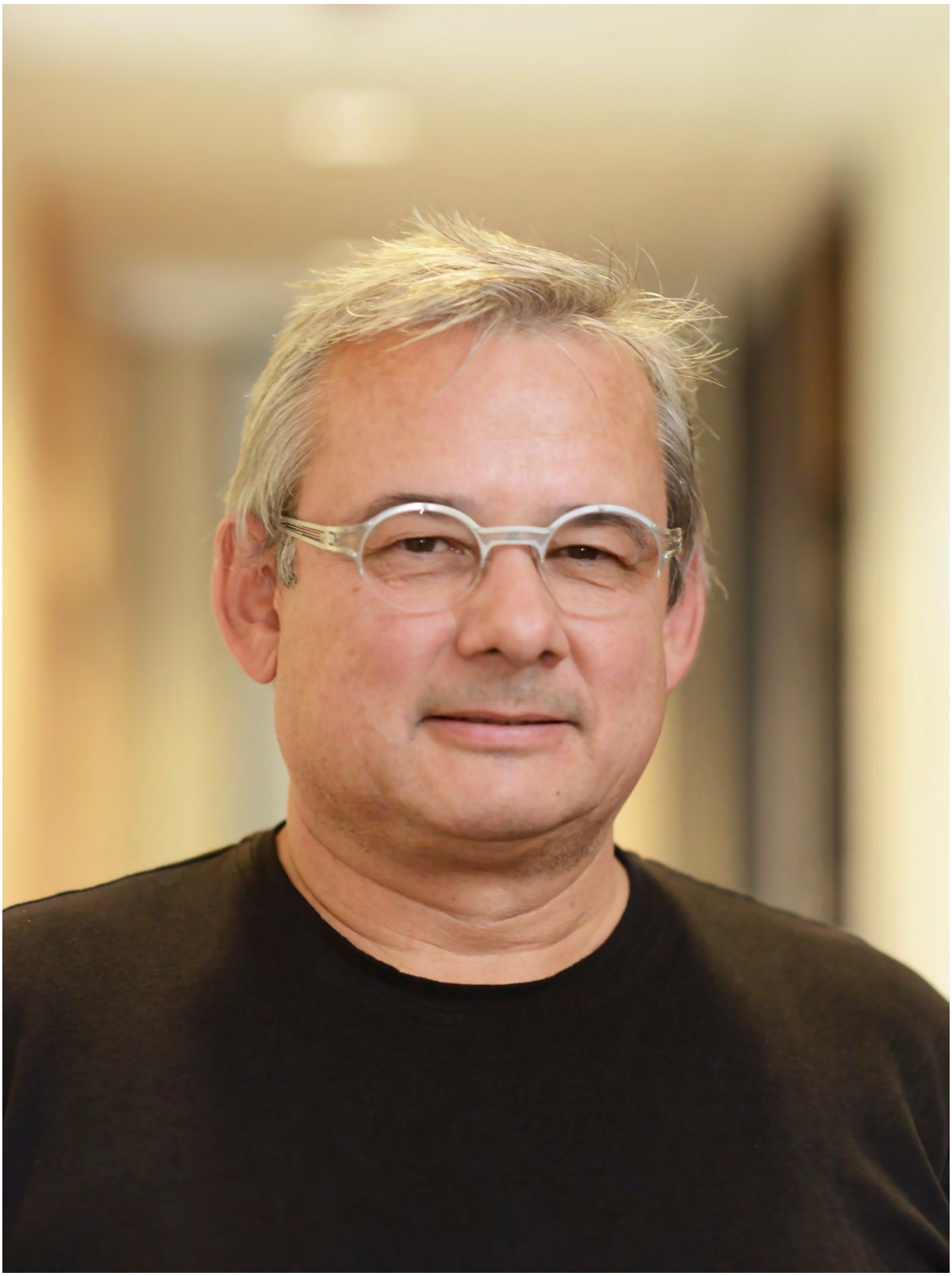


Andrei Vladimirescu, U.C. Berkeley

Thomas Haener, Amazon

**Mike Borza**

Synopsys



**Having Our Cake and Eating It Too:**
**Are Safety, Security and Privacy Possible Simultaneously ?**

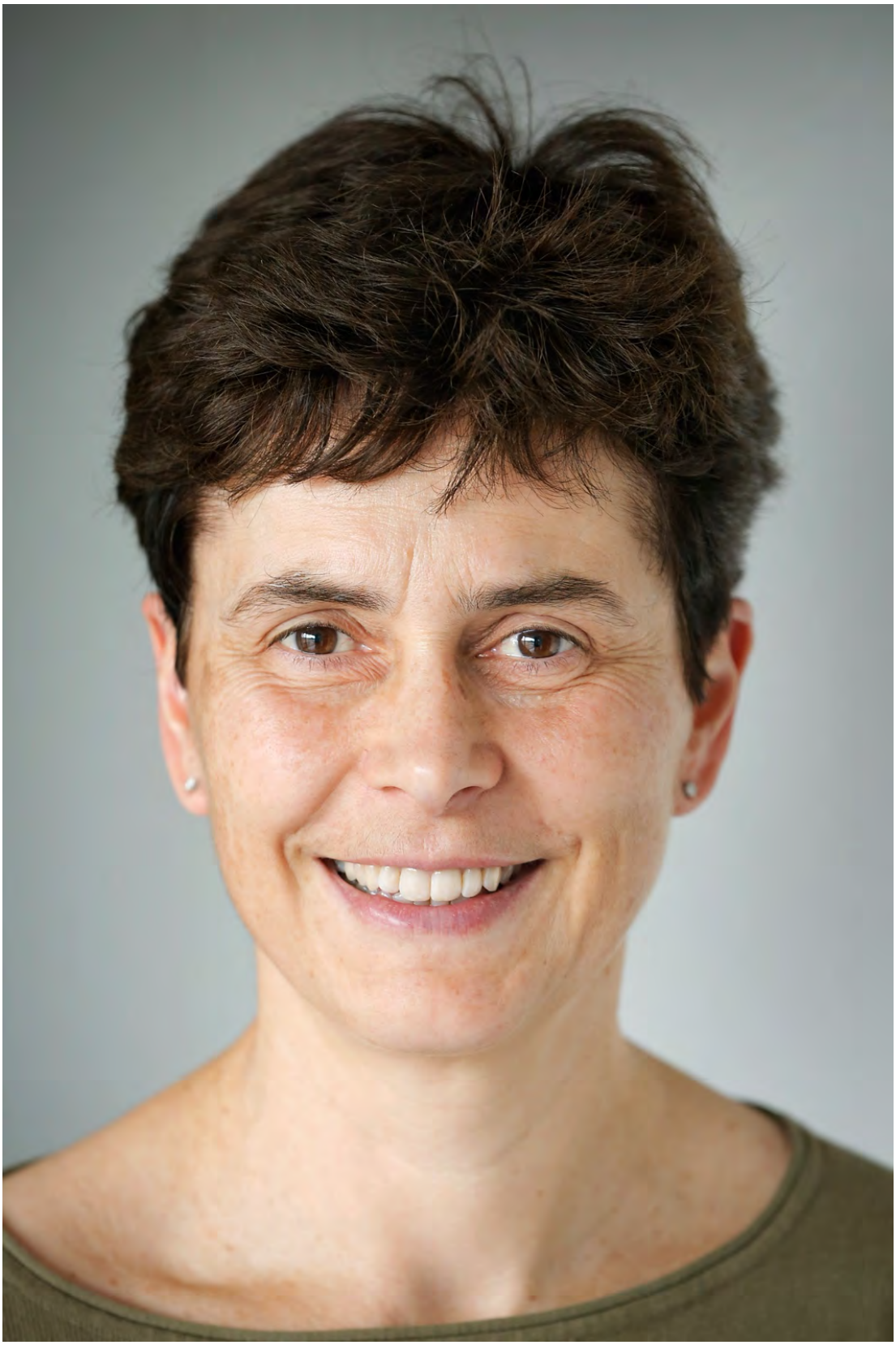
Mike Borza
Synopsys Scientist, Solutions Group
Synopsys, Inc.
https://www.synopsys.com/

**Abstract :**
Ever greater levels of computation and communication are part of the systems we use in our daily lives, and this will only accelerate as we enter the metaverse. Many of these systems have safety implications for the people who use them and for those nearby. Traditional safety systems were designed as if they operated in isolation, immune (or oblivious) to security risks from outside their boundary. We now recognize that there is no safety without security. Obvious examples include advancing automation and connectivity in automobiles, where the risks of compromised systems software represent obvious real risks to the safety of vehicle occupants, and other road users. Fortunately, practitioners in these areas are now rationalizing the sometimes opposing objectives of safety and security.

At the heart of security is the notion of strong identity immutably baked into a device during manufacturing. Often, derived and related identifiers that can be correlated to that foundational identity are used for different purposes. When this information is readily available and can be amassed as it moves through the world, or indeed the metaverse, it forms the basis for powerful surveillance technologies that ultimately are linked to the people who use these devices. This is a fundamental and unresolved challenge: is it possible to retain (or regain) privacy while also benefitting from strong security and safety posture of the products and services we use. Ethical goodwill and market positioning by product vendors are possibly parts of the solution. Legislative and regulatory approaches such as GDPR have had some positive effect; but, repeated violations demonstrate that this may be viewed as just a cost of business worth incurring. A technological solution that protects the privacy of system users while allowing them to benefit from underlying safety and security technologies would seem to be ideal. Whether this ideal can be achieved, and whether it will matter to users in the metaverse, are open questions. Have we entered the post-privacy era?

**Speaker Bio** :
Mike Borza is Synopsys Scientist working broadly on security in integrated circuits and systems at Synopsys, Inc. He has more than 25 years of leadership and technology experience in security and safety critical systems engineering. In 2002, he founded and was CTO of Elliptic Technologies, acquired by Synopsys in 2015. His previous experience includes Chrysalis-ITS (now Thales), Ankari (HID Global), and Alcatel Transport Automation (Thales Transport). He holds more than 20 US patents. He has been an active contributor to the security task group of IEEE 802.1, and was an editor of the 802.1 AR secure device identifier standard. He was vice-chair of the Accellera IP Security Assurance working group, and is a Principal Investigator in the DARPA Automatic Implementation of Secure Silicon (AISS) program.

**Ingrid Verbauwede**
KU Leuven



**Hardware: an essential partner to cryptography**

Ingrid Verbauwhede
KU Leuven,
Leuven, Belgium
https://www.esat.kuleuven.be/cosic/people/ingrid-verbauwhede/

**Abstract :**

Cryptography is a beautiful branch of mathematics with a nice goal of providing information security. To be useful in practical applications, the algorithms run on hardware or software, with software ultimately running also on hardware processors. This presentation covers multiple links of this relation between hardware and cryptography. The aim of the presentation is to link the mathematical goals of security and privacy with the challenges of hardware realizations. These challenges are multifold. First, hardware provides the means to accelerate the computationally demanding operations of cryptography. The most recent example is the realization of a new generation of post-quantum algorithms. A very nice aspect of cryptography is that it reduces what needs to be secret to the keys, while the algorithm itself can be publicly known. The hardware is responsible to keep the key(s) secret. Side-channel, fault-attacks and other physical attacks make this a challenging task.

Provable Secure mathematical countermeasures against physical attacks rely on models to abstract how the hardware behaves. Unfortunately, the models are often the weak link between theory and practice. As a result, many provable secure implementations are still broken in practice. Circuit designers learn how to optimize for area, throughput, latency, power and energy. These are the classical optimization goals. The elephant in the room is that the implementations also need to resist attacks. Countermeasures to resist timing, side-channel, fault, micro-architectural and other attacks have an implementation cost which add an extra design dimension.

**Speaker Bio** :

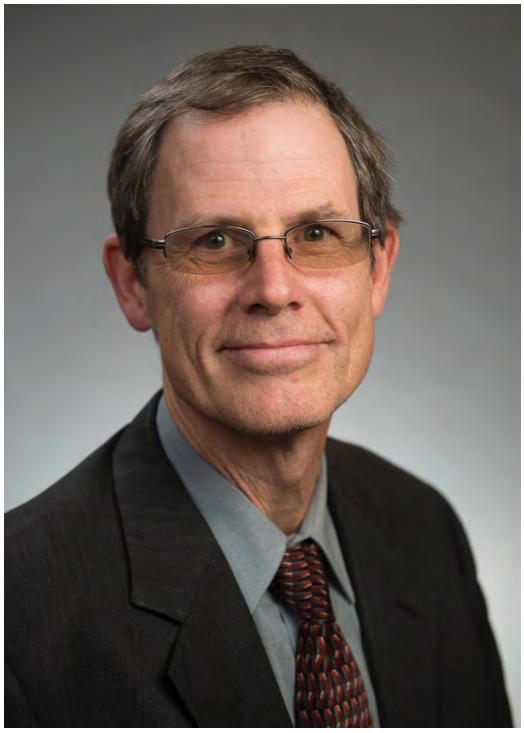
Dr Ir. Ingrid Verbauwhede is a Professor in the research group COSIC at the KU Leuven. She is a fellow of IEEE and of IACR. She is a member of the Royal Academy of Belgium in 2011. She is a recipient of two ERC Advanced Grant in 2016 and a second one in 2021. She received the IEEE 2017 Computer Society Technical Achievement Award. She delivered the 2022 IACR distinguished lecture. She will receive the 2023 IEEE D. Pederson award of the SSCS society.

She is a pioneer in the field of efficient and secure implementations of cryptographic algorithms on many different platforms: ASIC, FPGA, embedded, cloud. With her research she bridges the gaps between electronics, the mathematics of cryptography and the security of trusted computing. Her group owns and operates an advanced electronic security evaluation lab. Her list of publications is available from https://www.esat.kuleuven.be/cosic/people/ingrid-verbauwhede/ or https://scholar.google.com/citations?user=ZyG1ZGgAAAAJ&hl=en&oi=ao

**Panel Discussion:**

**Will information security be a reality for everyone?**

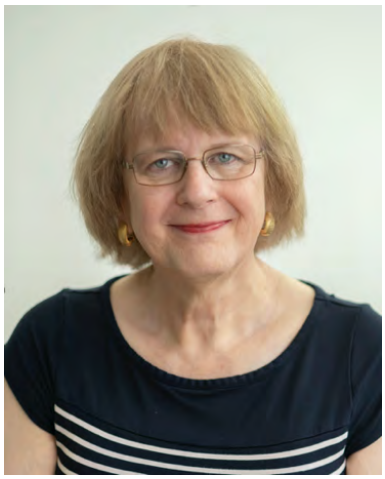
Chair: Wayne Burleson
University of Massachusetts, Amherst



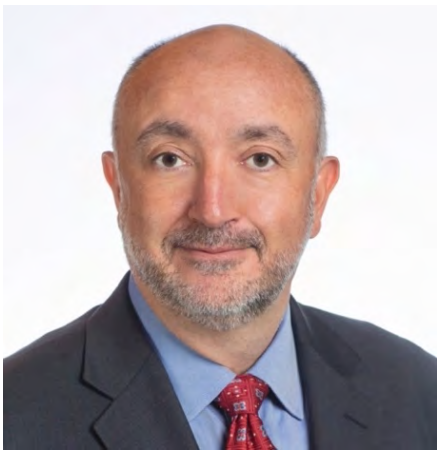
**Abstract:**

Security, safety and privacy are increasingly critical issues as technology permeates society and our lives. They are also difficult to define for different populations, especially in the Metaverse. Security, safety and privacy are also considered fundamental rights that should extend to all citizens of the world. Nevertheless, they are not equally available to all, especially the elderly, the under-educated and other disadvantaged groups. Hardware, software and AI technologies provide numerous security capabilities, but many vulnerabilities remain due to human and political factors. How should security, safety and privacy be balanced and designed into systems while still remaining affordable and accessible? Applications in medical, health, transportation, governance, education and finance present different scenarios, but share common challenges as well.

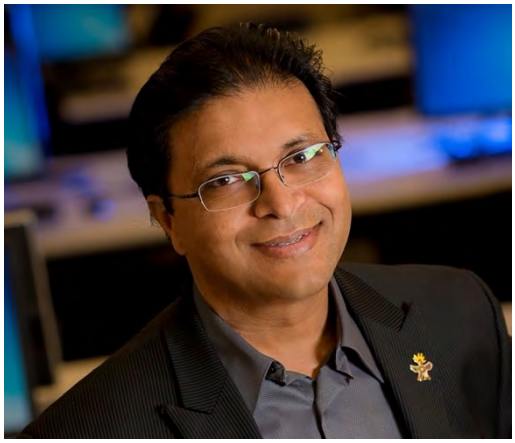
**Panelists** :



Marilyn Wolf, U.N. Lincoln

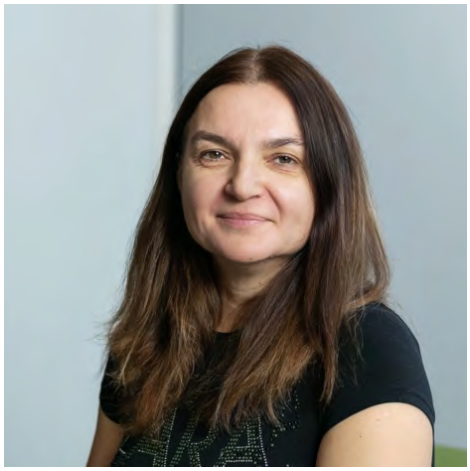


Yankin Tanurhan, Synopsys

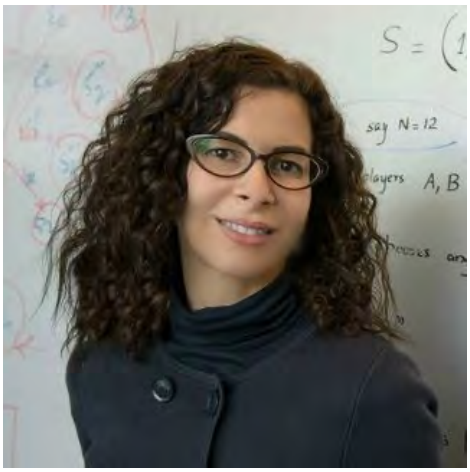


Rajesh Gupta, U.C. San Diego

Alena Simalatsar, HES-SO, Sion

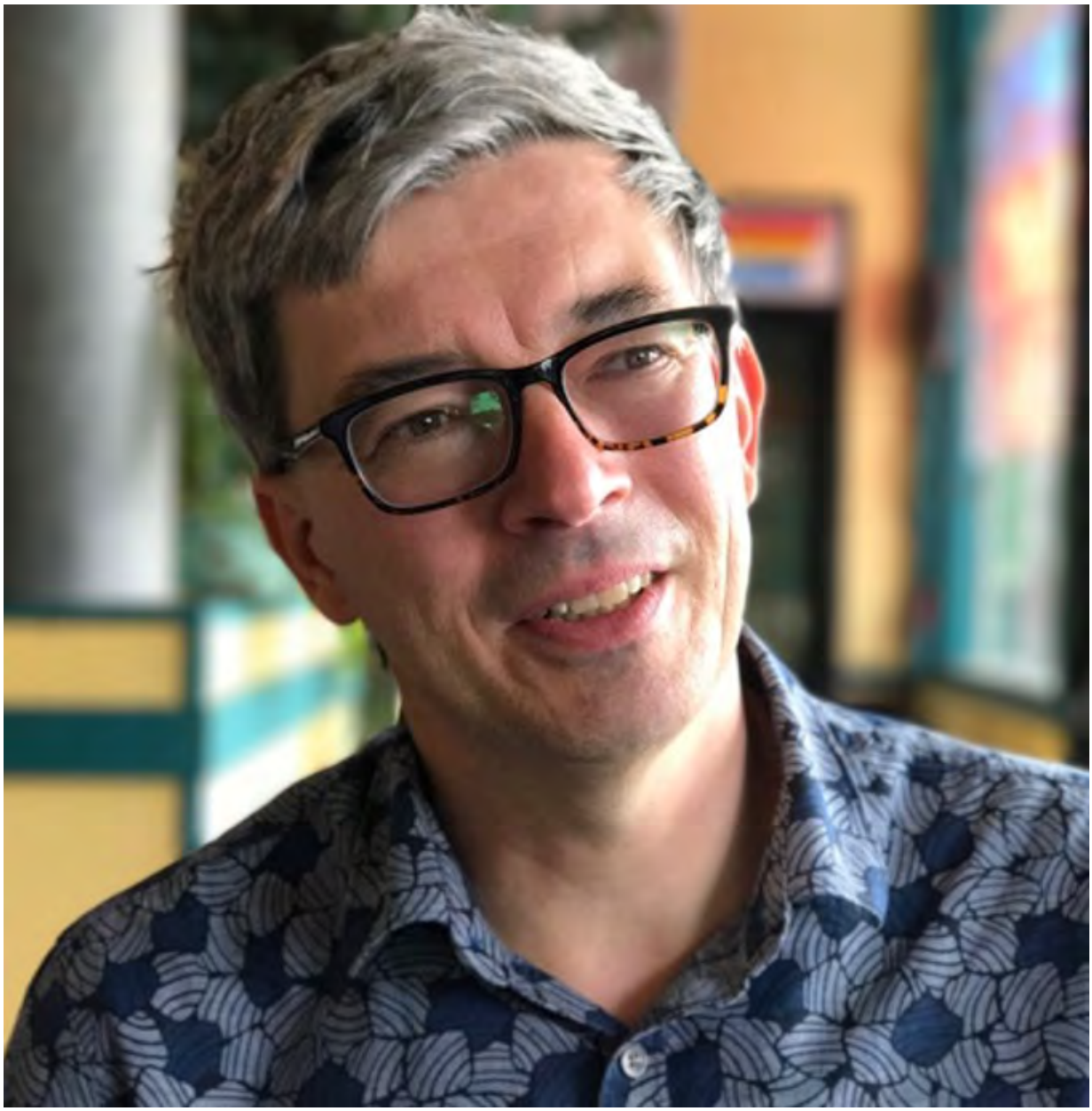


Lejla Batina, Radboud University




Farinaz Koushanfar, U.C. San Diego

**Patrick Groeneveld**
Cerebras Systems



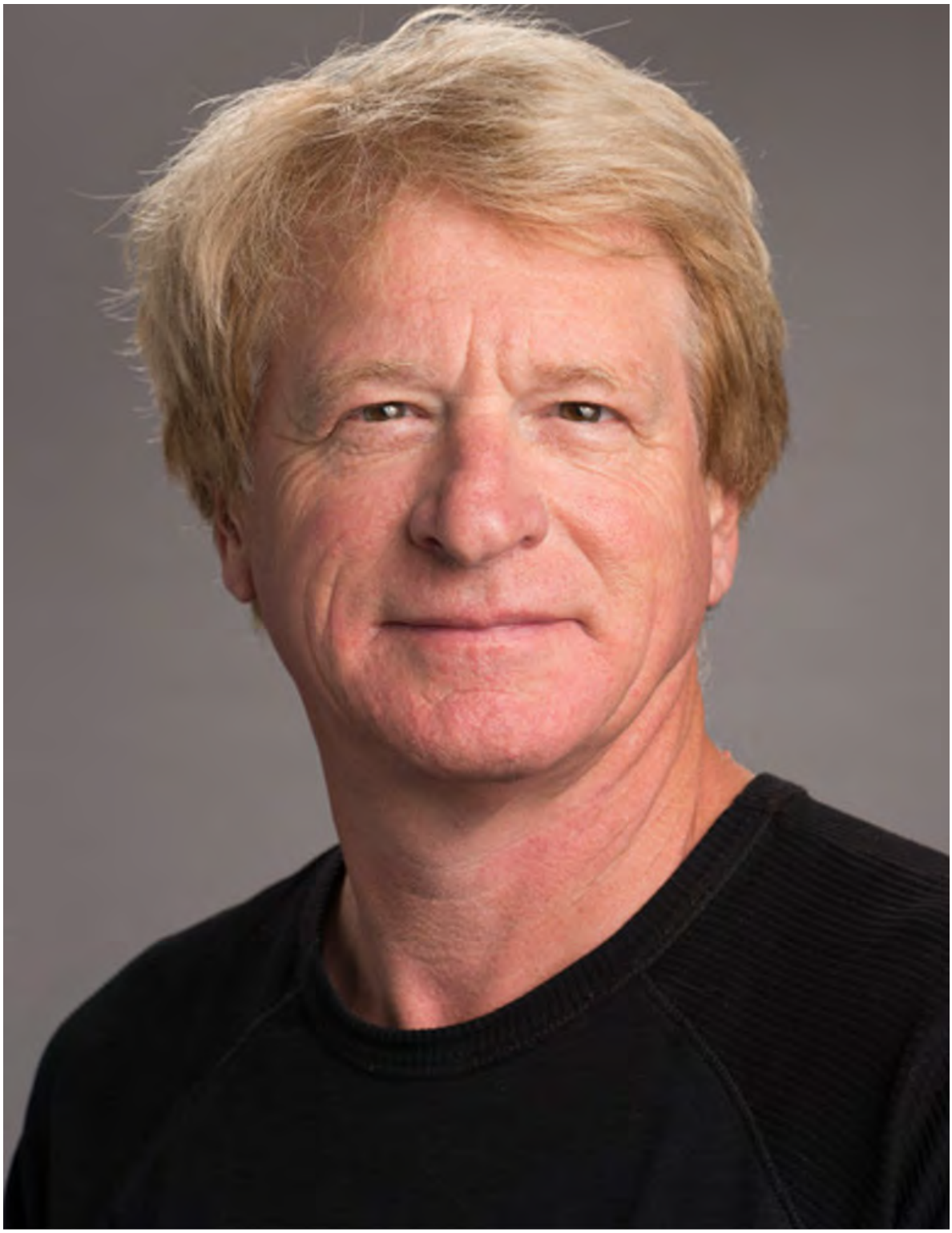
**Sustainable Innovation: Are we not fooling ourselves?**

Patrick Groeneveld
Cerebras Systems
prgr@stanford.edu

**Abstract:**
The Jevons paradox, a phenomenon first described by a 19th-century British economist, refers to the counterintuitive observation that technological improvements in efficiency can actually lead to increased - rather than reduced - resource consumption. In the case of mobile electronics, we can see this paradox at work, as the gains from Moore's law scaling are almost exclusively reinvested into additional features rather than energy savings. For instance, modern smartphones contain SoCs with 20 times more transistors than a decade ago. Currently the phone in our pocket may contain almost as many transistors as there are grains of sand on earth (!). But the power consumption has remained flat while improvements in functionality have been relatively modest. Another recent example can be seen in the significant energy required to power machine learning hardware, the increase of which far outstrips the rate of regular compute efficiency. Jevons paradox also applies to adjacent domains. While automotive propulsion has become more efficient, the gains are largely negated by the fact that cars have been growing into tall SUVs with oversized wheels that serve only aesthetic purposes. At this dinner presentation, we will discuss the scale of this paradox in microelectronics and in electrical systems more generally and consider how that might affect our goal of achieving sustainable innovation.

**Speaker Bio:**
Patrick Groeneveld currently focuses on machine learning hardware synthesis. At Cerebras Systems, a AI hardware startup, that hardware is the world's first monolithic supercomputer with 2.4 Trillion transistors. Patrick spent many years working in the EDA industry. During his tenure as Chief Technologist at Magma Design Automation, he was a part of the team that developed a groundbreaking RTL-to-GDS2 synthesis product. Additionally, Patrick served as a Full Professor of Electrical Engineering at Eindhoven University. Currently, he teaches a class in the EE department at Stanford University and also serves as the finance chair on the Executive Committee of the Design Automation Conference. Patrick received his MSc and PhD degrees from Delft University of Technology in the Netherlands.

**Jan Rabaey**
UC Berkeley



**The Mirror World – The Land between the Meta- and the Omniverse**

Jan M. Rabaey
University of California at Berkeley
*imec,* Belgium
*www.janrabaey.com*

**Abstract :**
In his 1992 novel Snow Crash, Neil Stephenson introduced the Metaverse, a virtual reality successor to the Internet. In his vision, humans represented by avatars frequent and explore an alternative world. Many decades later, the Metaverse concept is inspiring the next-generation products of social media and gaming companies such as "Meta", Microsoft, Epic Games and Magic Leap. Yet, sticking solely to an alternative world concept drastically reduces the potential footprint of these technologies. Our physical world and its population of biological and physical is increasingly being populated with a network of sensors and actuators. Hence one can imagine the emergence of a "mirror world", a virtual world that observes the operation of life on earth and potentially helps to inform and guide it. Think about traffic management with a mixture of humans and automata in the fold. This may resemble the "digital twin" concept, but the latter is more restrictive. One can imagine the mirror world looking forward in time considering multiple trajectories simultaneously, or play back the past (at least the way it has perceived it), leading in its most extreme form to an "omniverse". The mirror world must host avatars not only of humans but also of other biological beings and physical automata (cars, robots, drones, …). It further can be populated with virtual entities, representing for instance generative AI's.
Obviously, we are far from being capable of creating and operating such a mirror world, nor do we understand its usefulness and impact. At least, though, we can think about what it would take from a technological perspective. In this presentation, we will take a shot at identifying some of these needs.

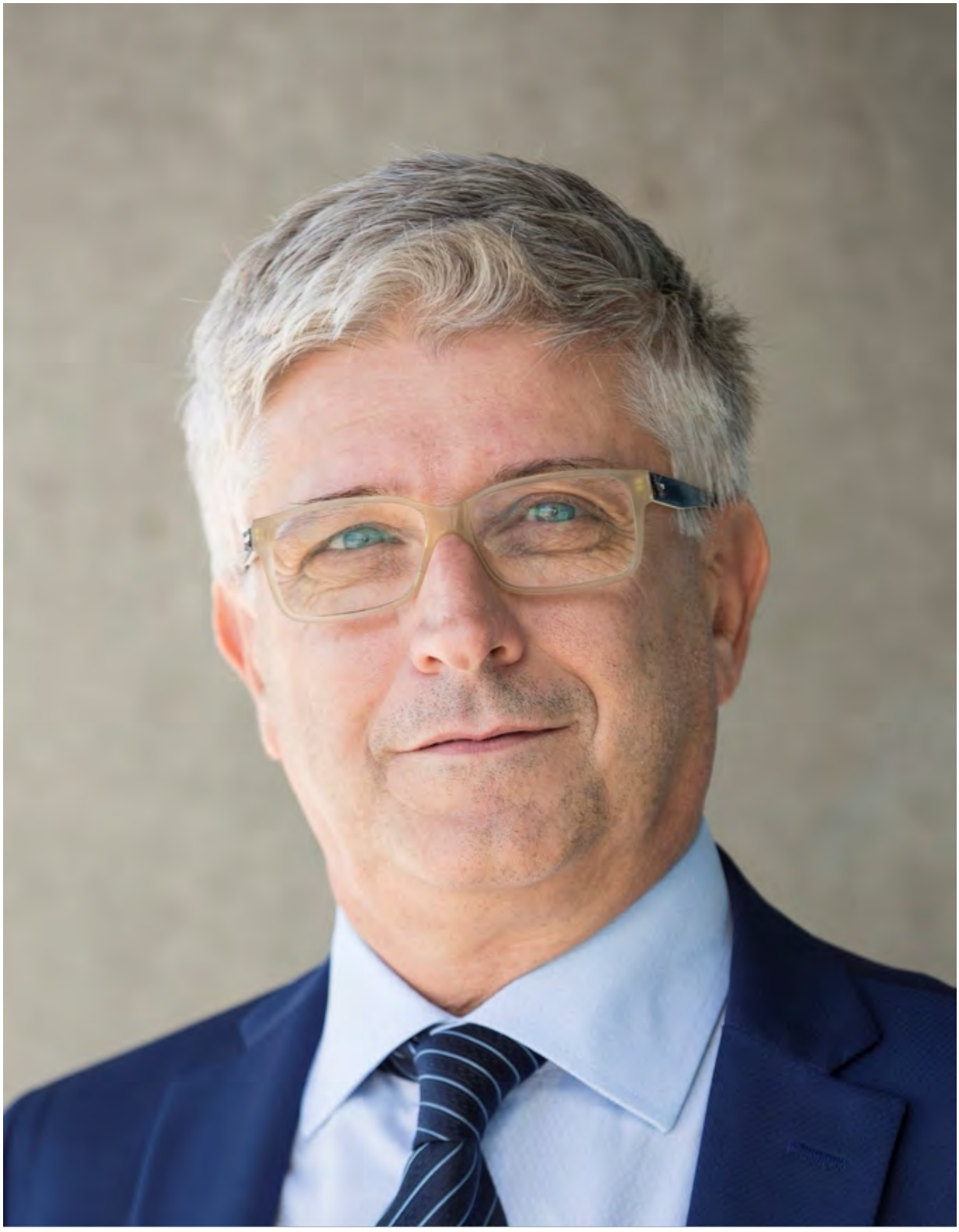
**Speaker Bio :**
Jan is a Professor in the Graduate School in the EECS Department the University of California at Berkeley, after being the holder of the Donald O. Pederson Distinguished Professorship at the same institute for over 30 years. He is a founding director of the Berkeley Wireless Research Center (BWRC) and the Berkeley Ubiquitous SwarmLab, and has served as the Electrical Engineering Division Chair at Berkeley twice. In 2019, he also became the CTO of the System-Technology Co-Optimization (STCO) Division of IMEC, Belgium.

Prof. Rabaey has made high-impact contributions to a number of fields, including low power integrated circuits, advanced wireless systems, mobile devices, sensor networks, and ubiquitous computing. Some of the systems he helped envision include the infoPad (a forerunner of the iPad), PicoNets and PicoRadios (IoT avant-la-lettre), the Swarm (IoT on steroids), Brain-Machine interfaces and the Human Intranet. His current interests include the conception of the next-generation distributed systems, as well as the exploration of the interaction between the cyber and the biological worlds.

He is the primary author of the influential "Digital Integrated Circuits: A Design Perspective" textbook that has served to educate hundreds of thousands of students all over the world. He is the recipient of numerous awards, is a Life Fellow of the IEEE, and has been involved in a broad variety of start-up ventures.

**Alessandro Cremonesi**

STMicroelectronics



**The *beauty* of being the "Enabler of the Future"**

Alessandro Cremonesi
Executive Vice President, Chief Innovation Officer General Manager,
System Research and Applications STMicroelectronics

**Abstract :**
You can look to the future from different application angles: IoT, AI, Metaverse, Robotics, ...and from different Industry sectors: Industrial, Mobility, Communications, Consumer, IT, Medical… and you discover that there is always a common enabler: the Semiconductor Industry and its related ecosystem.

The future will be fueled by a tide of innovation, continuous transformation spanning from physics and chemistry, through manufacturing equipment and design tools, to algorithms, data and software; from system-level components to heterogeneous integration.

In his speech Alessandro Cremonesi, Chief Innovation Officer at STMicroelectronics, will share his vision of the future, from the perspective of the tide of innovations that are just around the corner and will fuel once again the electronic industry... and our lives.

**Speaker Bio :**
Alessandro Cremonesi is STMicroelectronics' Executive Vice President, Chief Innovation Officer and General Manager of STMicroelectronics' System Research and Applications (SRA) Group. Cremonesi's responsibilities span from global innovation coordination to corporate advanced R&D to system-solutions support for ST customers.

He has been a key contributor to ST's extensive efforts and strategy in IoT and Artificial Intelligence and, more recently, has led the creation of strategic initiatives to increase ST's innovation capability.

He has authored several technical papers and patents and is a member of the Scientific Advisory Board at IMEC.

**Panel Discussion**

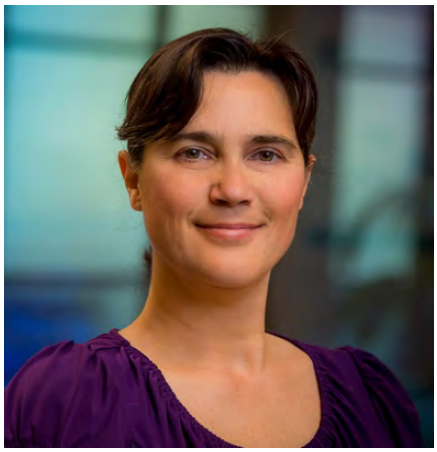
**Humans vs. things on the metaverse**

Chair: Jamil Kawa,
Synopsys

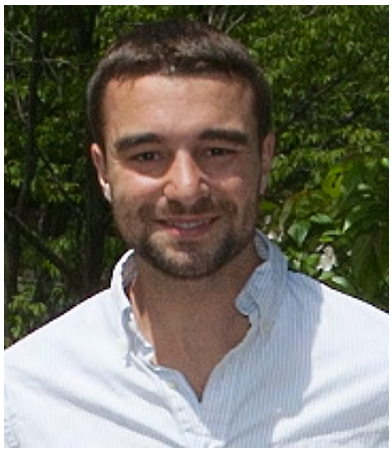
**Abstract:**

The metaverse has dramatically evolved since the term was coined back in 1992 by Neal Stephenson in his science fiction novel “Snow Crash”. It progressed from representing the Internet of Things to the Internet of Everything “IoE”, to a virtual world that encompasses augmented reality (AR), virtual reality (VR), 3D holographic avatars, and is moving along to include “smart objects”! It is considered by some to be the nucleus to a parallel universe. In this panel we’ll address the metaverse from an engineering and science perspective addressing issues related to the inclusion of actors beyond humans such as “smart objects”, we’ll address the potential of the metaverse to be an interconnected multiverse serving different applications, with different populations. We’ll also look at the possible evolution venues of the metaverse in the presence of AI and the security, safety and governance implications associated with that.

**Panelists**:

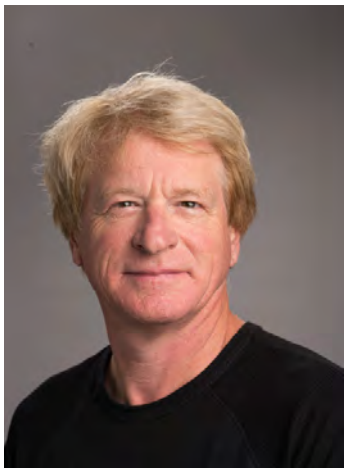


Tajana Simunic, U.C. San Diego



Joseph Friedman, U.T. Austin

David Atienza, EPFL



Jan Rabaey, U.C. Berkeley

Victor Grimblatt, Synopsys

**Tibor Mérey**

Boston Consulting Group

**How the Metaverse will Remake your Strategy**

Tibor Mérey
Managing Director & Partner
BCG Gamma/Boston Consulting Group
https://www.bcg.com/de-at/about/people/experts/tibor-merey

***Abstract :***

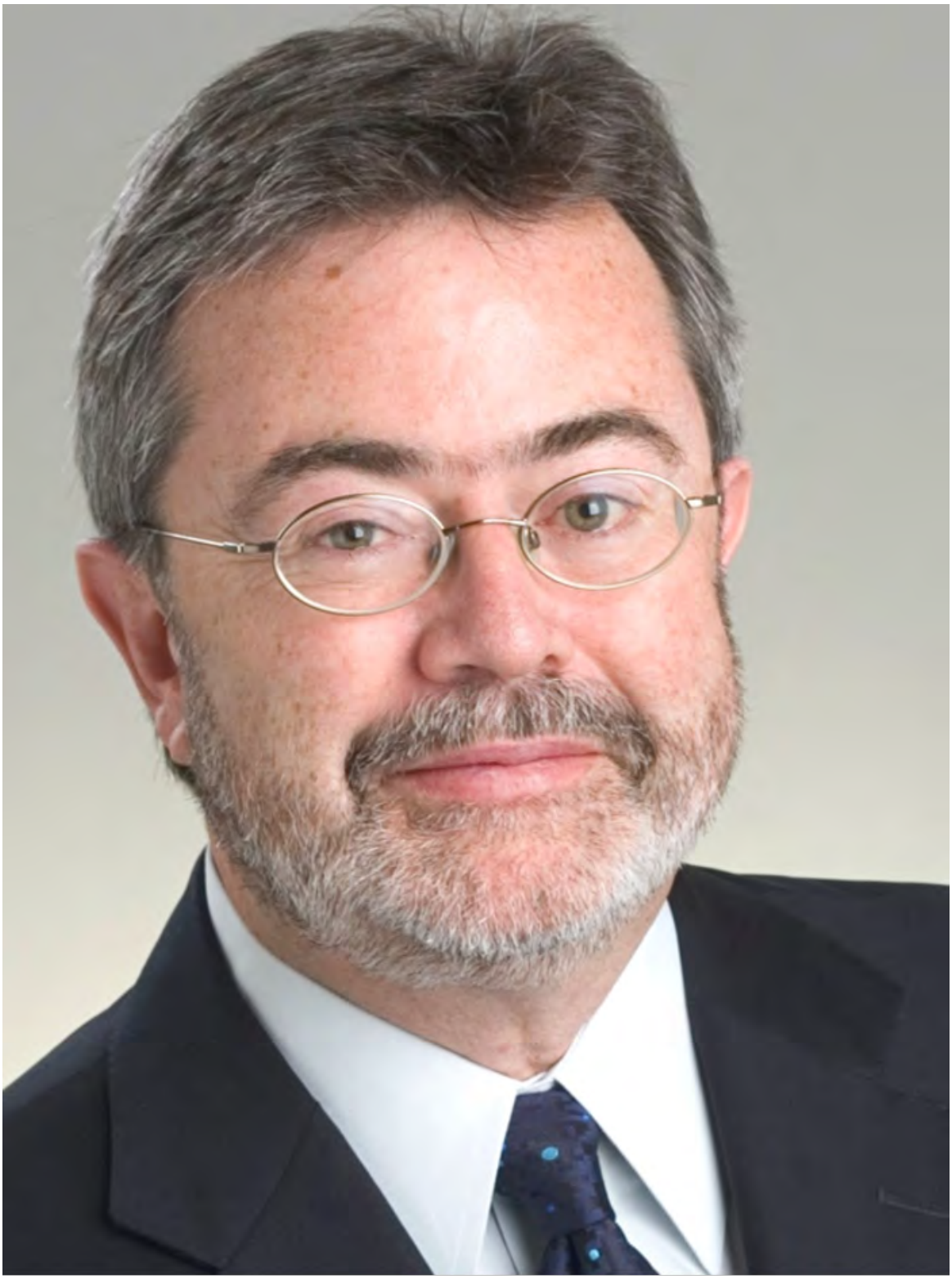
The metaverse is a futuristic idea - but the origin of the term actually lies in the past. Almost 30 years ago, to be precise. Author Neal Stephenson coined the term "metaverse" in his 1992 science fiction novel Snow Crash, in which he imagines a successor to the Internet based on virtual reality - but what exactly is the metaverse? Recall the introduction of the iPhone in 2007 - a single device that combined camera, computer, cell phone and operating system. Similarly, the metaverse is about the convergence of multiple developments, all of which involve incremental changes in technological capabilities - Metaworlds, immersive technologies (AR/VR/XR), and Web3. Tibor Mérey's keynote will explore how the convergence of these technologies will force companies to remake their strategies to stay relevant and reap the benefits which are being sown today.

***Speaker Bio :***

Tibor Mérey, Managing Director and Partner of BCG Gamma/Boston Consulting Group. Stations: Studies in Business Administration in St. Gallen, Finance (Barcelona), International Management (Sydney). 2018 Interim Head of Existing Customer Management at leading European telecommunications company. Today, as one of the global metaverse experts, deals with the economic potentials of the metaverse and supports customers in identifying and implementing the new technology with suitable use cases. His main focus: the acceleration of digitization with a focus on data-driven growth and the integration of artificial intelligence. With this expertise, he advises a wide variety of companies worldwide "The Metaverse will affect everything and everyone of us affect the way we live and work...”

**Raul Camposano**

Silvaco



**Digital Twins for Semiconductor Manufacturing**

Raúl Camposano
Silvaco, CTO
Silicon Catalyst, Partner
Stanford University, Adjunct Lecturer
https://silvaco.com/corporate/management/ https://siliconcatalyst.com/our-team

**Abstract :**

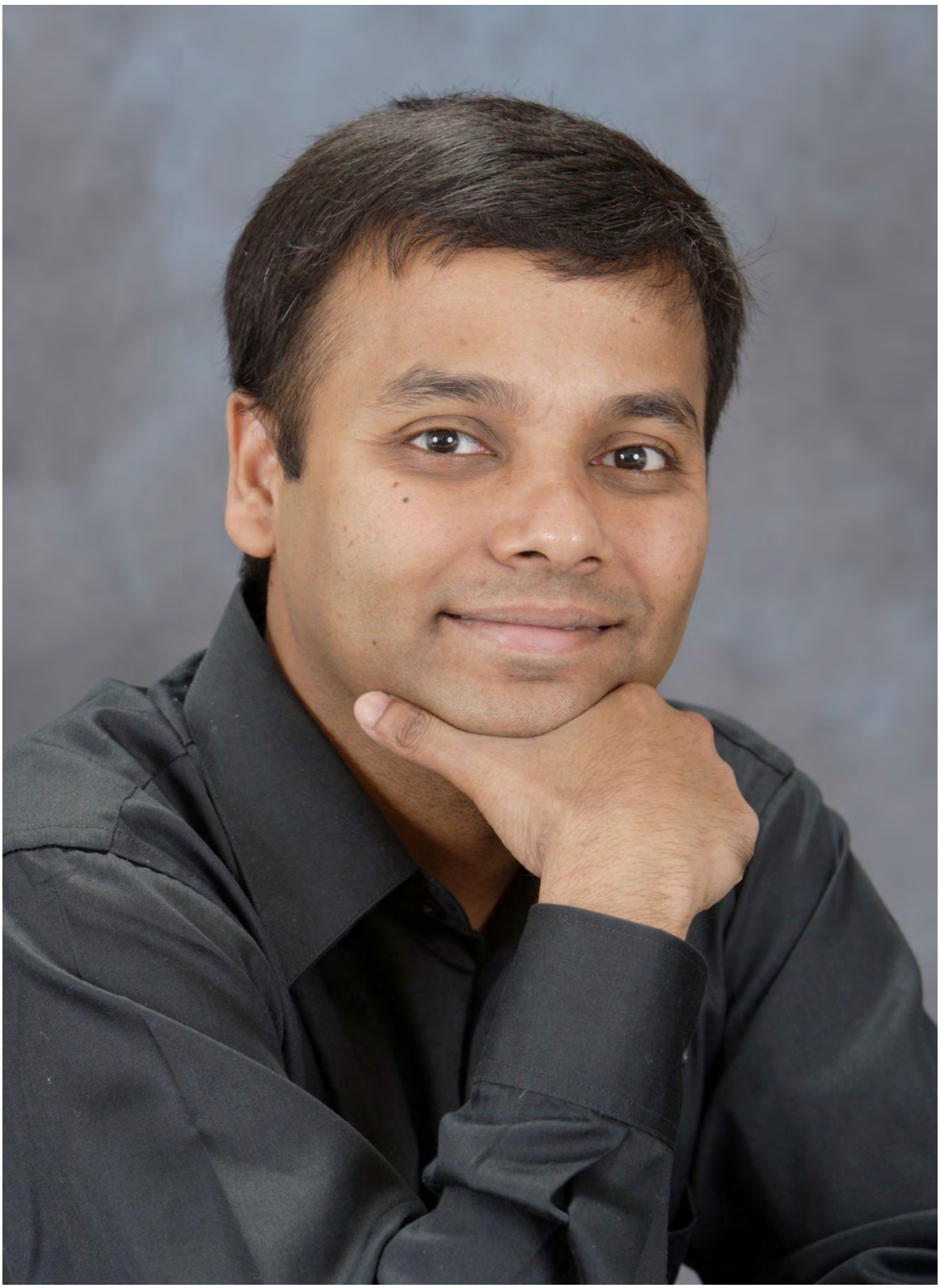
The mass production of semiconductors is a crucial aspect of the economy and is of strategic importance. A state-of-the-art semiconductor manufacturing facility can cost over $10B and can produce over 9 million 12-inch wafers. Technology Computer-Aided Design (TCAD) models are used to simulate the fabrication and operation of semiconductor devices. TCAD has become essential in the deployment of new semiconductor technology. With increasing accuracy, TCAD models can now be used as "digital twins" to simulate and optimize semiconductor manufacturing processes. Now these models are producing results that are accurate enough to be used as “digital twins”. The concept and model of the digital twin was introduced in 2002 by Michael Grieves. The accuracy threshold for a digital twin can vary depending on the application, with some models approaching the level of "exactness" described in Borges’ 1946 story: “cartography becomes so exact that only a map on the same scale as the empire itself will suffice”.

This opens up many new applications, such as virtual development of new semiconductor technology, reducing the need for physical experimentation, and ultimately shortening development time and time to yield. Digital twins can also be used during production in the fab to further optimize processes, monitor variations, and detect malfunctions. This presentation will delve into these concepts and provide examples of TCAD that can be used as digital twins.

**Speaker Bio :**

Raúl is currently the CTO of Silvaco. He is also a partner at Silicon Catalyst, an incubator for semiconductor solutions, and lectures on EDA and Machine Learning Hardware at Stanford. He was previously an advisor to Applied Materials and the CEO of Sage Design Automation acquired by Applied in 2020. He was also CEO of Nimbic, acquired by Mentor Graphics in 2014. Raúl spent most of his career with Synopsys, where he served as Chief Technology Officer, Senior Vice President, and General Manager. Prior to joining Synopsys, he was a Director for the German National Research Center for Computer Science, Professor of Computer Science at the University of Paderborn, and a Research Staff Member at the IBM T.J. Watson Research Center. Raúl holds a B.S and M.S. in Electrical Engineering from the University of Chile, and a Ph.D. in Computer Science from the University of Karlsruhe. He has published over 70 technical papers and written and/or edited three books on electronic design automation. Raúl has contributed significantly to building the design community serving on numerous editorial, advisory and company boards. Raúl was also an Advisory Professor at Fudan University and the Chinese Academy of Sciences. He was elected a Fellow of the IEEE in 1999 and to the board of directors of ESDA (aka EDAC, the EDA Consortium) in 2012.

**Subhasish Mitra**
Stanford University



# The Future of Hardware Technologies for Computing

Subhasish Mitra
Department of Electrical Engineering and Department of Computer Science
Stanford University
http://stanford.edu/~subh

**Abstract :**
The computation demands of 21st-century abundant-data workloads, such as AI/machine learning, far exceed the capabilities of today's computing systems. For example, a Dream AI Chip would ideally co-locate all memory and compute on a single chip, quickly accessible at low energy. Such Dream Chips aren't realizable today. Computing systems instead use large off-chip memory and spend enormous time and energy shuttling data back-and-forth. This memory wall gets worse with growing problem sizes, especially as conventional transistor miniaturization gets increasingly difficult.

The next leap in computing requires transformative NanoSystems by exploiting unique characteristics of nanotechnologies and abundant-data workloads. We create new chip architectures through ultra-dense 3D integration of logic and memory – the *N3XT 3D* approach. Multiple *N3XT 3D* chips are integrated through a continuum of chip stacking/interposer/wafer-level integration — the *N3XT 3D MOSAIC*. To scale with growing problem sizes, new *Illusion systems* orchestrate workload execution on *N3XT 3D MOSAIC* creating an illusion of a Dream Chip with near-Dream energy and throughput.

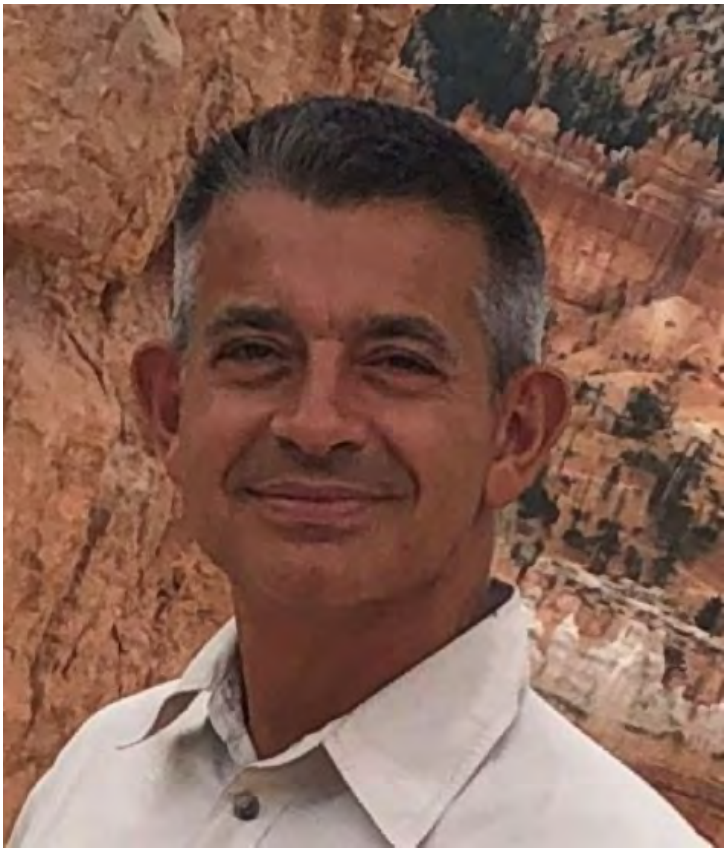
Several hardware prototypes, built in commercial and research fabrication facilities, demonstrate the effectiveness of our approach. We target 1,000X system-level energy-delay-product benefits, especially for abundant-data workloads. We also address new ways of ensuring robust system operation despite growing challenges of design bugs, manufacturing defects, reliability failures, and security attacks.

**Speaker Bio :**
Subhasish Mitra is Professor of Electrical Engineering and of Computer Science at Stanford University. He is also the Associate Chair (Faculty Affairs) of Computer Science. Prof. Mitra directs the Stanford Robust Systems Group, leads the Computation Focus Area of the Stanford SystemX Alliance, and is a member of the Wu Tsai Neurosciences Institute. His research ranges across Robust Computing, NanoSystems, Electronic Design Automation (EDA), and Neurosciences. Results from his research group have influenced almost every contemporary electronic system, and have inspired significant government and research initiatives in multiple countries. Prof. Mitra also has consulted for major technology companies including Cisco, Google, Intel, Samsung, and Xilinx. His honors include the Harry H. Goode Memorial Award (by the IEEE Computer Society for outstanding contributions in the information processing field), Newton Technical Impact Award in EDA (test-of-time honor by ACM SIGDA and IEEE CEDA), the University Researcher Award (by the Semiconductor Industry Association and Semiconductor Research Corporation to recognize lifetime research contributions), the Intel Achievement Award (Intel's highest honor), and the US Presidential Early Career Award. He and his students have published over 10 award-winning papers across 5 topic areas (technology, circuits, EDA, test, verification) at major venues including Design Automation Conference, International Solid-State Circuits Conference, International Test Conference, Symposium on VLSI Technology, Symposium on VLSI Circuits, and Formal Methods in Computer-Aided Design. Stanford undergraduates have honored him several times "for being important to them." He is an ACM Fellow, an IEEE Fellow, a foreign member of Academia Europaea, and a Distinguished Alumnus of the Indian Institute of Technology, Kharagpur.

**Panel Discussion:**

**Is *In-Memory Computing* a niche area or the main hardware platform for AI/ML?**

Chair: Luca Benini
ETHZ

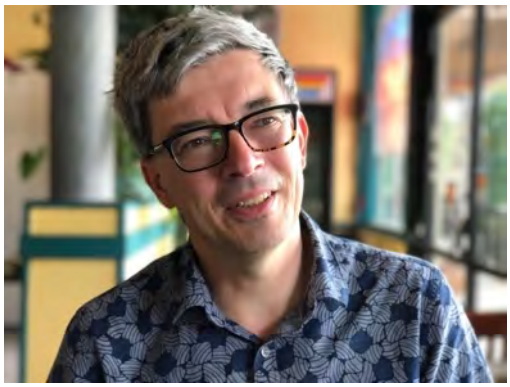


**Abstract:**

The skyrocketing needs for data manipulation coming from the current AI/ML wave is shaking the way we consider computing. In this context, large academic and industrial research efforts are looking at computing paradigms where processing can be made directly in the memory, effectively avoiding costly data transfers. This panel will explore the promises and challenges associated with in-memory computing. It will discuss the implications on hardware architectures, software models, viability to aggressive technologies nodes and will seek to establish if computing-in-memory will be the holy grail for AI/ML hardware platforms.

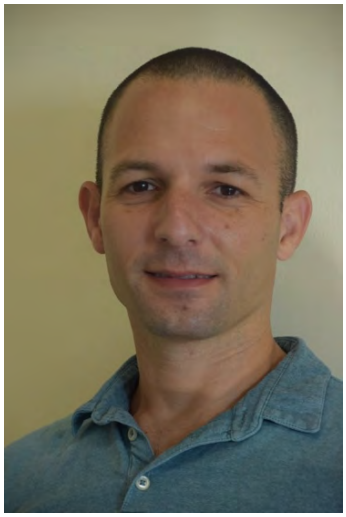
**Panelists :**

Amrita Mathuria, Kepler Computing



Patrick Groeneweld, Cerebras

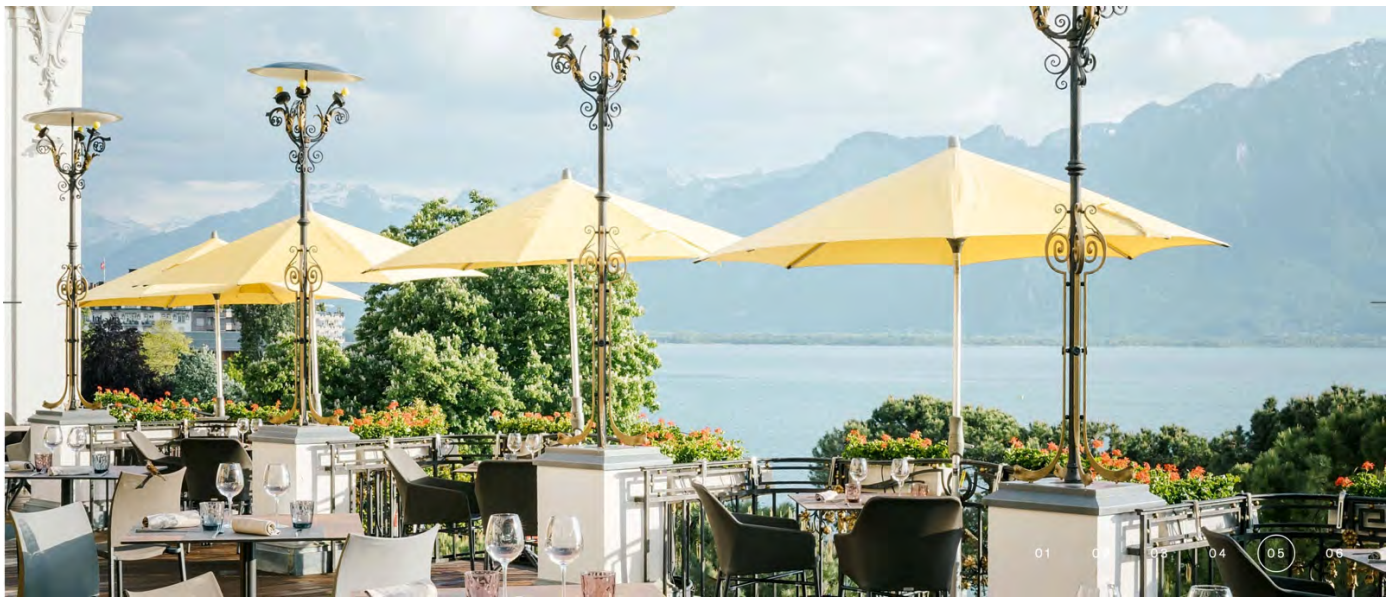
Daniele Ielmini, Politecnico di Milano



Shahar Kvatinsky, Technion

Abu Sebastian, IBM Research, Zurich

Pierre-Emmanuel Gaillardon, University of Utah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